

HAT1096C

Silicon P Channel MOS FET
Power Switching

R07DS1175EJ0500
(Previous: REJ03G1233-0400)
Rev.5.00
Mar 19, 2014

Features

- Low on-resistance
 $R_{DS(on)} = 225 \text{ m}\Omega$ typ. (at $V_{GS} = -4.5 \text{ V}$)
- Low drive current.
- 2.5 V gate drive devices.
- High density mounting

Outline

RENESAS Package code: PWSF0006JA-A
(Package name: CMFPAK-6)

1. Source
2. Drain
3. Drain
4. Drain
5. Drain
6. Gate

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source voltage	V_{DSS}	-20	V
Gate to Source voltage	V_{GSS}	± 12	V
Drain current	I_D	-1	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	-4	A
Body - Drain diode reverse drain current	I_{DR}	-1	A
Channel dissipation	P_{ch} ^{Note 2}	790	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. When using the glass epoxy board. (FR4 $40 \times 40 \times 1.6\text{mm}$), $T_a = 25^\circ\text{C}$

Electrical Characteristics

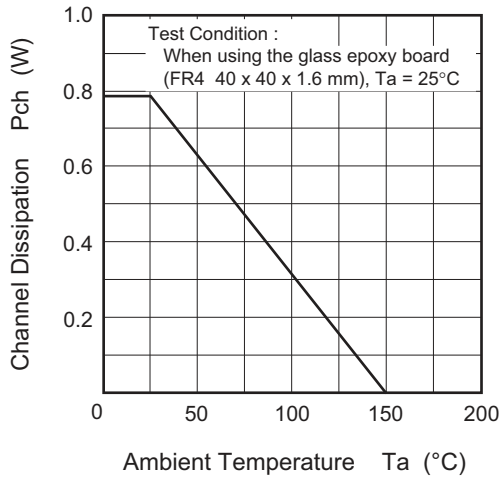
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to Source breakdown voltage	$V_{(BR)DSS}$	-20	—	—	V	$I_D = -10 \text{ mA}, V_{GS} = 0$
Gate to Source breakdown voltage	$V_{(BR)GSS}$	± 12	—	—	V	$I_G = \pm 100 \mu\text{A}, V_{DS} = 0$
Gate to Source leakage current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 10 \text{ V}, V_{DS} = 0$
Drain to Source leakage current	I_{DSS}	—	—	-1	μA	$V_{DS} = -20 \text{ V}, V_{GS} = 0$
Gate to Source cutoff voltage	$V_{GS(th)}$	-0.4	—	-1.4	V	$I_D = -1 \text{ mA}, V_{DS} = -10 \text{ V}$ ^{Note3}
Drain to Source on state resistance	$R_{DS(on)}$	—	225	293	m Ω	$I_D = -0.5 \text{ mA}, V_{GS} = -4.5 \text{ V}$ ^{Note3}
	$R_{DS(on)}$	—	380	530	m Ω	$I_D = -0.5 \text{ mA}, V_{GS} = -2.5 \text{ V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	0.6	0.9	—	S	$I_D = -0.5 \text{ mA}, V_{DS} = -10 \text{ V}$ ^{Note3}
Input capacitance	C_{iss}	—	155	—	pF	$V_{DS} = -10 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	40	—	pF	
Reverse transfer capacitance	C_{rss}	—	30	—	pF	
Total gate charge	Q_g	—	2	—	nC	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_D = -1 \text{ A}$
Gate to Source charge	Q_{gs}	—	0.4	—	nC	
Gate to Drain charge	Q_{gd}	—	0.6	—	nC	
Turn - on delay time	$t_{d(on)}$	—	12	—	ns	$V_{DS} = -10 \text{ V}, V_{GS} = -4.5 \text{ V},$ $I_D = -0.5 \text{ A}, R_L = 20 \Omega,$ $R_g = 4.7 \Omega$
Rise time	t_r	—	18	—	ns	
Turn - off delay time	$t_{d(off)}$	—	28	—	ns	
Fall time	t_f	—	8	—	ns	
Body - Drain diode forward voltage	V_{DF}	—	-0.85	-1.1	V	$I_F = -1 \text{ A}, V_{GS} = 0$

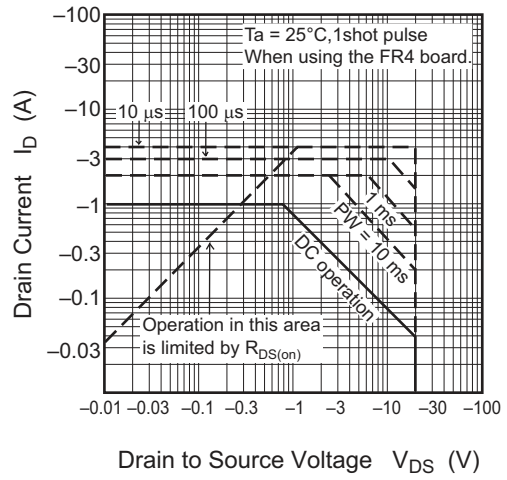
Notes: 3. Pulse test

Main Characteristics

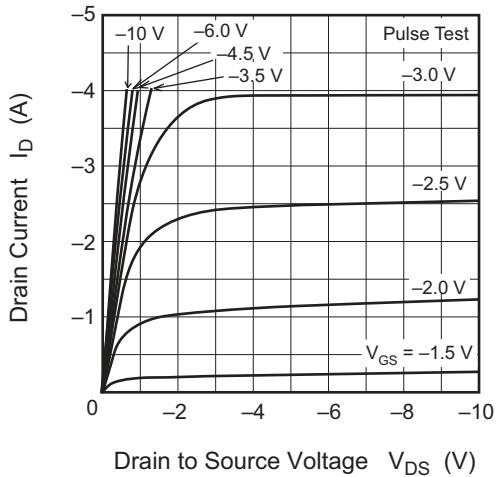
Power vs. Temperature Derating



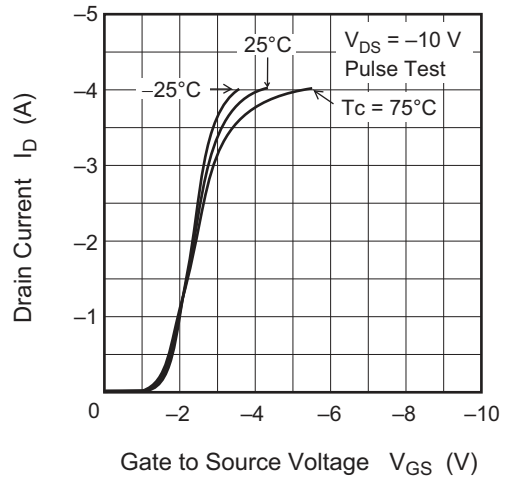
Maximum Safe Operation Area



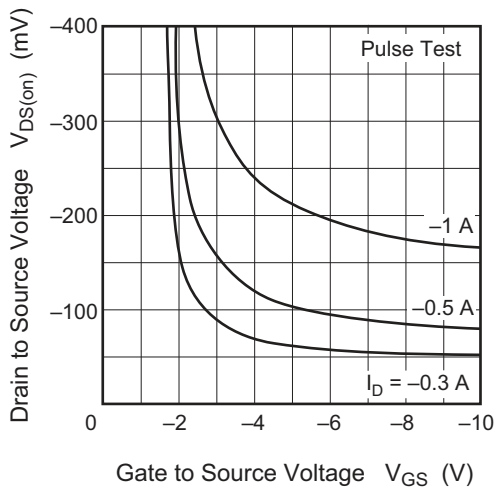
Typical Output Characteristics



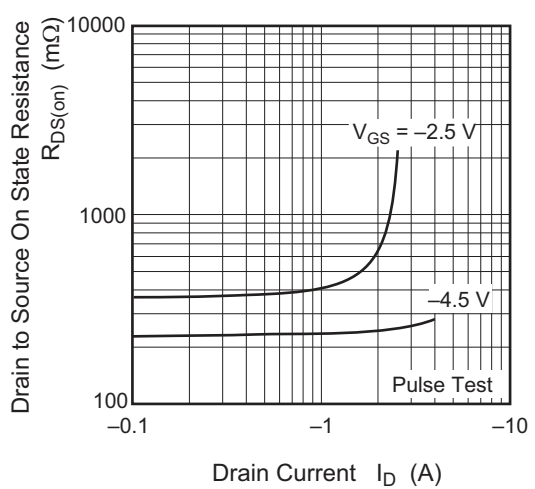
Typical Transfer Characteristics

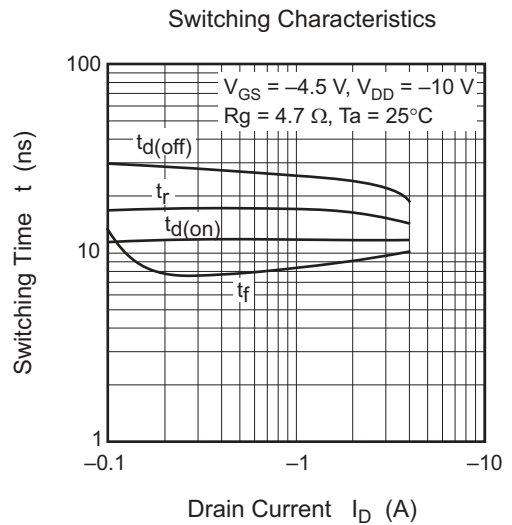
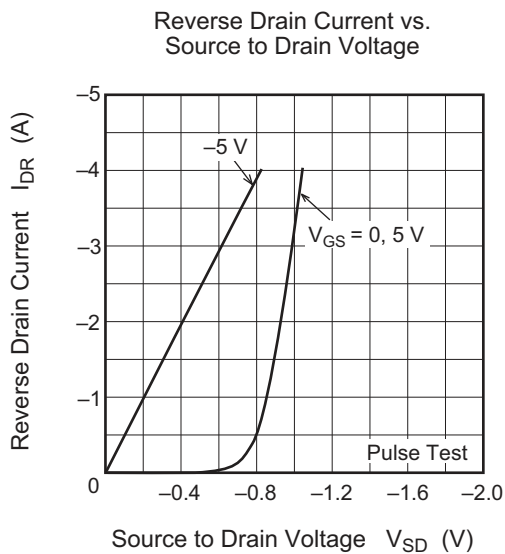
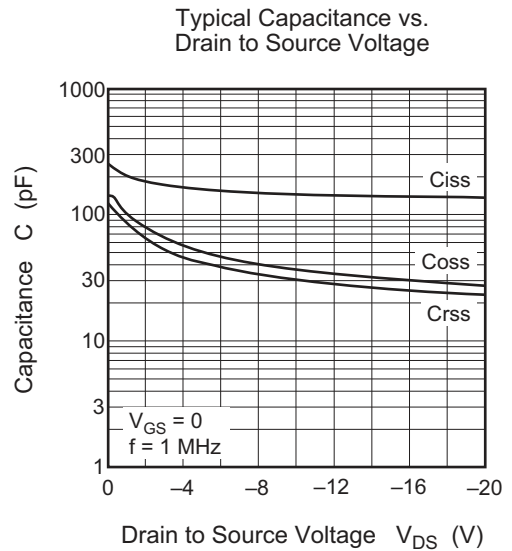
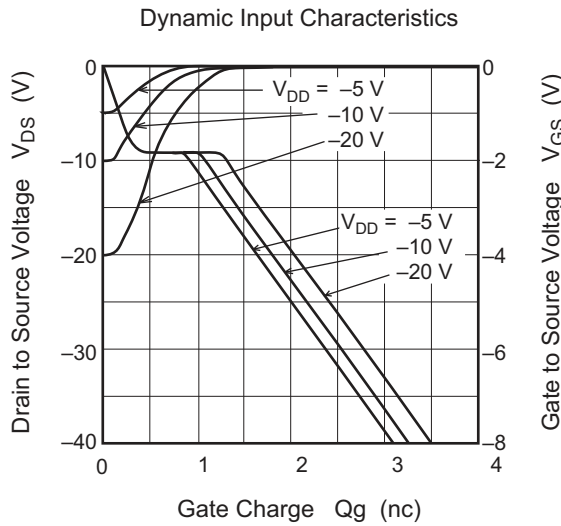
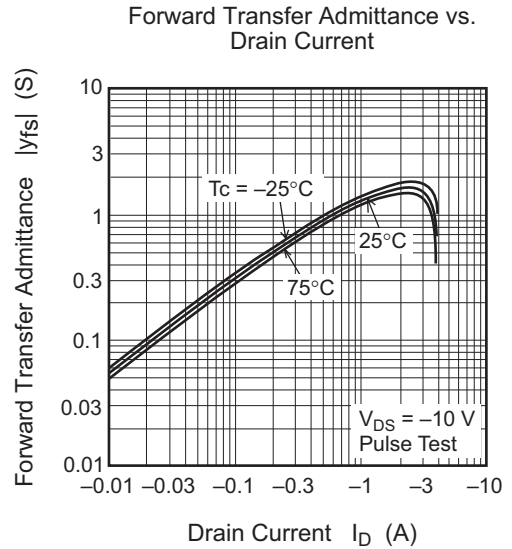
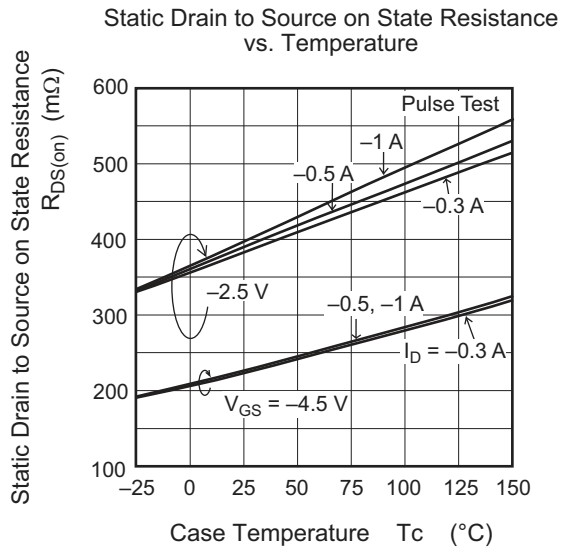


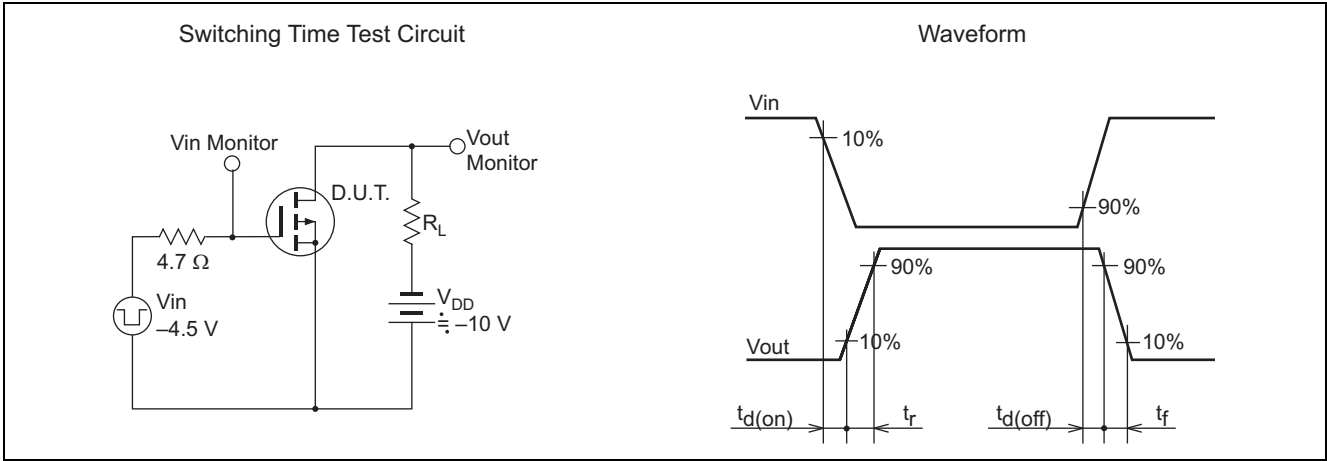
Drain to Source Saturation Voltage vs. Gate to Source Voltage



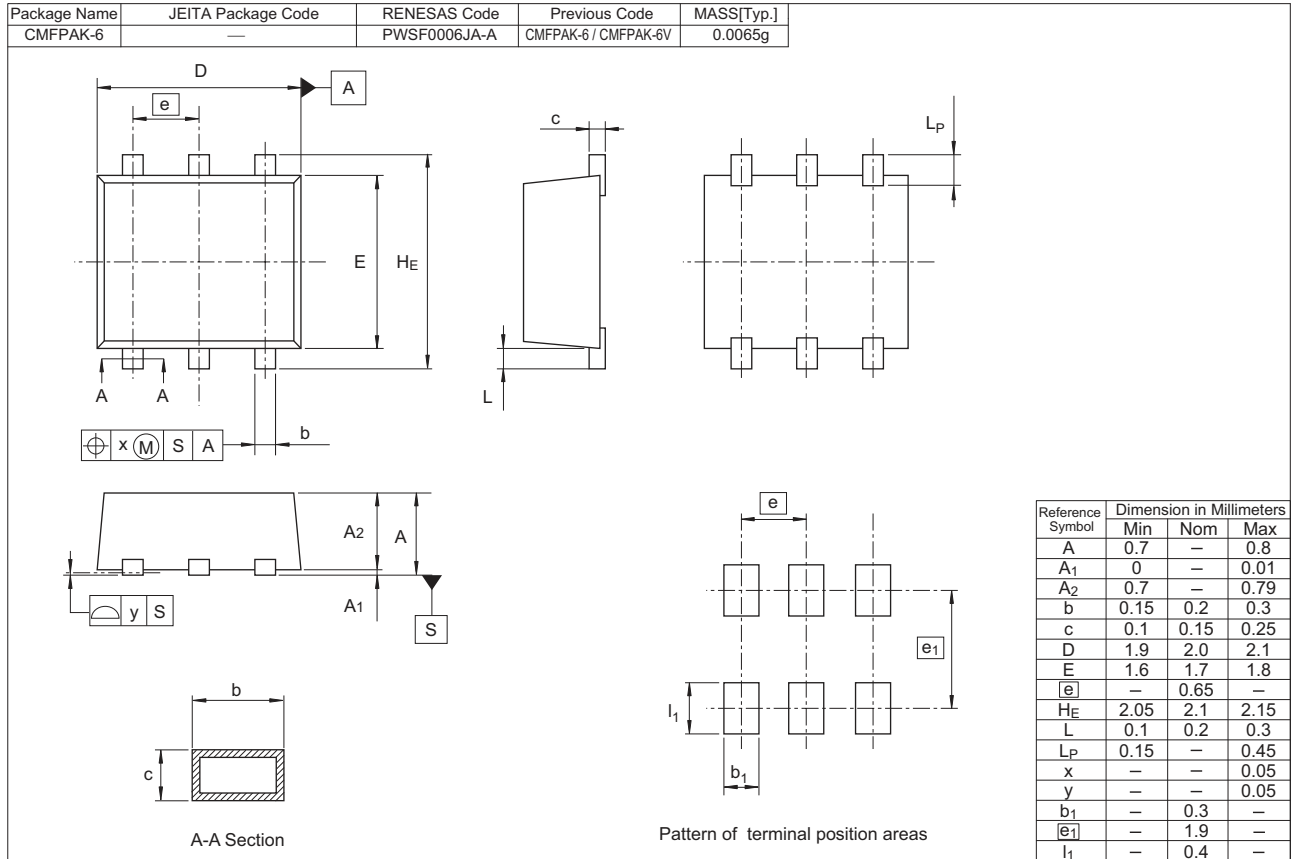
Static Drain to Source on State Resistance vs. Drain Current







Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
HAT1096C-EL-E	3000 pcs	Taping

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