

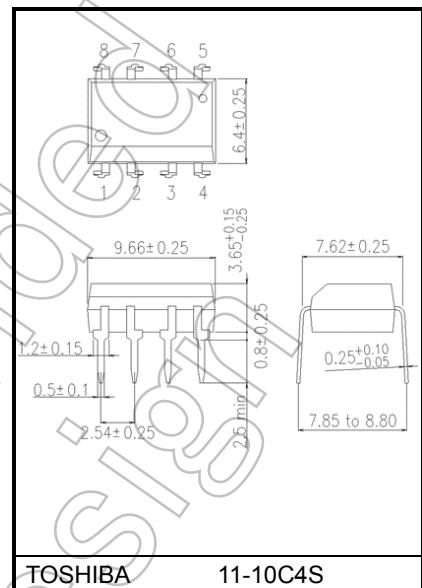
TLP2530, TLP2531

Digital Logic Isolation
 Line Receiver
 Power Supply Control
 Switching Power Supply
 Industrial Inverter

Unit: mm

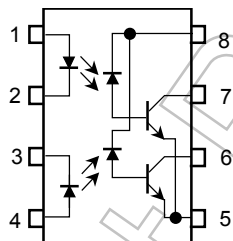
The TOSHIBA TLP2530 and TLP2531 dual photocouplers consist of a pair of infrared emitting diode and integrated photodetector. This unit is 8-lead DIP. Separate connection for the photodiode bias and output transistor collectors improve the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base-collector capacitance.

- TTL compatible
- Switching speed: $t_{pHL} = 0.2 \mu s$, $t_{pLH} = 0.3 \mu s$ (typ.)
 (@ $R_L = 1.9 k\Omega$)
- Guaranteed performance over temp: $0^\circ C$ to $70^\circ C$
- Isolation voltage: 2500 Vrms (min)
- UL-recognized: UL1577, File No.E67349
- cUL-recognized: CSA Component Acceptance Service No.5A
 File No.E67349



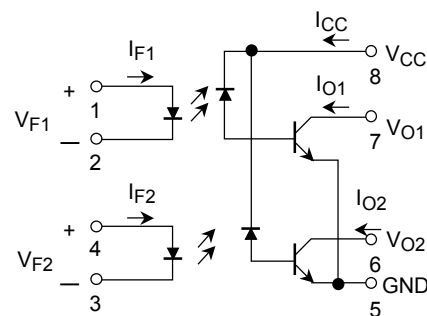
Weight: 0.54 g (typ.)

Pin Configuration (top view)



- 1. : Anode.1
- 2. : Cathode.1
- 3. : Cathode.2
- 4. : Anode.2
- 5. : GND
- 6. : V_{O2} (output 2)
- 7. : V_{O1} (output 1)
- 8. : V_{CC}

Schematic



Start of commercial production
 1986-03

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current (each channel)	I_F	25	mA
	Forward current derating (each channel) (Ta > 70 °C)	$\Delta I_F/T_a$	-0.8	mA / °C
	Pulse forward current (each channel) (Note 1)	I_{FP}	50	mA
	Pulse forward current derating (each channel) (Ta > 70 °C)	$\Delta I_{FP}/T_a$	-1.6	mA / °C
	Total pulse forward current (each channel) (Note 2)	I_{FPT}	1	A
	Reverse voltage (each channel)	V_R	5	V
	Diode power dissipation (each channel)	P_D	45	mW
	Diode power dissipation derating (each channel) (Ta > 70 °C)	$\Delta P_D/T_a$	-0.8	mW / °C
Detector	Output current (each channel)	I_O	8	mA
	Peak output current (each channel)	I_{OP}	16	mA
	Output voltage (each channel)	V_O	-0.5 to 15	V
	Supply voltage	V_{CC}	-0.5 to 15	V
	Output power dissipation (each channel)	P_O	35	mW
	Output power dissipation derating (each channel) (Ta > 70 °C)	$\Delta P_O/T_a$	-0.6	mW / °C
Operating temperature range		T_{opr}	-55 to 100	°C
Storage temperature range		T_{stg}	-55 to 125	°C
Lead solder temperature (10 s) (Note 3)		T_{sol}	260	°C
Isolation voltage (AC, 60 s, R.H. ≤ 60 %) (Note 4)		BV_S	2500	Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: 50 % duty cycle, 1 ms pulse width.

Note 2: Pulse width ≤ 1 μs, 300 pps.

Note 3: 2 mm below seating plane.

Note 4: Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Recommended Operating Conditions

Characteristic	Symbol	Min	Typ.	Max	Unit
Supply voltage	V_{CC}	0	—	12	V
Forward current (each channel)	I_F	—	16	25	mA
Operating temperature	T_{opr}	-25	—	85	°C

Note: Recommended operating conditions are given as a design guideline to obtain expected performance of the device. Additionally, each item is an independent guideline respectively. In developing designs using this product, please confirm specified characteristics shown in this document.

Electrical Characteristics (Ta = 0°C to 70°C, unless otherwise noted)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Input forward voltage (each channel)		V _F	I _F = 16 mA, Ta = 25 °C	—	1.65	1.7	V
Temperature coefficient of forward voltage (each channel)		ΔV _F / ΔTa	I _F = 16 mA	—	-2	—	mV/°C
Input reverse breakdown voltage (each channel)		BV _R	I _R = 10 μA, Ta = 25 °C	5	—	—	V
Input capacitance (each channel)		C _T	f = 1 MHz, V _F = 0 V	—	45	—	pF
Logic high output current (each channel)		I _{OH}	I _F = 0 mA, V _O = V _{CC} = 5.5 V Ta = 25 °C	—	3	500	nA
			I _F = 0 mA, V _O = V _{CC} = 15 V	—	—	50	μA
Logic low supply current		I _{CCL}	I _{F1} = I _{F2} = 16 mA V _{O1} = V _{O2} = Open V _{CC} = 15 V	—	160	—	μA
Logic high supply current		I _{CCH}	I _{F1} = I _{F2} = 0 mA V _{O1} = V _{O2} = Open V _{CC} = 15 V	—	0.05	4	μA
Current transfer ratio (each channel)	TLP2530	I _O / I _F	I _F = 16 mA, V _O = 0.4 V V _{CC} = 4.5 V, Ta = 25 °C	7	30	—	%
	TLP2531			19	30	—	
	TLP2530	I _O / I _F	I _F = 16 mA, V _O = 0.4 V V _{CC} = 4.5 V	5	—	—	%
	TLP2531			15	—	—	
Logic low output voltage (each channel)	TLP2530	V _{OL}	I _F = 16 mA, I _O = 1.1 mA V _{CC} = 4.5 V	—	0.1	0.4	V
	TLP2531			I _F = 16 mA, I _O = 2.4 mA V _{CC} = 4.5 V	—	0.1	0.4
Resistance (input-output)		R _S	V _S = 500 V R.H. ≤ 60 % (Note 1)	5×10 ¹⁰	10 ¹⁴	—	Ω
Capacitance (input-output)		C _S	f = 1 MHz (Note 1)	—	0.6	—	pF
Resistance (input-input)		R _{I-I}	V _{I-I} = 500 V (Note 1)	—	10 ¹¹	—	Ω
Capacitance (input-input)		C _{I-I}	f = 1 MHz (Note 1)	—	0.25	—	pF

Note: All typicals at Ta = 25 °C.

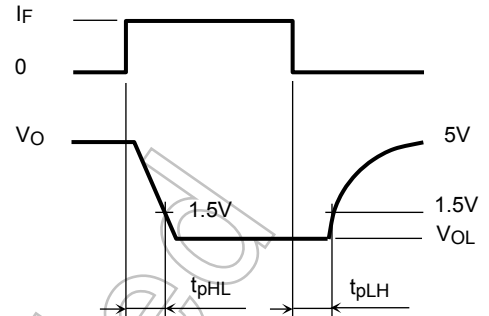
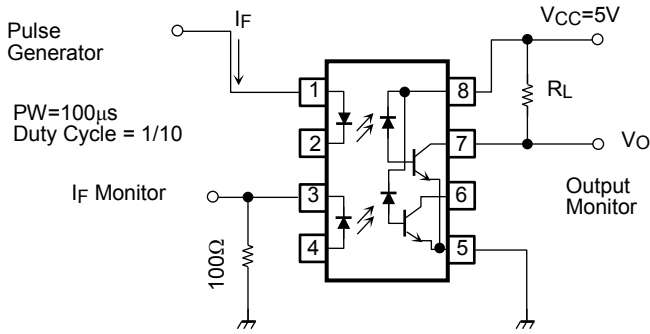
Note 1: Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

Switching Characteristics (unless otherwise specified, $T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$, $I_F = 16\text{mA}$)

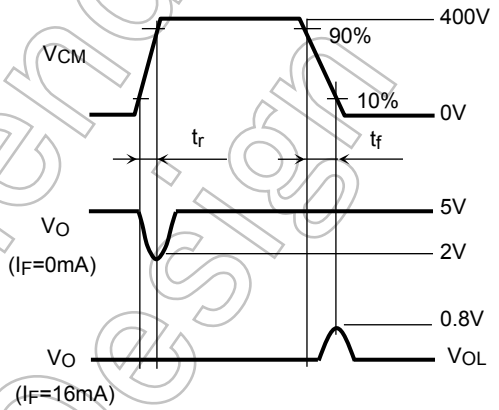
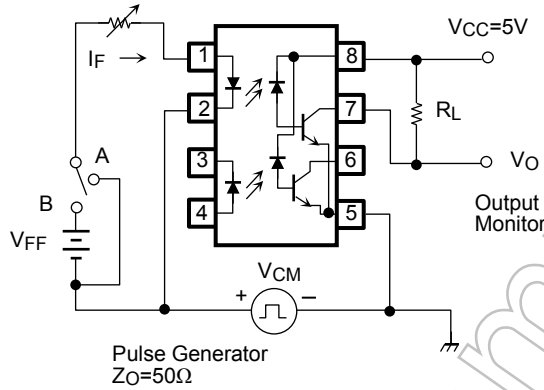
Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to logic low at output (each channel)	TLP2530	t_{pHL}	1	$R_L = 4.1\text{ k}\Omega$	—	0.3	1.5	μs
	TLP2531			$R_L = 1.9\text{ k}\Omega$	—	0.2	0.8	
Propagation delay time to logic high at output (each channel)	TLP2530	t_{pLH}	1	$R_L = 4.1\text{ k}\Omega$	—	0.5	1.5	μs
	TLP2531			$R_L = 1.9\text{ k}\Omega$	—	0.3	0.8	
Common mode transient immunity at logic high level output (each channel) (Note 1)	TLP2530	CM_H	2	$V_{CM} = 400\text{ V}_{p-p}$ $R_L = 4.1\text{ k}\Omega$, $I_F = 0\text{ mA}$	—	1500	—	$\text{V} / \mu\text{s}$
	TLP2531			$V_{CM} = 400\text{ V}_{p-p}$ $R_L = 1.9\text{ k}\Omega$, $I_F = 0\text{ mA}$	—	1500	—	
Common mode transient immunity at logic low level output (each channel) (Note 1)	TLP2530	CM_L	2	$V_{CM} = 400\text{ V}_{p-p}$ $R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$	—	-1500	—	$\text{V} / \mu\text{s}$
	TLP2531			$V_{CM} = 400\text{ V}_{p-p}$ $R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$	—	-1500	—	
Bandwidth (each channel)		BW	3	$R_L = 100\ \Omega$	—	2	—	MHz

Note 1: Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{CM} / dt on the leading edge of the common mode pulse, V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0\text{ V}$).
Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{CM} / dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in logic low state (i.e., $V_O < 0.8\text{ V}$).

Test Circuit 1: Switching Time, t_{pHL} , t_{pLH}

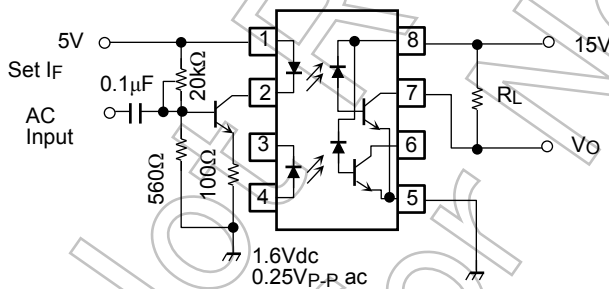


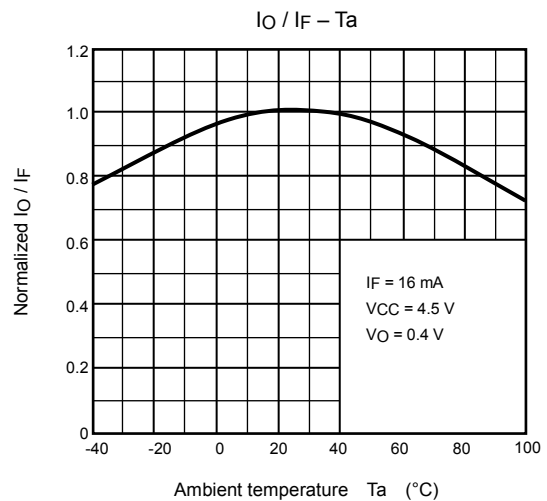
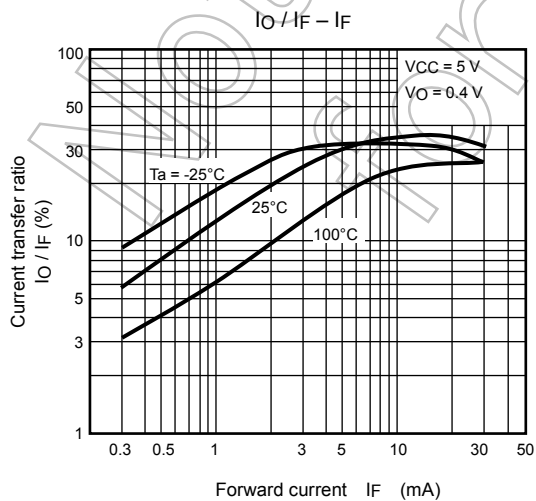
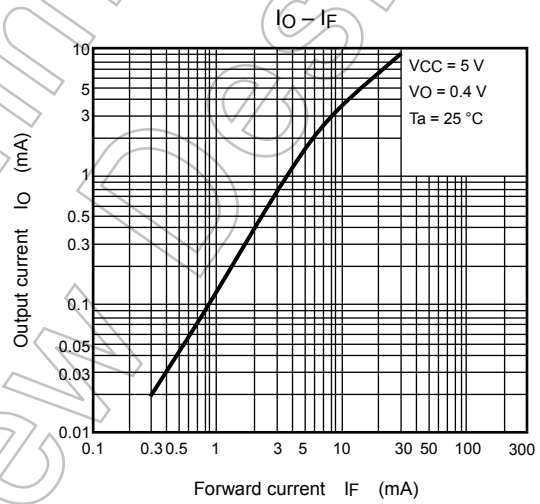
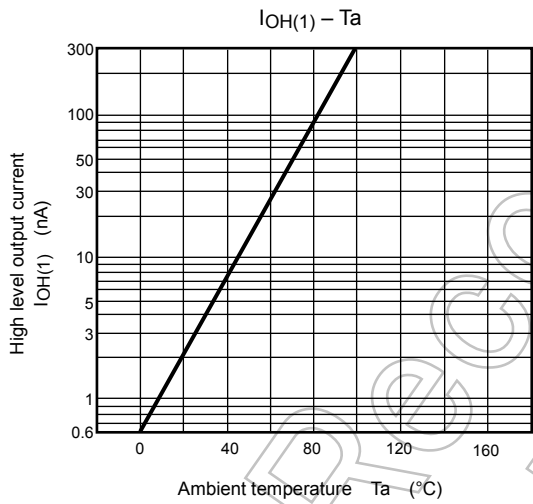
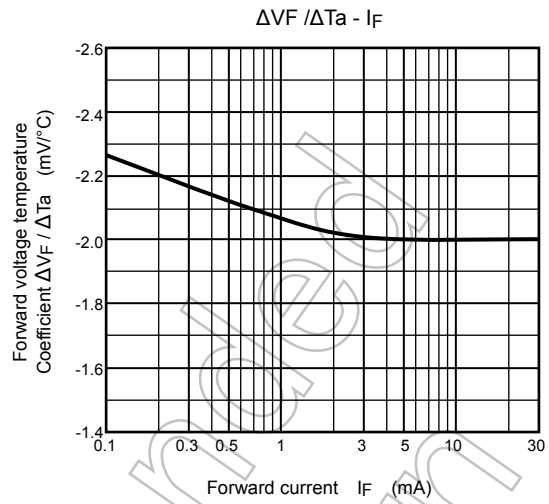
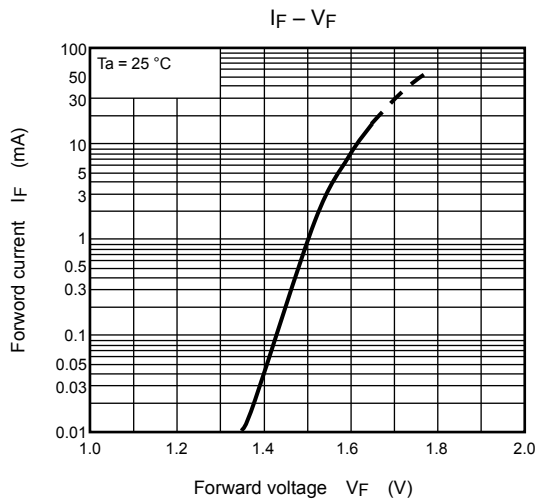
Test Circuit 2: Common mode transient Immunity and Typical Waveform



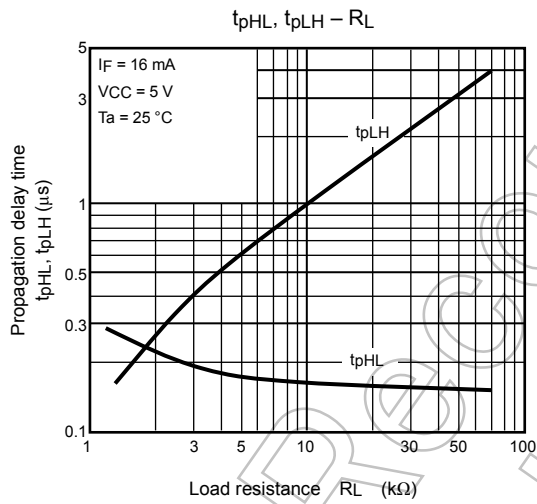
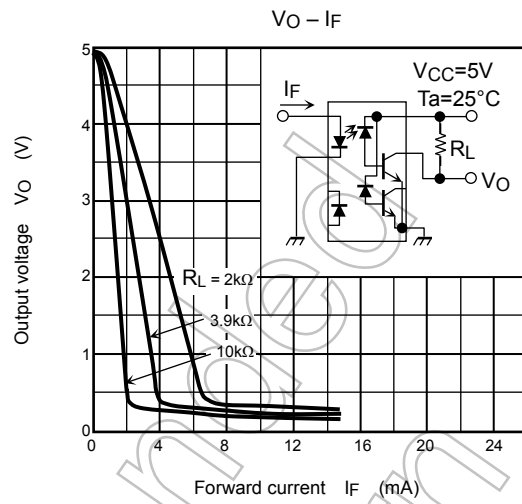
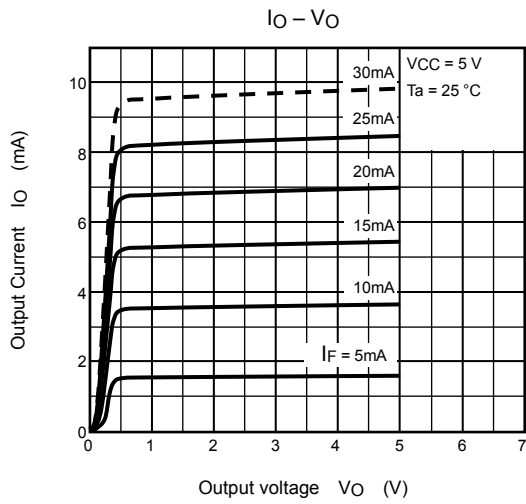
$$CM_H = \frac{320(V)}{t_r(\mu s)}, CM_L = \frac{320(V)}{t_f(\mu s)}$$

Test Circuit 3: Frequency Response





NOTE: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



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