Document Number: MC33888
Rev. 6.0, 2/2007

Quad High-Side and Octal Low-Side Switch for Automotive

33888
33888A

HIGH-SIDE/LOW-SIDE SWITCH

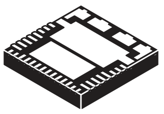
ADVANCE INFORMATION*

The 33888 is a single-package combination of a power die with four discrete high-side MOSFETs (two 10 mΩ and two 40 mΩ) and an integrated IC control die consisting of eight low-side drivers (600 mΩ each) with appropriate control, protection, and diagnostic features.

Programming, control, and diagnostics are accomplished using a 16-bit SPI interface. Additionally, each high-side output has its own parallel input for pulse-width modulation (PWM) control if desired. The low sides share a single configurable direct input.

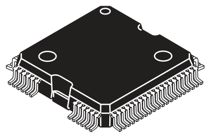
Features

- Dual 10 mΩ High Side, Dual 40 mΩ High Side, Octal 600 mΩ Low Side
- Full Operating Voltage of 6.0 V to 27 V
- SPI Control of High-Side Overcurrent Limit, High-Side Current Sense, Output OFF Open Load Detection, Output ON/OFF Control, Watchdog Timeout
- SPI Reporting of Program Status and Fault
- High-Side Analog Current Feedback with Selectable Ratio
- Enhanced 16 V Reverse Polarity V_{PWR} Protection



Bottom View

PNB SUFFIX
98ARL10544D
36-PIN PQFN



Top View

FB SUFFIX
98ARH99043A
64-PIN PQFP

ORDERING INFORMATION

Device	Temperature Range (T_A)	Package
MC33888APNB/R2	-40°C to 125°C	36 PQFN
MC33888FB/R2		64 PQFP

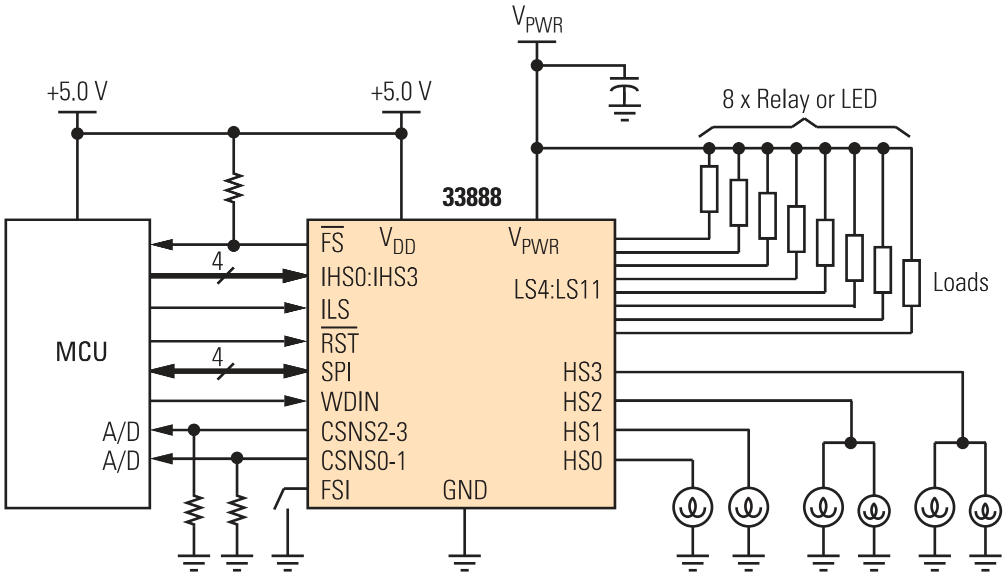


Figure 1. 33888 Simplified Application Diagram

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* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

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DEVICE VARIATIONS

Table 1. Features Comparison: 33888 and 33888A

Parameter	Symbol	Condition	33888	33888A	For details, see page
Undervoltage Low-Side Output Shutdown	V_{PWRUV}	–	5.0 V	3.0 V	10
Low-Side Drain-to-Source ON Resistance	$R_{DS(ON)}$	V_{PWR} = 4.5 V; V_{DD} = 3.5 V	Not specified	8.0 Ω	13
Recommended Frequency of SPI Operation	f_{SPI}	Extended Mode, V_{DD} = 3.4 V	Not specified	2.1 MHz (max)	16

INTERNAL BLOCK DIAGRAM

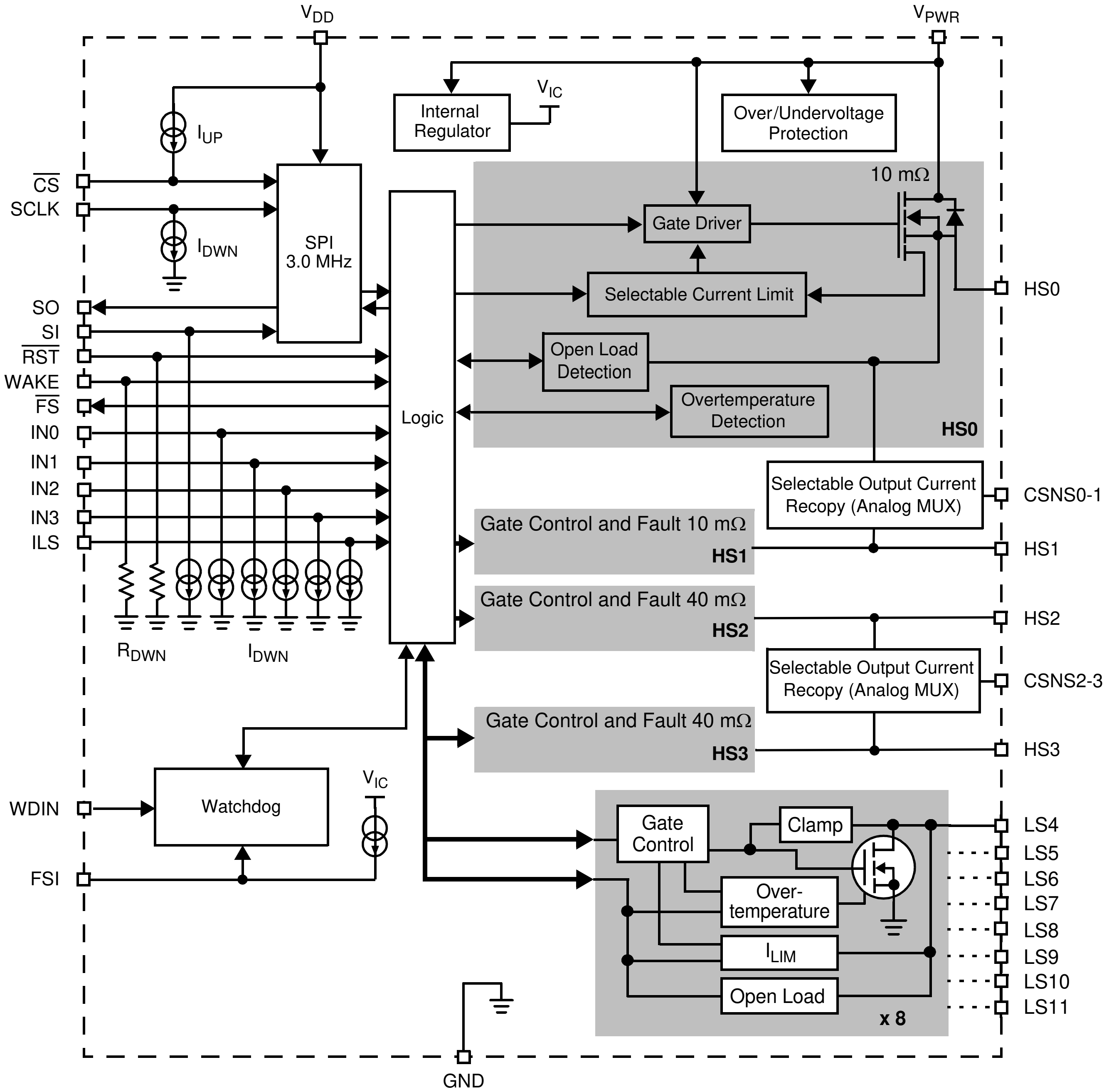

VDD
VPWR
VIC
Internal Regulator
Over/Undervoltage Protection
IUP
CS
SCLK
SPI 3.0 MHz
IDWN
10 mΩ
Gate Driver
Selectable Current Limit
HS0
SO
SI
RST
WAKE
FS
IN0
IN1
IN2
IN3
ILS
Logic
Open Load Detection
Overtemperature Detection
HS0
Selectable Output Current Recopy (Analog MUX)
CSNS0-1
Gate Control and Fault 10 mΩ
HS1
HS1
RDWN
IDWN
Gate Control and Fault 40 mΩ
HS2
HS2
Selectable Output Current Recopy (Analog MUX)
CSNS2-3
Gate Control and Fault 40 mΩ
HS3
HS3
Watchdog
VIC
WDIN
FSI
Gate Control
Clamp
Over-temperature
ILIM
Open Load
x 8
LS4
LS5
LS6
LS7
LS8
LS9
LS10
LS11
GND

Figure 2. 33888 Simplified Internal Block Diagram

PIN CONNECTIONS

Transparent Top View of Package

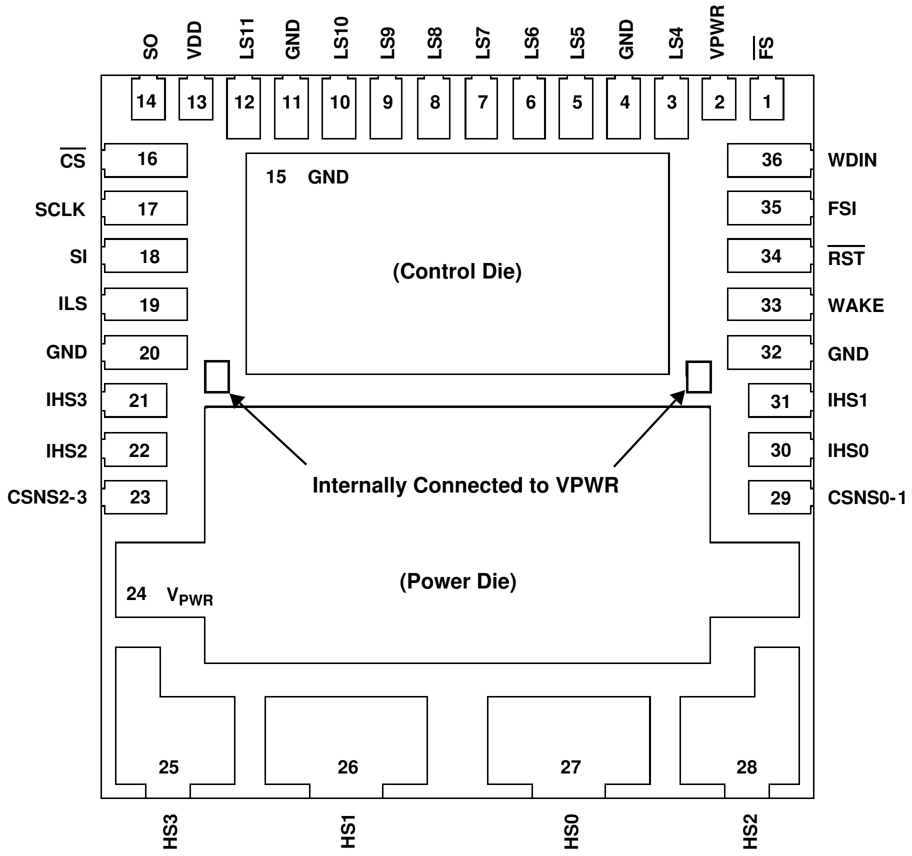

SO
VDD
LS11
GND
LS10
LS9
LS8
LS7
LS6
LS5
GND
LS4
VPWR
FS
14
13
12
11
10
9
8
7
6
5
4
3
2
1
CS
SCLK
SI
ILS
GND
IHS3
IHS2
CSNS2-3
16
17
18
19
20
21
22
23
15 GND
(Control Die)
Internally Connected to VPWR
(Power Die)
24 VPWR
36
35
34
33
32
31
30
29
WDIN
FSI
RST
WAKE
GND
IHS1
IHS0
CSNS0-1
25
26
27
28
HS3
HS1
HS0
HS2

Figure 3. 33888 Pin Connections for PQFN

Table 2. 33888 Pin Definitions for PQFN

A functional description of each pin can be found in the Functional Pin Description section beginning on page 18.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	FS	Output	Fault Status (Active Low)	This output pin is an open drain indication that goes active low when a fault mode is detected by the device.
2, 24	VPWR	Input	Positive Power Supply	These pin connects to the positive power supply and are the source input of operational power for the device. Pins 2 and 24 must be shorted together on the board.
3 6 8 10	LS4 LS6 LS8 LS10	Output	Low-Side Output 4 Low-Side Output 6 Low-Side Output 8 Low-Side Output 10	These outputs are current and thermal overload protected. Maximum steady state current through each of these outputs is 500 mA.
4, 11, 15, 20, 32	GND	Ground	Power Ground	These pins serve as the ground for the source of the low-side output transistors as well as the logic portion of the device. Pins 4, 11, 15, 20, and 32 must be shorted together on the board
5 7 9 12	LS5 LS7 LS9 LS11	Output	Low-Side Output 5 Low-Side Output 7 Low-Side Output 9 Low-Side Output 11	These outputs are current and thermal overload protected. Maximum steady state current through each of these outputs is 800 mA.

Table 2. 33888 Pin Definitions for PQFN (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 18.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
13	VDD	Input	Digital Drain Voltage (Power)	This is an external input pin used to supply power to the SPI circuit.
14	SO	Output	Serial Output	This is an output pin connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device in a daisy chain.
16	CS	Input	Chip Select (Active Low)	This is an input pin connected to a chip select output of a microcontroller (MCU).
17	SCLK	Input	Serial Clock	This input pin is connected to the SCLK pin of the master MCU, which is a bit (shift) clock for the SPI port.
18	SI	Input	Serial Input	This input pin is connected to the SPI Serial Data Output pin of the MCU from which it receives output command data.
19	ILS	Input	Low-Side Input	This input pin is used to directly control a number of the low-side devices as configured by SPI.
21 22 30 31	IHS3 IHS2 IHS0 IHS1	Input	High-Side Input 3 High-Side Input 2 High-Side Input 0 High-Side Input 1	These inputs may or may not be activated depending on the configured state of the internal logic.
23 29	CSNS2-3 CSNS0-1	Output	Current Sense 2-3 Current Sense 0-1	These pins deliver a metered amount of the high-side output current that can be used to generate signal ground referenced output voltages for use by the MCU.
25 28	HS3 HS2	Output	High-Side Output 3 High-Side Output 2	Each pin is the source of a 40 mΩ MOSFET high-side driver, which delivers current through the connected loads.
26 27	HS1 HS0	Output	High-Side Output 1 High-Side Output 0	Each pin is the source of a 10 mΩ MOSFET high-side driver, which delivers current through the connected loads.
33	WAKE	Input	Wake	This pin is used to input a logic [1] signal in order to enable the watchdog timer function.
34	RST	Input	Reset (Active Low)	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low current standby mode.
35	FSI	Input	Fail-Safe Input	The Fail-Safe input pin level determines the state of the outputs after a watchdog timeout occurs. This pin has an internal pullup.
36	WDIN	Input	Watchdog Input	This input pin is a CMOS logic level input that is used to monitor system operation.

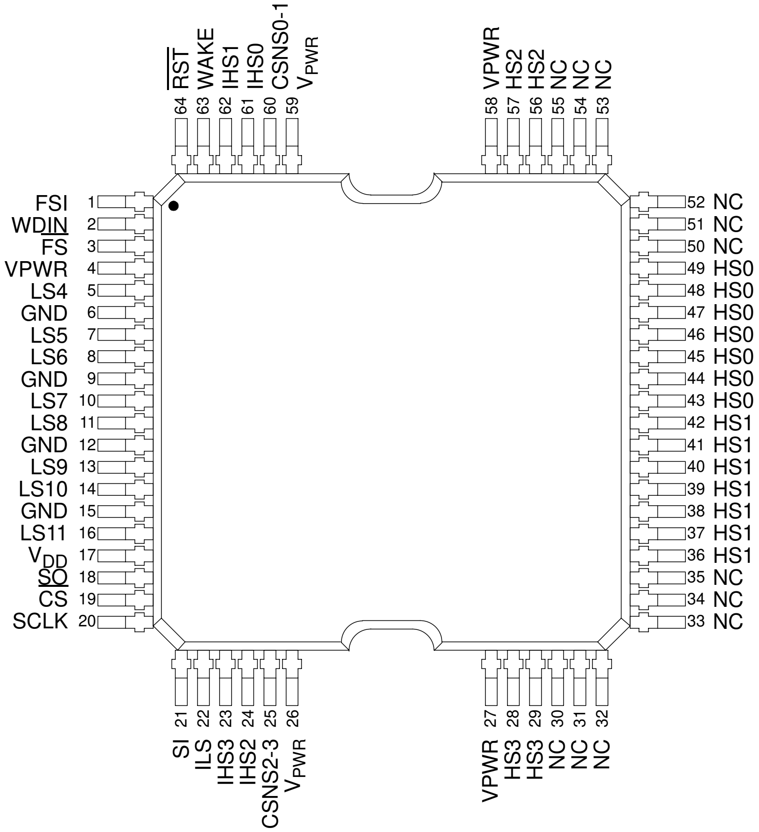

64 RST
63 WAKE
62 IHS1
61 IHS0
60 CSNS0-1
59 V_{PWR}
58 VPWR
57 HS2
56 HS2
55 NC
54 NC
53 NC
FSI 1
WDIN 2
FS 3
VPWR 4
LS4 5
GND 6
LS5 7
LS6 8
GND 9
LS7 10
LS8 11
GND 12
LS9 13
LS10 14
GND 15
LS11 16
V_{DD} 17
SO 18
CS 19
SCLK 20
52 NC
51 NC
50 NC
49 HS0
48 HS0
47 HS0
46 HS0
45 HS0
44 HS0
43 HS0
42 HS1
41 HS1
40 HS1
39 HS1
38 HS1
37 HS1
36 HS1
35 NC
34 NC
33 NC
21 SI
22 ILS
23 IHS3
24 IHS2
25 CSNS2-3
26 V_{PWR}
27 VPWR
28 HS3
29 HS3
30 NC
31 NC
32 NC

Figure 4. 33888 Pin Connections for PQFP

Table 3. 33888 Pin Definitions for PQFP

A functional description of each pin can be found in the Functional Pin Description section beginning on page 18.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
1	FSI	Input	Fail-Safe Input	The Fail-Safe input pin level determines the state of the outputs after a watchdog timeout occurs. This pin has an internal pullup.
2	WDIN	Input	Watchdog Input	This input pin is a CMOS logic level input that is used to monitor system operation.
3	FS	Output	Fault Status (Active Low)	This output pin is an open drain indication that goes active low when a fault mode is detected by the device.
4, 26, 27, 58, 59	VPWR	Input	Positive Power Supply	These pin connects to the positive power supply and are the source input of operational power for the device. Pins 4, 26, 27, 58 and 59 must be shorted together on the board.
5 8 11 14	LS4 LS6 LS8 LS10	Output	Low-Side Output 4 Low-Side Output 6 Low-Side Output 8 Low-Side Output 10	These outputs are current and thermal overload protected. Maximum steady state current through each of these outputs is 500 mA.
6, 9, 12, 15	GND	Ground	Power Ground	These pins serve as the ground for the source of the low-side output transistors as well as the logic portion of the device. Pins 6, 9, 12 and 15 must be shorted together on the board.

Table 3. 33888 Pin Definitions for PQFP (continued)

A functional description of each pin can be found in the Functional Pin Description section beginning on page 18.

Pin Number	Pin Name	Pin Function	Formal Name	Definition
7 10 13 16	LS5 LS7 LS9 LS11	Output	Low-Side Output 5 Low-Side Output 7 Low-Side Output 9 Low-Side Output 11	These outputs are current and thermal overload protected. Maximum steady state current through each of these outputs is 800 mA.
17	VDD	Input	Digital Drain Voltage (Power)	This is an external input pin used to supply power to the SPI circuit.
18	SO	Output	Serial Output	This is an output pin connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device in a daisy chain.
19	CS	Input	Chip Select (Active Low)	This is an input pin connected to a chip select output of a microcontroller (MCU).
20	SCLK	Input	Serial Clock	This input pin is connected to the SCLK pin of the master MCU, which is a bit (shift) clock for the SPI port.
21	SI	Input	Serial Input	This input pin is connected to the SPI Serial Data Output pin of the MCU from which it receives output command data.
22	ILS	Input	Low-Side Input	This input pin is used to directly control a number of the low-side devices as configured by SPI.
23 24 61 62	IHS3 IHS2 IHS0 IHS1	Input	High-Side Input 3 High-Side Input 2 High-Side Input 0 High-Side Input 1	Each high-side input pin is used to directly control only one designated high-side output.
25 60	CSNS2-3 CSNS0-1	Output	Current Sense 2-3 Current Sense 0-1	These pins deliver a metered amount of the high-side output current that can be used to generate signal ground referenced output voltages for use by the MCU.
28, 29 56, 57	HS3 HS2	Output	High-Side Output 3 High-Side Output 2	Each pin is the source of a 40 mΩ MOSFET high-side driver, which delivers current through the connected loads.
30–35, 50–55	NC	N/A	Not Connected	These pins are not connected internally.
36–42 43–49	HS1 HS0	Output	High-Side Output 1 High-Side Output 0	Each pin is the source of a 10 mΩ MOSFET high-side driver, which delivers current through the connected loads.
63	WAKE	Input	Wake	This pin is used to input a logic [1] signal in order to enable the watchdog timer function.
64	RST	Input	Reset (Active Low)	This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low current standby mode.

ELECTRICAL CONNECTIONS

MAXIMUM RATINGS

Table 4. Maximum Ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
ELECTRICAL RATINGS			
Power Supply Voltage Steady State	V_{PWR}	 -16 to 41	V
Input Pin Voltage (1)	V_{IN}	-0.3 to 7.0	V
WAKE Input Pin Clamp Current	I_{WICI}	2.5	mA
Continuous per Output Current (2) Low-Sides 4, 6, 8, 10 Low-Sides 5, 7, 9, 11	I_{OUTLS}	 500 800	mA
Continuous per Output Current (3) High-Sides 0, 1 High-Sides 2, 3	I_{OUTHS}	 10 5.0	A
Output Clamp Energy High-Sides 0, 1 (4) High-Sides 2, 3 (5) Low-Sides (6)	 E_{HS} E_{HS} E_{LS}	 450 120 50	mJ
ESD Voltage (7) Human Body Model Machine Model	 V_{ESD1} V_{ESD2}	 ±2000 ±200	V

Notes

1. Exceeding voltage limits on SCLK, SI, $\overline{\text{CS}}$, WDIN, $\overline{\text{RST}}$, IHS, FSI, or ILS pins may cause a malfunction or permanent damage to the device.
2. Continuous low-side output current rating so long as maximum junction temperature is not exceeded. Operation at 125°C ambient temperature will require calculation of maximum output current using package thermal resistance.
3. Continuous high-side output current rating so long as maximum junction temperature is not exceeded. Operation at 125°C ambient temperature will require calculation of maximum output current using package thermal resistance.
4. Active HS0 and HS1 clamp energy using the following conditions: single nonrepetitive pulse, $V_{PWR} = 16.0$ V, L = 40 mH, $T_J = 150°C$.
5. Active HS2 and HS3 clamp energy using the following conditions: single nonrepetitive pulse, $V_{PWR} = 16.0$ V, L = 10 mH, $T_J = 150°C$.
6. Active low-side clamp energy using the following conditions: single nonrepetitive pulse, 450 mA, $T_J = 150°C$.
7. ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP} = 100$ pF, $R_{ZAP} = 1500\ \Omega$), ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP} = 200$ pF, $R_{ZAP} = 0\ \Omega$).

Table 4. Maximum Ratings (continued)

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Ratings	Symbol	Value	Unit
THERMAL RATINGS			
Operating Temperature			°C
Ambient	T_A	-40 to 125	
Junction	T_J	-40 to 150	
Storage Temperature	T_{STG}	-55 to 150	°C
Control Die Thermal Resistance (8)	$R_{\theta CJC}$		°C/W
PQFP			
One Low-Side ON		12.5	
Two Low-Side ON		9.3	
Three Low-Side ON		7.3	
Four Low Side ON		5.9	
All Low-Sides ON		3.2	
PQFN			
One Low-Side ON		8.6	
Two Low-Side ON		6.0	
Three Low-Side ON		4.6	
Four Low Side ON		3.8	
All Low-Sides ON		2.0	
Power Die Thermal Resistance (8)	$R_{\theta PJC}$		°C/W
PQFP			
One High-Side 2, 3 ON		0.5	
All High-Sides ON		0.15	
PQFN			
One High-Side 2, 3 ON		0.5	
All High-Sides ON		0.1	
Thermal Resistance, Junction to Ambient, Natural Convection, Four-Layer Board (8)	$R_{\theta JA}$		°C/W
PQFP		33	
PQFN		37	
Peak Package Reflow Temperature During Reflow (9), (10)	T_{PPRT}	Note 10	°C

Notes

8. Board dimensions are 8.0 cm x 8.0 cm x 1.5 mm with a 300 mm^2 copper area on the bottom layer.
9. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
10. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL),
    > Go to www.freescale.com
    > Search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx)]
    > Locate your Part Number and in the Details column, select "View"
    > Select "Environmental and Compliance Information"

STATIC ELECTRICAL CHARACTERISTICS

Table 5. Static Electrical Characteristics

Characteristics noted under conditions 6.0 V $\leq V_{PWR} \leq$ 27 V, 4.5 V $\leq V_{DD} \leq$ 5.5 V, -40°C $\leq T_J \leq$ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT					
Supply Voltage Range	V_{PWR}				V
Fully Operational		6.0	–	27	
V_{PWR} Supply Current	$I_{PWR(ON)}$				mA
$T_J > 125°C$		–	17	25	
$T_J \leq 125°C$		–	–	20	
V_{PWR} Standby Current (All Outputs OFF, Open Load Detection Disabled, WAKE = H, $\overline{\text{RST}}$ = H)	$I_{PWR(SBY)}$				mA
$T_J > 125°C$		–	4.2	7.0	
$T_J \leq 125°C$		–	2.9	5.0	
Sleep State Supply Current (V_{PWR} < 12.6 V, $\overline{\text{RST}}$ < 0.5 V, WAKE < 0.5 V, HS[0:3] = 0 V) (11)	$I_{PWR(SS)}$				µA
$T_J = 85°C$		–	–	80	
$T_J = 25°C$		–	1.0	25	
Logic Supply Voltage Range	V_{DD}	4.5	5.0	5.5	V
Logic Supply Current	$I_{DD(ON)}$				mA
$T_J > 125°C$		–	4.2	7.0	
$T_J \leq 125°C$		–	2.9	5.0	
Logic Supply Sleep State Current	$I_{DD(SS)}$	–	–	5.0	µA
Sleep State Low-Side Output Leakage Current (per Low-Side Output, $\overline{\text{RST}}$ = LOW)	$I_{SLK(SS)}$				µA
$T_J = 85°C$		–	–	3.0	
$T_J = 25°C$		–	–	1.0	
Overvoltage Shutdown Threshold	V_{PWROV}	28.5	32	36	V
Overvoltage Shutdown Hysteresis	$V_{PWROV(HYS)}$	0.2	0.6	1.5	V
Undervoltage High-Side Output Shutdown (12)	V_{PWRUV}	5.0	5.6	6.0	V
Undervoltage Low-Side Output Shutdown	V_{PWRUV}				V
APNB Suffix Only (12)		3.0	4.0	4.4	
PNB and FB Suffixes		5.0	5.6	6.0	
Undervoltage High-Side Shutdown Hysteresis	$V_{PWRUV(HYS)}$	0.1	0.3	0.5	V

Notes

11. This parameter is tested at 125°C with a maximum value of 10 µA.
12. SPI/IO and internal logic operational. Outputs will recover in instructed state when V_{PWR} voltage level returns to normal as long as the level does not go below V_{PWRUV}.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 27 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER INPUT (continued)					
Current Sense Ratio (9.0 V ≤ V_{PWR} ≤ 16 V, CSNS ≤ 4.5 V) CSNS0-1/HS0, CSNS0-1/HS1	$C_{SR[0:1]}$	–	1/1400	–	–
Current Sense Ratio ($C_{SR[0:1]}$) Accuracy HS[0:1] Output Current 1.0 A 2.0 A 5.0 A 6.5 A 10 A	$C_{SR[0:1]\_ACC}$	 -35 -19 -14 -12 -12	 – – – – –	 35 19 14 12 12	%
Current Sense Ratio (V_{PWR} = 9.0 V – 16 V, CSNS < 4.5 V) CSNS2-3/HS2, CSNS2-3/HS3	C_{SR}	–	1/880	–	–
Current Sense Ratio ($C_{SR[2:3]}$) Accuracy HS[2:3] Output Current 0.5 A 1.0 A 3.0 A 3.7 A 5.0 A	$C_{SR[2:3]\_ACC}$	 -30 -19 -13.5 -12 -9.0	 – – – – –	 30 19 13.5 12 9.0	%
Current Sense Clamp Voltage I_{CNS} = 15 mA Generated by the Device	V_{SENSE}	4.5	6.0	7.0	V
HS0 AND HS1 POWER OUTPUTS					
Drain-to-Source ON Resistance (I_{OUT} = 5.5 A) T_J = 25°C V_{PWR} = 6.0 V V_{PWR} = 9.0 V V_{PWR} = 13 V T_J = 150°C V_{PWR} = 6.0 V V_{PWR} = 9.0 V V_{PWR} = 13 V	$R_{DS(ON)}$	 – – – – – –	 – – – – – –	 0.02 0.01 0.01 0.034 0.017 0.017	Ω
Reverse Battery Source-to-Drain ON Resistance (I_{OUT} = -5.5 A, T_J = 25°C) V_{PWR} = -12 V	$R_{DS(ON)REV}$	–	–	0.02	Ω
Output Self-Limiting Peak Current Outputs ON, V_{OUT} = V_{PWR}-2.0 V	$I_{LIM(PK)}$	33	49	66	A
Output Self-Limiting Sustain Current Outputs ON, V_{OUT} = V_{PWR}-2.0 V	$I_{LIM(SUS)}$	13	25	34	A
Open Load Detection Current (13)	I_{OLDC}	30	–	100	µA

Notes

13. Output OFF Open Load Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 27 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
HS0 AND HS1 POWER OUTPUTS (continued)					
Output Fault Detection Threshold [14]	$V_{OFD(THRES)}$				V
Output Programmed OFF		2.0	3.0	4.0	
Output Negative Clamp Voltage	V_{CL}				V
0.5 A ≤ I_{OUT} ≤ 2.0 A, Output OFF		-20	–	–	
Overtemperature Shutdown (Outputs OFF) [15]	T_{SD}	160	175	190	°C
Overtemperature Shutdown Hysteresis [15]	$T_{SD(HYS)}$	10	–	30	°C
HS2 AND HS3 POWER OUTPUTS					
Drain-to-Source ON Resistance (I_{OUT} = 4.5 A)	$R_{DS(ON)}$				Ω
T_J = 25°C					
V_{PWR} = 6.0 V		–	–	0.08	
V_{PWR} = 9.0 V		–	–	0.04	
V_{PWR} = 13 V		–	–	0.04	
T_J = 150°C					
V_{PWR} = 6.0 V		–	–	0.136	
V_{PWR} = 9.0 V		–	–	0.068	
V_{PWR} = 13 V		–	–	0.068	
Reverse Battery Source-to-Drain ON Resistance (I_{OUT} = 4.5 A, T_J = 25°C)	$R_{DS(ON)REV}$				Ω
V_{PWR} = -12 V		–	–	0.08	
Output Self-Limiting Peak Current	$I_{LIM(PK)}$				A
Outputs ON, V_{OUT} = V_{PWR} -2.0 V		15	23	35	
Output Self-Limiting Sustain Current	$I_{LIM(SUS)}$				A
Outputs ON, V_{OUT} = V_{PWR} -2.0 V		6.0	10	15	
Open Load Detection Current [16]	I_{OLDC}	25	–	100	μA
Output Fault Detection Threshold [17]	$V_{OFD(THRES)}$				V
Outputs Programmed OFF		2.0	3.0	4.0	
Output Negative Clamp Voltage	V_{CL}				V
0.5 A ≤ I_{OUT} ≤ 2.0 A, Outputs OFF		-20	–	–	
Overtemperature Shutdown (Outputs OFF) [18]	T_{SD}	160	170	190	°C
Overtemperature Shutdown Hysteresis [18]	$T_{SD(HYS)}$	10	–	30	°C

Notes

14. Output fault detection threshold with outputs programmed OFF. For the Low-Side Outputs, fault detection thresholds are the same for output open and battery shorts.
15. Guaranteed by design. Not production tested.
16. Output OFF Open Load Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.
17. Output fault detection threshold with outputs programmed OFF.
18. Guaranteed by design. Not production tested.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions $6.0\ V \le V_{PWR} \le 27\ V$, $4.5\ V \le V_{DD} \le 5.5\ V$, $-40°C \le T_J \le 150°C$ unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A = 25°C$ under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LOW-SIDE POWER OUTPUTS					
Drain-to-Source ON Resistance (I_{OUT} = 0.3 A)	$R_{DS(ON)}$				Ω
T_J = 25°C					
V_{PWR} = 4.5 V; V_{DD} = 3.5 V, 33888A Only		–	–	8.0	
V_{PWR} = 6.0 V		–	–	1.0	
V_{PWR} = 9.0 V		–	–	0.7	
V_{PWR} = 13 V		–	–	0.6	
T_J = 150°C					
V_{PWR} = 4.5 V; V_{DD} = 3.5 V, 33888A Only		–	–	8.0	
V_{PWR} = 6.0 V		–	–	1.8	
V_{PWR} = 9.0 V		–	–	1.1	
V_{PWR} = 13 V		–	–	0.9	
Output Self-Limiting Current (Outputs Programmed ON, V_{OUT} = 3.0 V)	I_{LIM}				A
Low-Side 4, 6, 8, 10		0.5	0.9	1.5	
Low-Side 5, 7, 9, 11		0.8	1.3	2.0	
Output OFF Open Load Detection Current [19]	I_{OLDC}				µA
Output Programmed OFF, V_{OUT} = 3.0 V		25	50	100	
Output Fault Detection Threshold [20]	$V_{OFD(THRES)}$				V
Output Programmed OFF		2.0	3.0	4.0	
Output Clamp Voltage	V_{CL}				V
2.0 mA ≤ I_{OUT} ≤ 200 mA, Outputs OFF		41	53	60	
Low-Side Body Diode Voltage (I = -300 mA, T_J = 125°C)	V_{BD}	0.5	0.7	0.9	V
Overtemperature Shutdown (Outputs OFF) [21]	T_{LIM}	160	170	190	°C
Overtemperature Shutdown Hysteresis [21]	$T_{LIM(HYS)}$	10	20	30	°C

Notes

19. Output OFF Open Load Detection Current is the current required to flow through the load for the purpose of detecting the existence of an open load condition when the specific output is commanded OFF.
20. Output fault detection threshold with outputs programmed OFF. For the low-side outputs, fault detection thresholds are the same for output open and battery shorts.
21. Guaranteed by design. Not production tested.

Table 5. Static Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V $\leq V_{PWR} \leq$ 27 V, 4.5 V $\leq V_{DD} \leq$ 5.5 V, -40°C $\leq T_J \leq$ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
CONTROL INTERFACE					
Input Logic High Voltage (22)	V_{IH}	0.7 V_{DD}	–	–	V
Input Logic Low Voltage (22)	V_{IL}	–	–	1.0	V
Input Logic Voltage Hysteresis (SI, $\overline{CS}$, SCLK, IHS[0:3], ILS) (23)	$V_{IN(HYS)}$	100	350	750	mV
Input Logic Pulldown Current (SI, SCLK, IHS[0:3], ILS, WDIN)	I_{DWN}	5.0	–	20	µA
Input Logic Pulldown Resistor (WAKE, $\overline{RST}$)	R_{DWN}	100	200	400	kΩ
Input Logic Pullup Current ($\overline{CS}$, V_{IN} = 0.7 V_{DD}) (24)	I_{UPC}	5.0	–	20	µA
Input Logic Pullup Current (FSI, V_{IN} = 3.5 V)	I_{UPF}	5.0	–	20	µA
Wake Input Clamp Voltage (I_{WICI} < 2.5 mA) (25)	V_{WIC}	7.0	–	14	V
Wake Input Forward Voltage (I_{WICI} = -2.5 mA)	V_{WIF}	-2.0	–	-0.3	V
SO High-State Output Voltage (I_{OH} = 1.0 mA)	V_{SOH}	0.8 V_{DD}	–	–	V
$\overline{FS}$, SO Low-State Output Voltage (I_{OL} = -1.6 mA)	V_{SOL}	–	0.2	0.4	V
SO Tri-State Leakage Current ($\overline{CS} \geq$ 3.5 V)	I_{SOLK}	-5.0	0	5.0	µA
Input Capacitance (26)	C_{IN}	–	4.0	12	pF
SO, $\overline{FS}$ Tri-State Capacitance (23)	C_{SO}	–	–	20	pF

Notes

22. Upper and lower logic threshold voltage range applies to SI, $\overline{CS}$, SCLK, $\overline{RST}$, IHS[0:3], ILS, WAKE, and WDIN input signals. The WAKE, FSI, and $\overline{RST}$ signals are derived from an internal supply.
23. Parameter is guaranteed by design but is not production tested.
24. $\overline{CS}$ is pulled up to V_{DD}.
25. The current must be limited by a series resistor when using voltages higher than the W_{ICV}.
26. Input capacitance of SI, $\overline{CS}$, SCLK, $\overline{RST}$, IHS[0:3], ILS, WAKE, and WDIN. This parameter is guaranteed by process monitoring but is not production tested.

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 6. Dynamic Electrical Characteristics

Characteristics noted under conditions 6.0 V ≤ V_{PWR} ≤ 27 V, 4.5 V ≤ V_{DD} ≤ 5.5 V, -40°C ≤ T_J ≤ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING					
High-Side Output Rising Fast Slew Rate (27) 6.0 V < V_{PWR} < 9.0 V 9.0 V < V_{PWR} < 16 V 16 V < V_{PWR} < 27 V	SR_{R_FAST}	 0.03 0.05 0.1	 – 0.5 –	 0.6 0.8 1.1	V/µs
High-Side Output Rising Slow Slew Rate (28) 6.0 V < V_{PWR} < 9.0 V 9.0 V < V_{PWR} < 16 V 16 V < V_{PWR} < 27 V	SR_{R_SLOW}	 0.01 0.01 0.01	 – 0.08 –	 0.14 0.18 0.2	V/µs
High-Side Output Falling Fast Slew Rate (27) 6.0 V < V_{PWR} < 9.0 V 9.0 V < V_{PWR} < 16 V 16 V < V_{PWR} < 27 V	SR_{F_FAST}	 0.2 0.3 0.5	 – 0.8 –	 1.0 1.5 2.2	V/µs
High-Side Output Falling Slow Slew Rate (28) 6.0 V < V_{PWR} < 9.0 V 9.0 V < V_{PWR} < 16 V 16 V < V_{PWR} < 27 V	SR_{F_SLOW}	 0.05 0.08 0.08	 – 0.15 –	 0.3 0.4 0.5	V/µs
High-Side Output Turn ON Delay Time (29)	$t_{DLY(ON)}$	5.0	30	150	µs
High-Side Output Turn OFF Delay Time (30)	$t_{DLY(OFF)}$	5.0	80	150	µs
Low-Side Output Falling Slew Rate (31)	SR_F	0.5	3.0	10	V/µs
Low-Side Output Rising Slew Rate (31)	SR_R	1.0	6.0	20	V/µs
Low-Side Output Turn ON Delay Time (32)	$t_{DLY(ON)}$	0.5	2.0	10	µs
Low-Side Output Turn OFF Delay Time (33)	$t_{DLY(OFF)}$	0.5	4.0	10	µs
Low-Side Output Fault Delay Timer (34)	$t_{DLY(\overline{FS})}$	70	150	250	µs

Notes

27. High-side output rise and fall fast slew rates measured across a 5.0 Ω resistive load at high-side output = 0.5 V to V_{PWR}-3.0 V (see Figure 5, page 17). These parameters are guaranteed by process monitoring.
28. High-side output rise and fall slow slew rates measured across a 5.0 Ω resistive load at high-side output = 0.5 V to V_{PWR}-3.0 V (see Figure 5, page 17). These parameters are guaranteed by process monitoring.
29. High-side output turn-ON delay time measured from 50% of the rising IHS to 0.5 V of output OFF with R_L = 27 Ω resistive load (see Figure 5, page 17).
30. High-side output turn-OFF delay time measured from 50% of the falling IHS to V_{PWR}-2.0 V of the output OFF with R_L = 27 Ω resistive load (see Figure 5, page 17).
31. Low-side output rise and fall slew rates measured across a 5.0 Ω resistive load at low-side output = 10% to 90% (see Figure 6, page 17).
32. Low-side output turn-ON delay time measured from 50% of the rising ILS to 90% of V_{OUT} with R_L = 27 Ω resistive load (see Figure 6, page 17).
33. Low-side output turn-OFF delay time measured from 50% of the falling ILS to 10% of V_{OUT} with R_L = 27 Ω resistive load (see Figure 6, page 17). These parameters are guaranteed by process monitoring.
34. Propagation time of Short Fault Disable Report Delay measured from rising edge of $\overline{CS}$ to output disabled, low-side = 5.0 V, and device configured for low-side output overcurrent latch-off using CLOCCR.

Table 6. Dynamic Electrical Characteristics (continued)

Characteristics noted under conditions 6.0 V $\leq V_{PWR} \leq$ 27 V, 4.5 V $\leq V_{DD} \leq$ 5.5 V, -40°C $\leq T_J \leq$ 150°C unless otherwise noted. Typical values noted reflect the approximate parameter means at T_A = 25°C under nominal conditions unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
POWER OUTPUT TIMING (continued)					
Watchdog Timeout (35)	t_{WDTO}	340	584	770	ms
Peak Current Limit Timer (36)	t_{PCT}	40	70	100	ms
Direct Input Switching Frequency (37)	f_{PWM}	–	125	–	Hz
SPI INTERFACE TIMING (38)					
Recommended Frequency of SPI Operation Normal Mode Extended Mode: V_{DD} = 3.4 V; V_{PWR} = 4.5 V, APNB Suffix Only	f_{SPI}	 – –	 – –	 3.0 2.1	MHz
Required Low State Duration for $\overline{\text{RST}}$ (39)	t_{WRST}	–	50	167	ns
Rising Edge of $\overline{\text{CS}}$ to Falling Edge of $\overline{\text{CS}}$ (Required Setup Time) (40)	t_{CS}	–	–	300	ns
Rising Edge of $\overline{\text{RST}}$ to Falling Edge of $\overline{\text{CS}}$ (Required Setup Time) (40)	t_{ENBL}	–	–	5.0	µs
Falling Edge of $\overline{\text{CS}}$ to Rising Edge of SCLK (Required Setup Time) (40)	t_{LEAD}	–	50	167	ns
Required High State Duration of SCLK (Required Setup Time) (40)	t_{WSCLKh}	–	–	167	ns
Required Low State Duration of SCLK (Required Setup Time) (40)	t_{WSCLKl}	–	–	167	ns
Falling Edge of SCLK to Rising Edge of $\overline{\text{CS}}$ (Required Setup Time) (40)	t_{LAG}	–	50	167	ns
SI to Falling Edge of SCLK (Required Setup Time) (40)	$t_{SI(SU)}$	–	25	83	ns
Falling Edge of SCLK to SI (Required Hold Time) (40)	$t_{SI(HOLD)}$	–	25	83	ns
SO Rise Time C_L = 200 pF	t_{RSO}	 –	 25	 50	ns
SO Fall Time C_L = 200 pF	t_{FSO}	 –	 25	 50	ns
SI, $\overline{\text{CS}}$, SCLK, Incoming Signal Rise Time (41)	t_{RSI}	–	–	50	ns
SI, $\overline{\text{CS}}$, SCLK, Incoming Signal Fall Time (41)	t_{FSI}	–	–	50	ns
Time from Falling Edge of $\overline{\text{CS}}$ to SO Low Impedance (42)	$t_{SO(EN)}$	–	–	145	ns
Time from Rising Edge of $\overline{\text{CS}}$ to SO High Impedance (43)	$t_{SO(DIS)}$	–	65	145	ns
Time from Rising Edge of SCLK to SO Data Valid (44) 0.2 $V_{DD} \leq$ SO $\geq$ 0.8 V_{DD}, C_L = 200 pF	t_{VALID}	 –	 65	 105	ns

Notes

35. Watchdog timeout delay is measured from the rising edge of WAKE or $\overline{\text{RST}}$ from the sleep state to the HS[0:1] turn-ON with the outputs driven OFF and the FSI floating. The accuracy of t_{WDTO} is maintained for all configured watchdog time-outs.
36. t_{PCT} measured from the rising edge of $\overline{\text{CS}}$ to 90% of $I_{LIMPKHS[x,x]}$ when the peak current limit is enabled.
37. This frequency is a typical value. Maximum switching frequencies are dictated by the turn-ON delay, turn-OFF delay, output rise and fall times, and the maximum allowable junction temperature.
38. Symmetrical 50% duty cycle SCLK clock period of 333 ns.
39. $\overline{\text{RST}}$ low duration measured with outputs enabled and going to OFF or disabled condition.
40. Maximum setup time required for the 33888 is the minimum guaranteed time needed from the MCU.
41. Rise and fall time of incoming SI, $\overline{\text{CS}}$, and SCLK signals suggested for design consideration to prevent the occurrence of double pulsing.
42. Time required for output status data to be available for use at SO. 1.0 kΩ pullup on $\overline{\text{CS}}$.
43. Time required for output status data to be terminated at SO. 1.0 kΩ pullup on $\overline{\text{CS}}$.
44. Time required to obtain valid data out from SO following the rise of SCLK.

TIMING DIAGRAMS

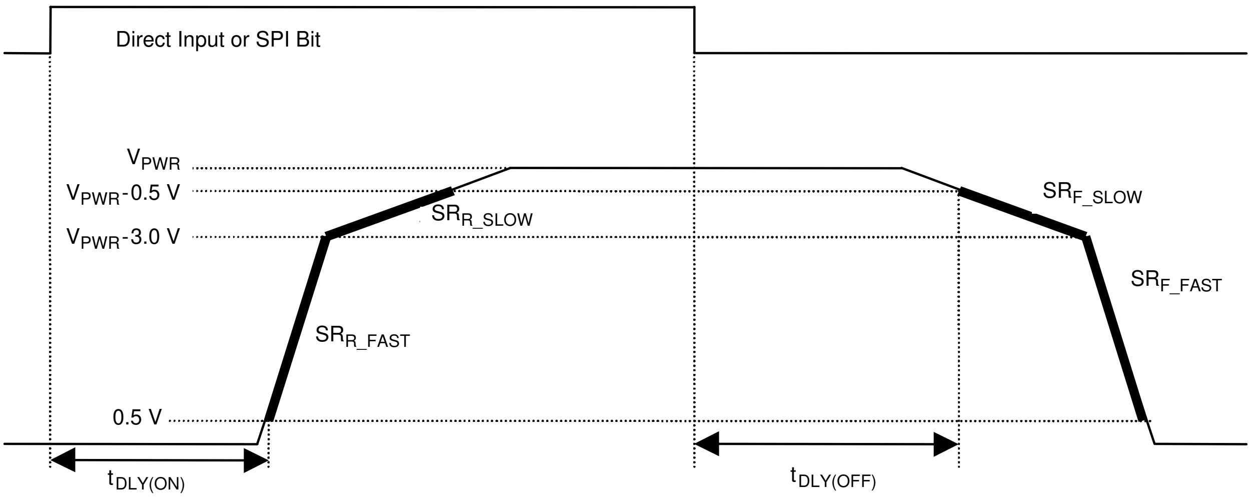

Direct Input or SPI Bit
V_{PWR}
V_{PWR}-0.5 V
V_{PWR}-3.0 V
SR_{R_SLOW}
SR_{F_SLOW}
SR_{F_FAST}
SR_{R_FAST}
0.5 V
$t_{DLY(ON)}$
$t_{DLY(OFF)}$

Figure 5. Output Slew Rates and Time Delays, High Side

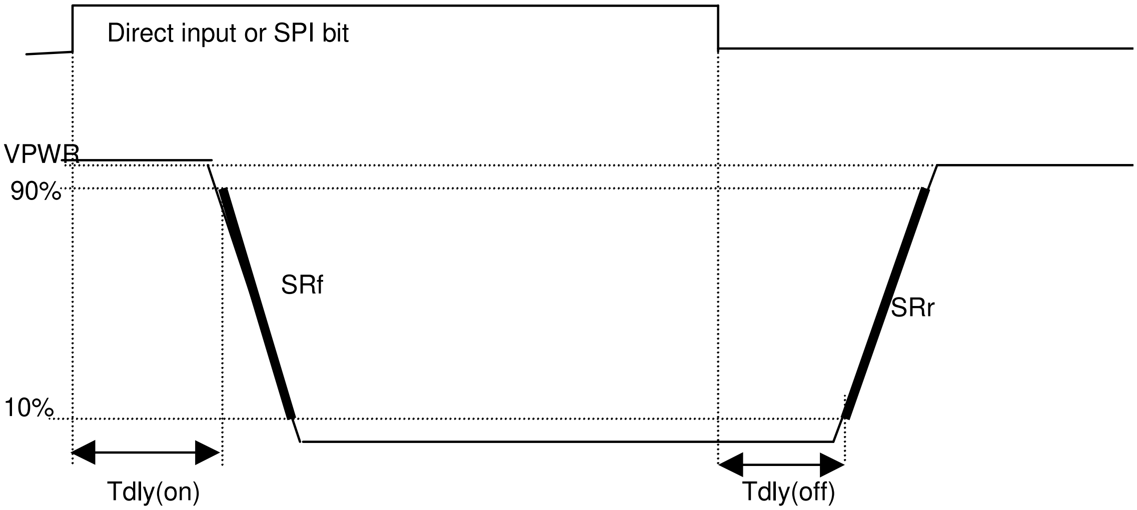

Direct input or SPI bit
VPWR
90%
SRf
SRr
10%
Tdly(on)
Tdly(off)

Figure 6. Output Slew Rates and Time Delays, Low Side

FUNCTIONAL DESCRIPTION

INTRODUCTION

This 33888 is a single-package combination of a power die with four discrete high-side MOSFETs and an integrated IC control die consisting of eight low-side drivers with appropriate control, protection, and diagnostic features. The high-side drivers are useful for both internal and external vehicle lighting applications as well as capable of driving inductive solenoid loads. The low-side drivers are capable of controlling low-current on/off type inductive loads, such as relays and solenoids as well as LED indicators and small lamps (see Figure 2, page 3). The device is useful in body control, instrumentation, and other high-power switching applications and systems.

The 33888 is available in two packages: a power-enhanced 12 x 12 non-leaded Power QFN package with exposed tabs and a 64-lead Power QFP plastic package. Both packages are intended to be soldered directly onto the printed circuit board.

The 33888 differs from the 33888A as explained in Table 1, page 2.

FUNCTIONAL PIN DESCRIPTION

FAULT STATUS (FS)

This output pin is an open drain indication that goes active low when a fault mode is detected by the device. Specific device fault indication is given via the SO pin.

POSITIVE POWER SUPPLY (V_{PWR})

These pin connects to the positive power supply and are the source input of operational power for the device.

LOW-SIDE OUTPUT (LS4, LS6, LS8, LS10)

Each low-side pin is one 0.6 Ω low-side output MOSFET drain, which pulls current through the connected loads. Each of the outputs is actively clamped at 53 V. These outputs are current and thermal overload protected. Maximum steady state current through each of these outputs is 500 mA.

GROUND (GND)

These pins serve as the ground for the source of the low-side output transistors as well as the logic portion of the device.

LOW-SIDE OUTPUT (LS5, LS7, LS9, LS11)

Each low-side pin is one 0.6 Ω low-side output MOSFET drain, which pulls current through the connected loads. Each of the outputs is actively clamped at 53 V. These outputs are current and thermal overload protected. Maximum steady state current through each of these outputs is 800 mA.

DIGITAL DRAIN VOLTAGE (V_{DD})

This is an external input pin used to supply power to the SPI circuit.

SERIAL OUTPUT (SO)

This is an output pin connected to the SPI Serial Data Input pin of the MCU or to the SI pin of the next device in a daisy chain. This output will remain tri-stated unless the device is selected by a low CS pin. The output signal generated will have CMOS logic levels and the output data will transition on the rising edges of SCLK. The serial output data provides fault information for each output and is returned MSB first when the device is addressed. OD11 through OD0 are output fault bits for outputs 11 through 0, respectively.

CHIP SELECT (CS)

This is an input pin connected to a chip select output of a microcontroller (MCU). This IC controls which device is addressed (selected) by pulling the CS pin of the desired device logic Low, enabling the SPI communication with the device, while other devices on the serial link keep their serial outputs tri-stated. This input has an internal active pullup and requires CMOS logic levels.

SERIAL CLOCK (SCLK)

This input pin is connected to the SCLK pin of the master MCU, which is a bit (shift) clock for the SPI port. It transitions one time per bit transferred at an operating frequency, fSPI, and is idle between command transfers. It is 50% duty cycle and has CMOS logic levels. This signal is used to shift data to and from the 33888.

SERIAL INPUT (SI)

This input pin is connected to the SPI Serial Data Output pin of the MCU from which it receives output command data. This input has an internal active pull-down and requires CMOS logic levels. The serial data transmitted on this line is a 16-bit control command sent MSB first, which controls the twelve output channels. Bits D3:D0 control the high-side outputs HS3:HS0, respectively. Bits D11:D4 control the low-side outputs LS11:LS4, respectively. The MUC will ensure that data is available on the falling edge of SCLK.

LOW-SIDE INPUT (ILS)

This input pin is used to directly control a number of the low-side devices as configured by SPI. This pin may or may not be activated depending on the configured state of the internal logic.

HIGH-SIDE INPUT (IHS3, IHS2, IHS0, IHS1)

Each high-side input pin is used to directly control only one designated high-side output. These inputs may or may not be activated depending on the configured state of the internal logic.

CURRENT SENSE (2-3, 0-1)

These pins deliver a metered amount of the high-side output current that can be used to generate signal ground referenced output voltages for use by the MCU. Each respective CSNS pin can be configured via SPI to deliver current from either of the two assigned outputs, or the currents could be the sum of the two. Current from HS0 and/or HS1 are sensed via CSNS0-1. Current from HS2 and/or HS3 are sensed via CSNS2-3.

HIGH SIDE OUTPUT (HS3, HS2)

Each pin is the source of a 40 mΩ MOSFET high-side driver, which delivers current through the connected loads. These outputs can be controlled via SPI or using the IHS pins depending on the internal configuration. These outputs are current limited and thermally protected. During fail-safe mode, output HS2 will be turned on until the device is re-initialized and then immediately followed by normal operation.

HIGH SIDE OUTPUT (HS1, HS0)

Each pin is the source of a 10 mΩ MOSFET high-side driver, which delivers current through the connected loads. These outputs can be controlled via SPI or using the IHS pins depending on the internal configuration. These outputs are current limited and thermally protected. During fail-safe mode, output HS0 will be turned on until the device is re initialized and then immediately followed by normal operation.

WAKE (WAKE)

This pin is used to input a logic [1] signal in order to enable the watchdog timer function. An internal clamp protects the pin from high voltages when current is limited with an external resistor. This input has a passive internal pulldown.

RESET (RST)

This input pin is used to initialize the device configuration and fault registers, as well as place the device in a low current standby mode. This pin also starts the watchdog timeout when transitioned from logic [0] to logic [1]. This pin should not be allowed to be at logic [1] until VDD is in regulation. This input has an internal passive pulldown.

FAIL-SAFE INPUT (FSI)

The Fail-Safe input pin level determines the state of the outputs after a watchdog timeout occurs. This pin has an internal pullup. If the FSI pin is left to float to a logic [1], then HS0 and HS2 will turn on when in the Fail-Safe state. If the FSI pin is tied to GND, the watchdog circuit and fail-safe operation will be disabled, thus allowing operation without a watchdog signal.

WATCHDOG INPUT (WDIN)

This input pin is a CMOS logic level input that is used to monitor system operation. If the incoming watchdog signal does not transition within the normal watchdog timeout range, the device will operate in the Fail-Safe mode. This input has an active internal pulldown.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

WATCHDOG AND FAIL-SAFE OPERATION

The watchdog is enabled and a timeout is started when the WAKE or $\overline{\text{RST}}$ transitions from logic [0] to logic [1]. The WAKE input is capable of being pulled up to V_{PWR} with a series limiting resistance that limits the internal clamp current. The timeout is a multiple of an internal oscillator. As long as the WDIN pin or the WD bit (D15) of an incoming SPI message is toggled within the minimum watchdog timeout, WDTO (or a divided value configured during a WDCSCR message), then the device will operate normally. If the watchdog timeout occurs before the WD bit or the WDIN pin is toggled, then the device will revert to a Fail-Safe mode until the device is re initialized (if the FSI pin is left disconnected).

During Fail-Safe mode, all outputs will be OFF except for HS0 and HS2, which will be driven ON regardless of the state of the various direct inputs and modes (Table 7). The device can be brought out of the Fail-Safe mode by transitioning the WAKE and $\overline{\text{RST}}$ pins from logic [1] to logic [0]. In the event the WAKE pin was not transitioned to a logic [1] during normal operation and the watchdog times out, then the device can be brought out of fail-safe by bringing the $\overline{\text{RST}}$ to a logic [0]. If the FSI pin is tied to GND, then the watchdog, and therefore fail-safe operation, will be disabled.

DEFAULT MODE

The default mode describes the state of the device after first applying V_{PWR} voltage or a reset transition from logic [0] to logic [1] prior to SPI communication. In the default mode, all outputs will be off (assuming that the direct inputs ILS and IHS[0:3] and the WAKE pin are at logic [0]). All of the specific pin functions will operate as though all of the addressable configuration register bits were set to logic [0]. This means, for example, that all of the low-side outputs will be controllable by the ILS pin, and that all high-side outputs will be controllable via their respective IHS pins. During the default mode, all high-side drivers will default with open load detection enabled. All low-side drivers will default with open load detection disabled. This mode allows limited control of the 33888 with the direct inputs in the absence of an SPI.

Returning the device to the default state after a period of normal operation, followed by the removal of the V_{PWR} voltage, requires that the $\overline{\text{RST}}$ input be held at a logic [0] state until V_{PWR} falls to a level below 2.0 V. If the $\overline{\text{RST}}$ and V_{DD} input levels are normal, then failure to allow V_{PWR} to fall below 2.0 V will result in an internal bias circuit clamping the V_{PWR} pin to approximately 3.5 V. Once V_{PWR} falls below 2.0 V, the $\overline{\text{RST}}$ can be returned to 5.0 V without re-enabling the bias circuit.

Table 7. Fail-Safe Operation and Transitions to Other 33888 Modes

WAKE	$\overline{\text{RST}}$	WDTO	HS0	HS2	LS[4:11], HS[1,3]	Comments
0	0	x	OFF	OFF	OFF	Device in Sleep mode.
1	0	NO	OFF	OFF	OFF	All outputs are OFF. When $\overline{\text{RST}}$ transitions to logic [1], device is in default.
1	0	YES	ON	ON	OFF	Fail-Safe mode. Device reset into Default mode by transitioning WAKE to logic [0].
0	1	NO	S	S	S	Device in Normal operating mode.
0	1	YES	ON	ON	OFF	Fail-Safe mode. Device reset into Default mode by transitioning $\overline{\text{RST}}$ to logic [0].
1	1	NO	S	S	S	Device in Normal operating mode.
1	1	YES	ON	ON	OFF	Fail-Safe mode. Device reset into Default mode by transitioning $\overline{\text{RST}}$ and WAKE to logic [0].

Assumptions: Normal operating voltage and junction temperatures, FSI pin floating.
x = Don't care.
S = State determined by SPI and/or direct input configurations.

FAULT LOGIC REQUIREMENTS

The 33888 indicates all of the following faults as they occur:

- Overtemperature Fault
- Overvoltage Fault
- Open Load Fault
- Overcurrent Fault

With the exception of the overvoltage, these faults are output specific. The overvoltage fault is a global fault. The overcurrent fault is only reported for the low-side outputs.

The 33888 low-side outputs incorporate an internal fault filter, $t_{DLY(\overline{FS})}$. The fault timer filters noise and switching transients for overcurrent faults when the output is ON and open load faults when the output is OFF. All faults are latched and indicated by a logic [1] for each output in the 33888 status word (Table 10, page 25). If the fault is removed, the status bit for the faulted output will be cleared by a rising edge on $\overline{\text{CS}}$.

The $\overline{\text{FS}}$ pin is driven to a logic [0] when a fault exists on any of the outputs. $\overline{\text{FS}}$ provides real time monitoring of the overvoltage fault. For the high-side outputs, $\overline{\text{FS}}$ provides real time monitoring of the open load and overtemperature. For the low-side outputs, the $\overline{\text{FS}}$ is latched to a logic [0] for open load, overtemperature, and overcurrent faults. The latch is cleared by toggling the state of the faulted output or by bringing $\overline{\text{RST}}$ low.

OVERTEMPERATURE FAULT

The 33888 incorporates overtemperature detection and shutdown circuitry into each individual output structure. Overtemperature detection occurs when an output is in the ON state. When an output is shut down due to an overtemperature condition, no other output is affected. The output experiencing the fault is shut down to protect itself from damage. A fault bit is loaded into the status register if the overtemperature condition is removed, and the fault bit is cleared upon the rising edge of $\overline{\text{CS}}$.

For the low-side outputs, the faulted output is latched OFF during an overtemperature condition. If the temperature falls below the recovery level, $T_{LIM(HYS)}$, then the output can be turned back ON only after the output has first been commanded OFF either through the SPI or the ILS, depending on the logic configuration.

For the high-side output(s), an overtemperature condition will result in the output(s) turning OFF until the temperature falls below the $T_{LIM(HYS)}$. This cycle will continue indefinitely until action is taken by the MCU to shut the output(s) OFF.

OVERVOLTAGE FAULT

The 33888 shuts down all outputs during an overvoltage condition on the V_{PWR} pin. The outputs remain in the OFF state until the overvoltage condition is removed. Fault status for all outputs is latched into the status register. Following an overvoltage condition, the next write cycle sent by the SO pin of the 33888 is logic [1] on OD11:OD0, indicating all outputs have shut down. If the overvoltage condition is removed, the status register can be cleared by a rising edge on $\overline{\text{CS}}$.

OPEN LOAD FAULT

The 33888 incorporates open load detection circuitry on every output. A high-side or low-side output open load fault is detected and reported as a fault condition when the corresponding output is disabled (OFF) if it was configured for open load detection by setting the appropriate bit to logic [0] (HS3:HS0) or logic [1] (LS11:LS4) in the OLFCR register (see Figure 7).

The high-side open load fault is detected and latched into the status register after the internal gate voltage is pulled low enough to turn off the output. If the open load fault is removed or if the faulted output is commanded ON, the status register can be cleared by a rising edge on $\overline{\text{CS}}$. Note that the device default state will enable the high-side open load detection and disable the low-side open load detection circuits, respectively.

It is recommended to disable the open load detection circuitry (OL bit sets to logic [1]) in case of a permanent open load fault condition.

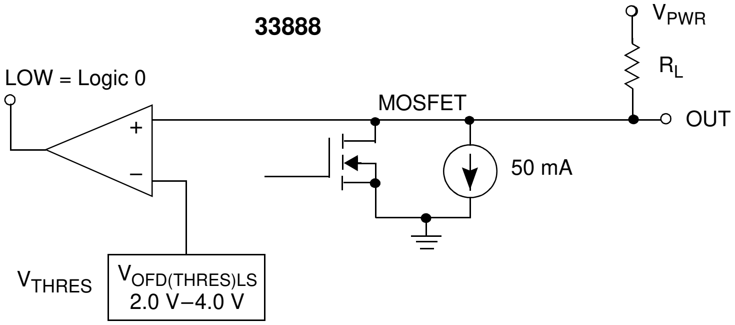


Figure 7. Low-Side Output OFF Open Load Detection

OVERCURRENT FAULT REQUIREMENTS: LOW-SIDE OUTPUT

An overcurrent condition is defined as any current value greater than I_{LIM} (500 mA minimum value for LS5, LS7, LS9, LS11, and 800 mA minimum value for LS4, LS6, LS8, LS10). The status of the corresponding bit in the CLOCCR register determines whether a specific output shuts down or continues to operate in an analog current limited mode until either the overcurrent condition is removed or the thermal shutdown limit is reached (Figure 10, page 27). If the overcurrent shutdown mode is disabled, the fault reporting is disabled as well.

For the low-side output of interest, if a D11:D4 bit was set to a logic [1] in the OLCR register, the overcurrent protection shutdown circuitry will be enabled for that output. When a low-side output is commanded ON either from the SPI or the ILS pin, the drain of the low-side driver will be monitored for a voltage greater than the fault detection threshold (3.0 V typical). If the drain voltage exceeds this threshold, a timer will start and the output will be turned off and a fault latched in the status register after the timeout expires. The faulted output can be retried only by commanding the output OFF and back ON either through the SPI or the ILS pin, depending on the logic configuration. If the fault is gone, the retried output will return to normal operation and the status register can be cleared on a rising edge of $\overline{\text{CS}}$. If the fault remains, the retried output will latch off after the fault timer expires and the fault bit will remain set in the status register.

For the low-side output of interest, if a D11:D4 bit was set to a logic [0] in the OLCR register, the output experiencing an overcurrent condition is not disabled until an overtemperature fault threshold has been reached. The specific output goes into an analog current limit mode of operation, I_{LIM}. The 33888 uses overtemperature shutdown to protect all outputs in this mode of operation. If the overcurrent condition is removed before the output has reached its overtemperature limit, the output will function as if no fault has occurred.

Note that each pair of low-side drivers, LS4:LS5, LS6:LS7, LS8:LS9, and LS10:LS11, consists of a 500 mA and a 800 mA output. Each pair of outputs shares ground bond wires. The bond wires are not rated to handle both outputs in current limit mode simultaneously.

OVERCURRENT FAULT REQUIREMENTS: HIGH-SIDE OUTPUT

For the high-side output of interest, the output current is limited to one of four levels depending on the type of high-side output, the amount of time that has elapsed since the output was switched on, and the state of the CLOCCR register. Assuming that bits D3:D0 of the CLOCCR register are at logic [0], the current limit levels of the outputs will be initially at their peak levels as specified by the $I_{LIM(PK)HS[0:3]}$. After the high-side output is switched on, the peak current timer starts. After a period of time t_{PCT}, the current limit level changes to the sustain levels $I_{LIMSUSHS[x,x]}$.

For the high-side output of interest, if a D3:D0 bit of the CLOCCR is at logic [1], then the assigned output will only current limit at the sustain level specified by $I_{LIMSUSHS[x,x]}$.

Current is limited until the overtemperature circuitry shuts OFF the device. The device turns ON automatically when the temperature fails below the $T_{LIM(HYS)}$. This cycle continues indefinitely until action is taken by the master to shut the output(s) OFF.

LOGIC COMMANDS AND REGISTERS

SPI INTERFACE AND PROTOCOL DESCRIPTION

The SPI interface has full duplex, three-wire synchronous data transfer and has four I/O lines associated with it: Serial Clock (SCLK), Serial Input (SI), Serial Output (SO), and Chip Select ($\overline{\text{CS}}$).

The SI/SO pins of the 33888 follow a first-in first-out (D15/D0) protocol with both input and output words transferring the most significant bit first. All inputs are compatible with 5.0 V CMOS logic levels. During SPI output control, a logic [0] in a message word will result in the designated output being turned off. Similarly, a logic [1] will turn on a corresponding output.

The SPI lines perform the following functions:

Serial Clock (SCLK)

The SCLK pin clocks the internal shift registers of the 33888. The serial input (SI) pin accepts data into the input shift register on the falling edge of the SCLK signal while the serial output pin (SO) shifts data information out of the SO line driver on the rising edge of the SCLK signal. It is important that the SCLK pin be in a logic [0] state whenever the chip select ($\overline{\text{CS}}$) makes any transition. For this reason, it is recommended that the SCLK pin be kept in a logic [0] state as long as the device is not accessed ($\overline{\text{CS}}$ in logic [1] state). SCLK has an active internal pulldown, I_{DWN}. When $\overline{\text{CS}}$ is logic [1], signals at the SCLK and SI pins are ignored and SO is tri-stated (high impedance). (See Figures 8 and 9 on page 23.)

Serial Interface (SI)

This is a serial interface (SI) command data input pin. Each SI bit is read on the falling edge of SCLK. A 16-bit stream of serial data is required on the SI pin, starting with D15 to D0. The 12 outputs of the 33888 are configured and controlled using the 3-bit addressing scheme and the 12 assigned data bits designed into the 33888. SI has an active internal pulldown, I_{DWN}.

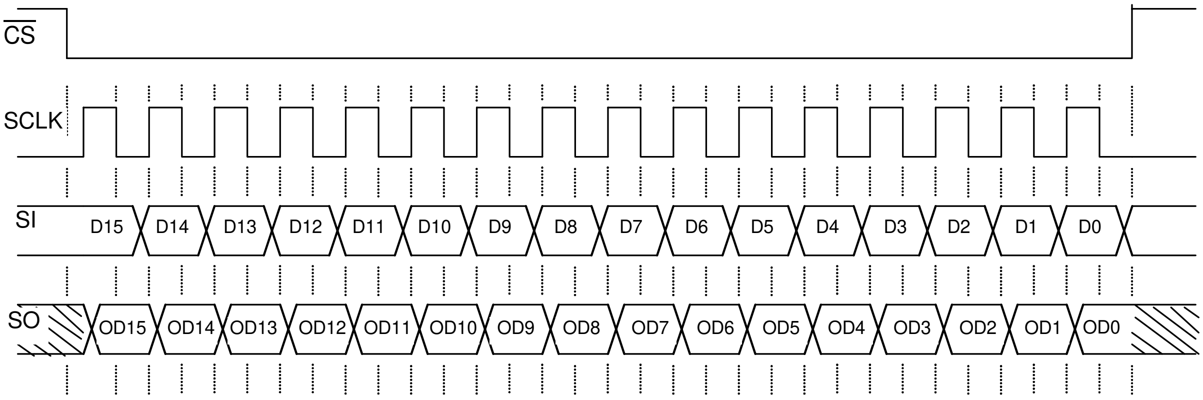
Serial Output (SO)

The SO data pin is a tri-stateable output from the shift register. The SO pin remains in a high-impedance state until the $\overline{\text{CS}}$ pin is put into a logic [0] state. The SO data report the status of the outputs as well as provide the capability to reflect the state of the direct inputs. The SO pin changes states on the rising edge of SCLK and reads out on the falling edge of SCLK. When an output is ON or OFF and not faulted, the corresponding SO bit, OD11:OD0, is a logic [0]. If the output is faulted, the corresponding SO state is a logic [1]. SO OD14:OD12 reflect the state of six various inputs (three at a time) depending upon the reported state of the previously written watchdog bit OD15.

Chip Select ($\overline{\text{CS}}$)

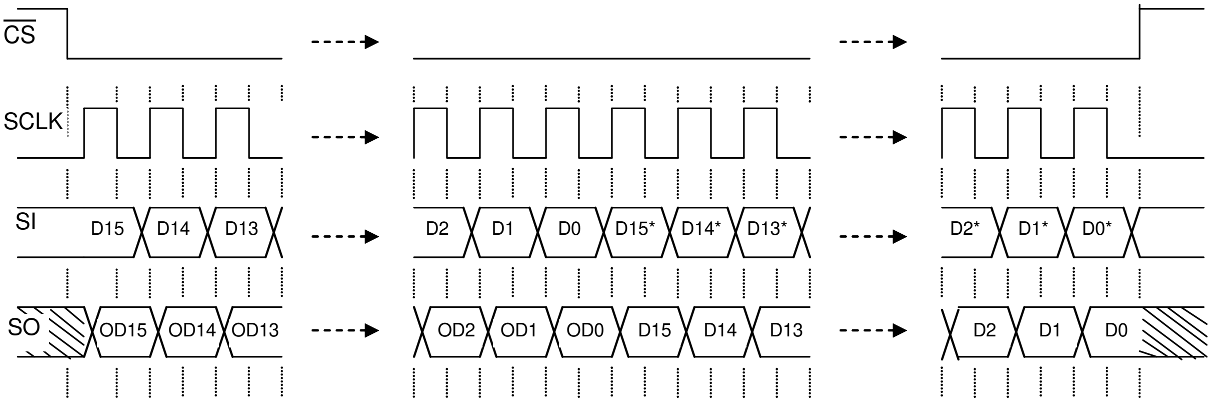
The $\overline{\text{CS}}$ pin enables communication with the master microcontroller (MCU). When this pin is in a logic [0] state, the 33888 is capable of transferring information to and receiving information from the MCU. The 33888 latches in data from the input shift registers to the addressed registers on the rising edge of $\overline{\text{CS}}$. The 33888 transfers status information from the power outputs to the shift registers on the falling edge of $\overline{\text{CS}}$. The output driver on the SO pin is enabled when $\overline{\text{CS}}$ is logic [0]. $\overline{\text{CS}}$ is only transitioned from a logic [1] state to a logic [0] state when SCLK is a logic [0]. $\overline{\text{CS}}$ has an active internal pullup, I_{UP}.

The 33888 is capable of communicating directly with the MCU via the 16-bit SPI protocol as described in the next section.



Notes
1. RST is in a logic [1] state during the above operation.
2. D15:D0 relate to the most recent ordered entry of program data into the 33888.
3. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the 33888.

Figure 8. Single 16-Bit Word SPI Communication



Notes
1. RST is a logic [1] state during the above operation.
2. D15:D0 relate to the most recent ordered entry of program data into the 33888.
3. D15*:D0* relate to the first 16 bits of ordered entry data out of the 33888.
4. OD15:OD0 relate to the first 16 bits of ordered fault and status data out of the 33888.

Figure 9. Multiple 16-Bit Word SPI Communication

SERIAL INPUT COMMUNICATION

SPI communication is accomplished using 16-bit messages. A message is transmitted by the MCU starting with the MSB, D15, and ending with the LSB, D0 (refer to Table 8, page 23). Each incoming command message on the SI pin can be interpreted using the following bit assignments: the first twelve LSBs, D11:D0, control each of the twelve outputs; the next three bits, D14:D12, determine the command mode; and the MSB, D15, is the watchdog bit.

Multiple messages can be transmitted in succession to accommodate those applications where daisy chaining is desirable or to confirm transmitted data, as long as the messages are all multiples of 16 bits. Any attempt made to latch in a message that is not 16 bits will be ignored.

The 33888 has six registers that are used to configure the device and control the state of the four high-side and eight low-side outputs (Table 9, page 24). The registers are addressed via D14:D12 of the incoming SPI word (Table 8, page 23).

Table 8. SI Message Bit Assignment

Bit Sig	SI Msg Bit	Message Bit Description
MSB	D15	Watchdog in: toggled to satisfy watchdog requirements.
	D14:12	Register address bits.
	D11	Used to configure Low-Side Output LS11.
	D10	Used to configure Low-Side Output LS10.

Table 8. SI Message Bit Assignment (continued)

Bit Sig	SI Msg Bit	Message Bit Description
	D9	Used to configure Low-Side Output LS9.
	D8	Used to configure Low-Side Output LS8.
	D7	Used to configure Low-Side Output LS7.
	D6	Used to configure Low-Side Output LS6.
	D5	Used to configure Low-Side Output LS5 (Watchdog timeout MSB during WDCSCR configuration).
	D4	Used to configure Low-Side Output LS4 (Watchdog timeout LSB during WDCSCR configuration).
	D3	Used to configure High-Side Output HS3.
	D2	Used to configure High-Side Output HS2.
	D1	Used to configure High-Side Output HS1.
LSB	D0	Used to configure High-Side Output HS0.

Table 9. Serial Input Address and Configuration Bit Map

SI Register	WD	Address			Low-Side								High-Side			
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
SOCR	x	0	0	0	LS11	LS10	LS9	LS8	LS7	LS6	LS5	LS4	HS3	HS2	HS1	HS0
DICR	x	1	0	0	PWB11	PWB10	PWB9	PWB8	PWB7	PWB6	PWB5	PWB4	PWB3	PWB2	PWB1	PWB0
LFCR	x	0	1	0	A/OB11	A/OB10	A/OB9	A/OB8	A/OB7	A/OB6	A/OB5	A/OB4	A/OB3	A/OB2	A/OB1	A/OB0
WDCSCR	x	1	1	0	NA	NA	NA	NA	NA	NA	WDH	WDL	CS3	CS2	CS1	CS0
OLCR	x	0	0	1	OL11	OL10	OL9	OL8	OL7	OL6	OL5	OL4	OLB3	OLB2	OLB1	OLB0
CLOCCR	x	1	0	1	OC11	OC10	OC9	OC8	OC7	OC6	OC5	OC4	ILIM3	ILIM2	ILIM1	ILIM0
NOT USED	x	0	1	1	–	–	–	–	–	–	–	–	–	–	–	–
TEST	x	1	1	1	–	–	–	–	–	–	–	–	ILIMPK	WD	ILIM	OT

x=Don’t care.
NA=Not applicable.

LOGIC COMMANDS AND REGISTERS

DEVICE REGISTER ADDRESSING

The following section describes the possible register addresses and their impact on device operation.

Address 000—SPI Output Control Register (SOCR)

The SOCR register allows the MCU to control the outputs via the SPI. Incoming message bits D3:D0 reflect the desired states of high-side outputs HS3:HS0. Message bits D11:D4 reflect the desired state of low-side outputs LS11:LS4, respectively.

Address 100—Direct Input Control Register (DICR)

The DICR register is used by the MCU to enable direct input control of the outputs. For the outputs, a logic [0] on bits D11:D0 will enable the corresponding output for direct control. A logic [1] on a D11:D0 bit will disable the output from direct control.

Address 010—Logic Function Control Register (LFCR)

The LFCR register is used by the MCU to configure the relationship between SOCR bits D11:D0 and the direct inputs IHS[0:3] and ILS. While addressing this register (if the direct inputs were enabled for direct control with the DICR), a logic [1] on any or all of the D3:D0 bits will result in a Boolean AND of the IHS[0:3] pin(s) with its (their) corresponding D3:D0 message bit(s) when addressing the SOCR. A logic [1] on any or all of the D11:D4 bits will result in a Boolean AND of the ILS and the corresponding D11:D4 message bits when addressing the SOCR. Similarly, a logic [0] on the D3:D0 bits will result in a Boolean OR of the IHS[0:3] pin(s) with their corresponding message bits when addressing the SOCR register, and the ILS will be Boolean OR’d with message bits D11:D4 when addressing the SOCR register (if ILS is enabled).

Address 110—Watchdog and Current Sense Configuration Register (WDCSCR)

The WDCSCR register is used by the MCU to configure the watchdog timeout and the CSNS0-1 and CSNS2-3 pins. The watchdog timeout is configured using bits D4 and D5. The state of D4 and D5 determine the divided value of the WDTO. For example, if D5 and D4 are logic [0] and logic [0], respectively, then the WDTO will be in the default state as specified in Table 9, page 24. A D5 and a D4 of logic [0] and logic [1] will result in a watchdog timeout of WDTO ÷ 2. Similarly, a D5 and a D4 of logic [1] and logic [0] result in a watchdog timeout of WDTO ÷ 4, and a D5 and a D4 of logic [1] and logic [1] result in a watchdog timeout of WDTO ÷ 8. Note that when D5 and D4 bits are programmed for the desired watchdog timeout period, the WD bit (D15) should be toggled as well to ensure that the new timeout period is programmed at the beginning of a new count sequence.

CSNS0-1 is the current sense output for the HS0 and HS1 outputs. Similarly, the CSNS2-3 pin is the current sense output for the HS2 and HS3 outputs. In this mode, a logic [1] on any or all of the message bits that control the high-side outputs will result in the sensed current from the corresponding output being directed out of the appropriate CSNS output. For example, if D1 and D0 are both logic [1], then the sensed current from HS0 and HS1 will be summed into the CSNS0-1. If D2 is logic [1] and D3 is logic [0], then only the sensed current from HS2 will be directed out of CSNS2-3.

Address 001—Open Load Configuration Register (OLCR)

The OLCR register allows the MCU to configure each of the outputs for open load fault detection. While in this mode, a logic [1] on any of the D3:D0 message bits will disable the corresponding outputs' circuitry that allows the device to detect open load faults while the output is OFF. For the low-side drivers, a logic [1] on any of the D11:D4 bits will enable the open load detection circuitry. This feature allows the MCU to minimize load current in some applications and may be useful to diagnose output shorts to battery (for HS).

Address 101—Current Limit Overcurrent Configuration Register (CLOCCR)

The CLOCCR register allows the MCU to individually override the peak current limit levels for each of the high-side outputs. A logic [1] on any or all of the D3:D0 bit(s) results in the corresponding HS3:HS0 output pins to current limit at the sustain current limit level. This register also allows the MCU to enable or disable the overcurrent shutdown of the low-side output pins. A logic [1] on any or all of the D11:D4 message bit(s) will result in the corresponding LS11:LS4 pins latching off if the current exceeds I_{LIM} after a timeout of $t_{DLY(\overline{FS})}$.

Address 011—Not Used

Not currently used.

Address 111—TEST

The TEST register is reserved for test and is not accessible via SPI during normal operation.

SERIAL OUTPUT COMMUNICATION (DEVICE STATUS RETURN DATA)

When the $\overline{\text{CS}}$ pin is pulled low, the output status register for each output is loaded into the output register and the fault data is clocked out MSB (OD15) first as the new message data is clocked into the SI pin.

OD15 reflects the state of the watchdog bit (D15) that was addressed during the prior SOCR communication (refer to Table 10, page 25). If bit OD15 is logic [0], then the three MSBs OD14:OD12 will reflect the logic states of the IHS0, IHS1, and FSI pins, respectively. If bit OD15 is logic [1], then the same three MSB bits will reflect the logic states of the IHS2, IHS3, and WAKE pins. The next twelve bits clocked out of SO following a low transition of the $\overline{\text{CS}}$ pin (OD11:OD0) will reflect the state of each output, with a logic [1] in any of the bits indicating that the respective output experienced a fault condition prior to the $\overline{\text{CS}}$ transition. Any bits clocked out of the SO pin after the first 16 will be representative of the initial message bits that were clocked into the SI pin since the $\overline{\text{CS}}$ pin first transitioned to a logic [0]. This feature is useful for daisy chaining devices as well as message verification.

Following a $\overline{\text{CS}}$ transition logic [0] to logic [1], the device determines if the message was of a valid length (a valid message length is one that is a multiple of 16 bits) and if so, latches the data into the appropriate registers. At this time, the SO pin is tri-stated and the fault status register is now able to accept new fault status information.

Table 10. Serial Output Bit Assignment

Bit Sig	SO Msg Bit	Message Bit Description
MSB	OD15	Reflects the state of the Watchdog bit from the previously clocked-in message.
	OD14	If OD15 is logic [0], then this bit will reflect the state of the direct input IHS0. If OD15 is logic [1], then this bit will reflect the state of IHS2.
	OD13	If OD15 is logic [0], then this bit will reflect the state of the direct input IHS1. If OD15 is logic [1], then this bit will reflect the state of IHS3.
	OD12	If OD15 is logic [0], then this bit will reflect the state of the input FSI. If OD15 is logic [1], then this bit will reflect the state of the input WAKE.
	OD11	Reports the absence or presence of a fault on LS11.
	OD10	Reports the absence or presence of a fault on LS10.
	OD9	Reports the absence or presence of a fault on LS9.
	OD8	Reports the absence or presence of a fault on LS8.
	OD7	Reports the absence or presence of a fault on LS7.
	OD6	Reports the absence or presence of a fault on LS6.

Table 10. Serial Output Bit Assignment (continued)

	OD5	Reports the absence or presence of a fault on LS5.
	OD4	Reports the absence or presence of a fault on LS4.
	OD3	Reports the absence or presence of a fault on HS3.
	OD2	Reports the absence or presence of a fault on HS2.
	OD1	Reports the absence or presence of a fault on HS1.
LSB	OD0	Reports the absence or presence of a fault on HS0.
LSB	OD0	Reports the absence or presence of a fault on HS0.

The MC33888 device reports the occurrence of the following faults via the output dedicated bits clocked out of the SO pin:

- Over voltage
- Open Load
- Over temperature

In the event of an occurrence of faults, the bits clocked out of the device will indicate the presence of a fault with a logic [1] on the output dedicated bit, prior to and since the last SPI communication, or at the time of the CSB pin going to logic [0]. Each type of fault can be differentiated from the others as follows:

OVER VOLTAGE

An over voltage occurrence can be inferred if all twelve bits representing each of the outputs are logic [1] at the same time.

OPEN LOAD

An open load condition is only detected when the output is off and the open load detection for the output of concern is enabled. The first SPI read after the output is commanded on will clear the fault bit for this output.

OVER TEMPERATURE

An over temperature condition is indicated and latched into the fault register if the output is on and the indicating output experienced an over temperature event since the last SPI write. Each output has a dedicated temperature sensor. The high side drivers will turn off after the over temperature shutdown level is reached until the temperature falls below the specified hysteresis level and then will turn back on automatically, unless the output has been commanded off. In either case, a fault indication for the faulted output will be present for the next SPI read.

CURRENT LIMIT

An output which current limits will not indicate a fault unless the limitation results in enough power dissipation to increase the temperature of the limiting transistor to its over temperature shutdown level.

Each of these faults are indicated real time by the FLTB pin, which could be used as an initial indication of the presence of a fault within the device. Determining the actual faulted output would requires an analysis of the fault bits provided by the device via the SO pin.

Note that the very first SPI read after the battery falls below 6V may not be correct, if the VDD remained in specification and a reset was not generated by the MCU.

PROTECTION AND DIAGNOSTIC FEATURES

REVERSE BATTERY REQUIREMENTS

The low-side and high-side outputs survive the application of reverse battery as low as -16 V.

GROUND DISCONNECT PROTECTION

In the event that the 33888 ground is disconnected from load ground, the device protects itself and safely turns OFF the outputs, regardless of the state of the output at the time of disconnection.

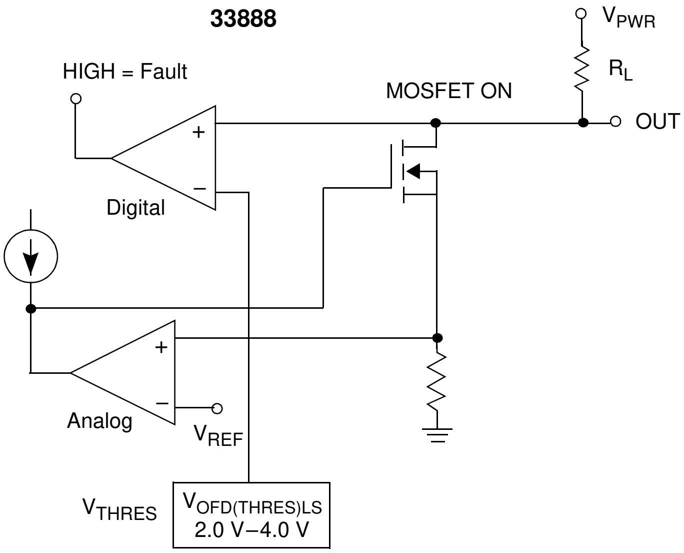


Figure 10. Low-Side Short Circuit Detection and Analog Current Limit

UNDERVOLTAGE SHUTDOWN REQUIREMENTS

All outputs turn off at some battery voltage below 6.0 V; For the A version, the low side shutdown at a lower value, V_{PWRUV}. however, as long as the level stays above 5.0 V, the internal logic states within the device are designed to be sustained. This ensures that when the battery level then rises above 6.0 V, the device will return to the state that it was in prior to the excursion between 5.0 V and 6.0 V (assuming that there was no SPI communication or direct input changes during the event). If the battery voltage falls to a level below 5.0 V, then the internal logic is re initialized and the device is then in the default state upon the return of levels in excess of 6.0 V.

OUTPUT VOLTAGE CLAMPING

Each output has an internal clamp to provide protection and dissipate the energy stored in inductive loads. Each clamp independently limits the drain-to-source voltage to the range specified in the Power Outputs section of Table 5, Static Electrical Characteristics beginning on page 10. Also see Figure 11.

If the VPWR supply is disconnected, no issue exists for resistive or capacitive loads, but additional protection circuitry is required for the device to support a battery disconnect for an inductive load connected to HS pins.

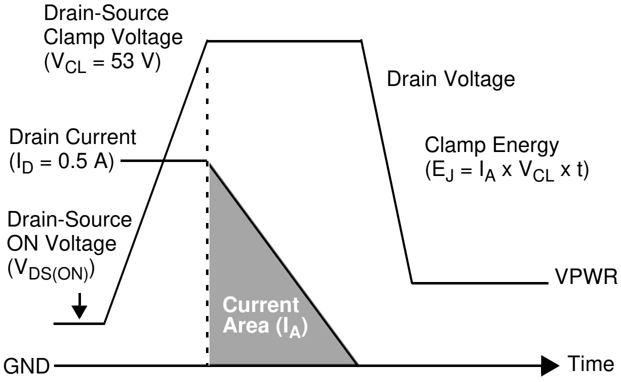
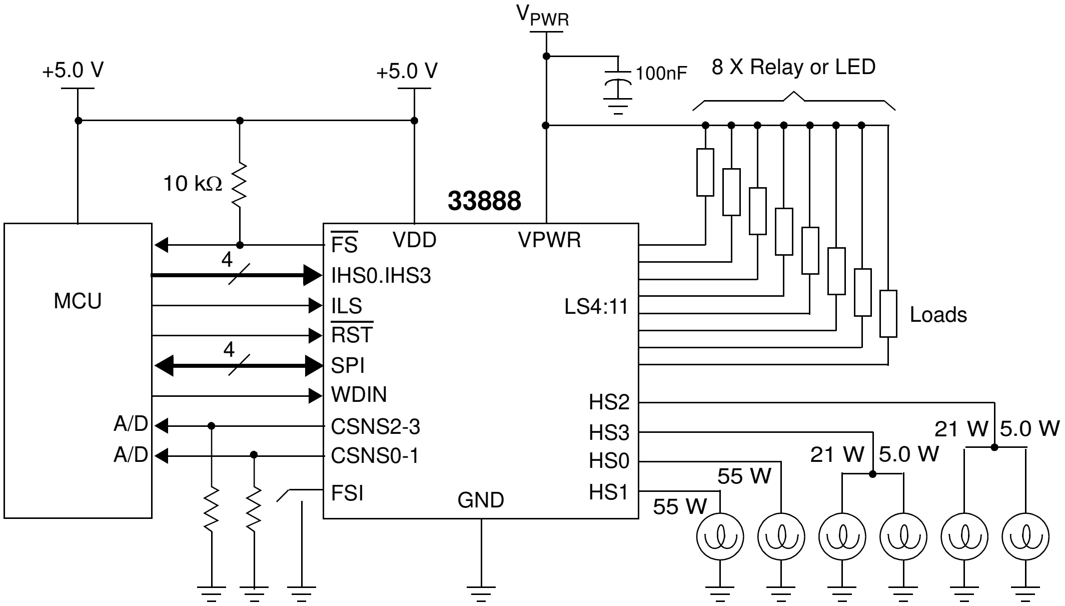


Figure 11. Low-Side Output Voltage Clamping

TYPICAL APPLICATIONS

Figure 12 shows a typical lighting application for the 33888. 55W bulb driven with 10 milliohm outputs, and 21W plus 5W lamps with 40 milliohm outputs.

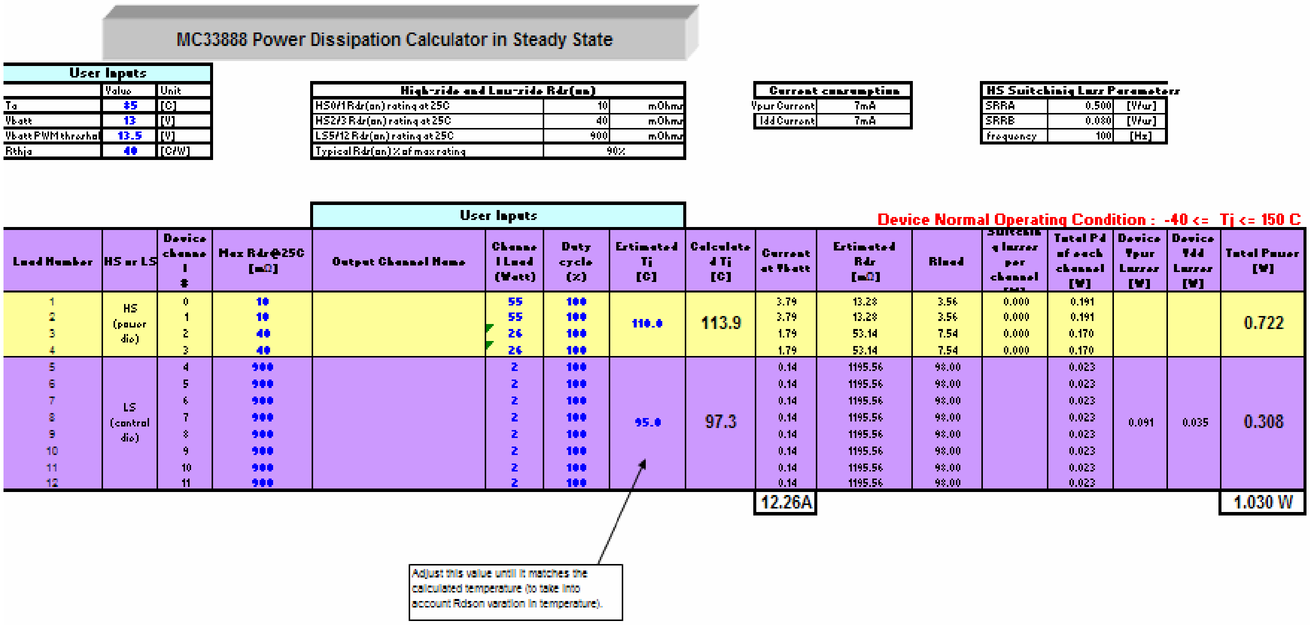


V_{PWR}
+5.0 V
+5.0 V
100nF
8 X Relay or LED
10 kΩ
33888
MCU
FS
VDD
VPWR
4
IHS0.IHS3
ILS
RST
4
SPI
WDIN
A/D
CSNS2-3
A/D
CSNS0-1
FSI
GND
LS4:11
Loads
HS2
HS3
HS0
HS1
21 W
5.0 W
21 W
5.0 W
55 W
55 W

Figure 12. 33888 Typical Application Diagram

An excel tool has been created to calculate the dissipated power and the junction temperature knowing the application conditions in steady state, as shown in Figure 13.

The parameters to enter concern the loads (bulbs only considered) and the board. They are VPWR, loads (in Watts), PWM frequency, ambient temperature and thermal impedance. The calculations are done with a $R_{DS(ON)}$ at an estimated junction temperature. The current is also considered constant in the loads.



MC33888 Power Dissipation Calculator in Steady State

User Inputs	Value	Unit
Ta	85	[C]
Vbatt	13	[V]
Vbatt PWM threshol	13.5	[V]
Rthja	40	[C/W]

High-side and Low-side Rds(on)		
HS0/1 Rds(on) rating at 25C	10	mOhms
HS2/3 Rds(on) rating at 25C	40	mOhms
LS5/12 Rds(on) rating at 25C	900	mOhms
Typical Rds(on) % of max rating	90%	

Current consumption	
Vpwr Current	7mA
Idd Current	7mA

HS Switching Loss Parameters		
SRRA	0.500	[V/us]
SRRB	0.080	[V/us]
frequency	100	[Hz]

User Inputs

Device Normal Operating Condition : -40 <= Tj <= 150 C

Load Number	HS or LS	Device channel #	Max Rds@25C [mΩ]	Output Channel Name	Channel Load (Watt)	Duty cycle (%)	Estimated Tj [C]	Calculated Tj [C]	Current at Vbatt	Estimated Rds [mΩ]	Rload	Switching losses per channel	Total Pd of each channel [W]	Device Vpwr Losses [W]	Device Vdd Losses [W]	Total Power [W]
1	HS (power dio)	0	10		55	100	110.0	113.9	3.79	13.28	3.56	0.000	0.191			0.722
2		1	10		55	100			3.79	13.28	3.56	0.000	0.191			
3		2	40		26	100			1.79	53.14	7.54	0.000	0.170			
4		3	40		26	100			1.79	53.14	7.54	0.000	0.170			
5	LS (control dio)	4	900		2	100	95.0	97.3	0.14	1195.56	98.00		0.023	0.091	0.035	0.308
6		5	900		2	100			0.14	1195.56	98.00		0.023			
7		6	900		2	100			0.14	1195.56	98.00		0.023			
8		7	900		2	100			0.14	1195.56	98.00		0.023			
9		8	900		2	100			0.14	1195.56	98.00		0.023			
10		9	900		2	100			0.14	1195.56	98.00		0.023			
11		10	900		2	100			0.14	1195.56	98.00		0.023			
12		11	900		2	100			0.14	1195.56	98.00		0.023			
									12.26A							1.030 W

Adjust this value until it matches the calculated temperature (to take into account Rdson variation in temperature).

Figure 13. Figure 13 – MC33888 power dissipation calculator

Automotive lamps do not tolerate high voltages very well. Tests of a few lamps indicated that failures can occur when 18V is applied for a few seconds. Consequently, PWM switching allows to reduce the effective RMS voltage in order to drive bulbs safety. The “Vbatt PWM” threshold determines the transition between the fully-on and PWMing modes.

For example, to maintain the power dissipation associated with a 13V battery at 100% duty cycle, the duty cycle would be adjusted to $(13/18)^2$, or 52%, when the battery is at 18V.

The loads must be chosen in order to guarantee the device normal operating condition as junction temperature from -40 to 150 °C. In case of permanent current limitation conditions, the duration and number of activation cycles must be limited with a dedicated MCU fault management using the fault reporting through SPI.

SHAFFNER TESTS

The MC33888 device is protected in case of positive and negative transients on VPWR and the output lines (HS[0:3] and LS[4:11]) per ISO 7637-2 standard.

The following characterization has been done without decoupling capacitors and for HS1 resistive load=2.5Ω and HS3 resistive load=3Ω.

Table 11. Results of Fast Transient Pulses on VPWR

Pulses on VPWR	HS1 & 3 ON state loaded	HS1 & 3 ON state open load	HS1 & 3 OFF state loaded	HS1 & 3 OFF state open load
Pulse 1 Ri = 10Ω 5000 occurrences	PASS: -100V	PASS : -40V, FAIL : -50V	PASS: -100V	PASS : -40V, FAIL: -50V
Pulse 2a Ri = 2Ω 5000 occurrences	PASS: +50V	PASS: +42V , FAIL: +50V	PASS: +50V	PASS: +50V
Pulse 3a Ri = 50Ω Duration 1 hour	PASS: -150V	PASS: -150V	PASS: -150V	PASS: -150V
Pulse 3b Ri = 50Ω Duration: 1 hour	PASS: +100V	PASS: +100V	PASS: +100V	PASS: +100V
Pulse 5a Ri = 2Ω (Load dump) 50 pulses	PASS: +42V	PASS: +42V	PASS: +42V	PASS: +42V
Pulse 5b Ri = 2Ω (Load dump) 50 pulses	PASS: +42V	PASS: +42V	PASS: +42V	PASS: +42V

Table 12. Rating of Fast Transient Pulses on VPWR

Test Pulse	Test Level	Rate	Nb of pulses or test time	Comment
1	-100V	D	5000 for each config	Failure in case of openload condition
1	-40V	A	5000 for each config	/
2A	+50V	D	5000 for each config	Failure in case of openload condition for high-side 'on'
2A	+42V	A	5000 for each config	/
3A	-150V	A	1h for each config	/
3B	+100V	A	1h for each config	/
5A	+42V	A	50 for each config	When outputs are on, the load dump reset it
5B	+42v Clamped	A	50 for each config	When outputs are on, the load dump reset it

Rate signification:

A: Device fully operational after test without any degradation.

B: One or more function is (are) unavailable during the test and good after

C: One or more function is (are) unavailable during the test and after it.

D: Device's damaged.

Pulse on one output while others are open:

Table 13. Results of Fast Transient Pulses on HS1 and HS3

Pulse on high-side output	HS1	HS3
Pulse 1 Ri = 10Ω, 5000 occurrences	PASS: -100 V	PASS: -100 V

Table 14. Results of Fast Transient Pulses on LS4 and LS5

Pulse on low-side output	LS4	LS5
Pulse 2a Ri = 2Ω, 5000 occurrences	PASS: +50 V	PASS: +50 V

Table 15. Rating of Fast Transient Pulses on HS1, HS3, LS4, and LS5

Test pulse	Test Level	Rate	Nb of pulses or test time	Comment
1	-100V	A	5000 for each config	/
2A	+50V	A	5000 for each config	/

Rate signification:

A: Device fully operational after test without any degradation.

B: One or more function is (are) unavailable during the test and good after

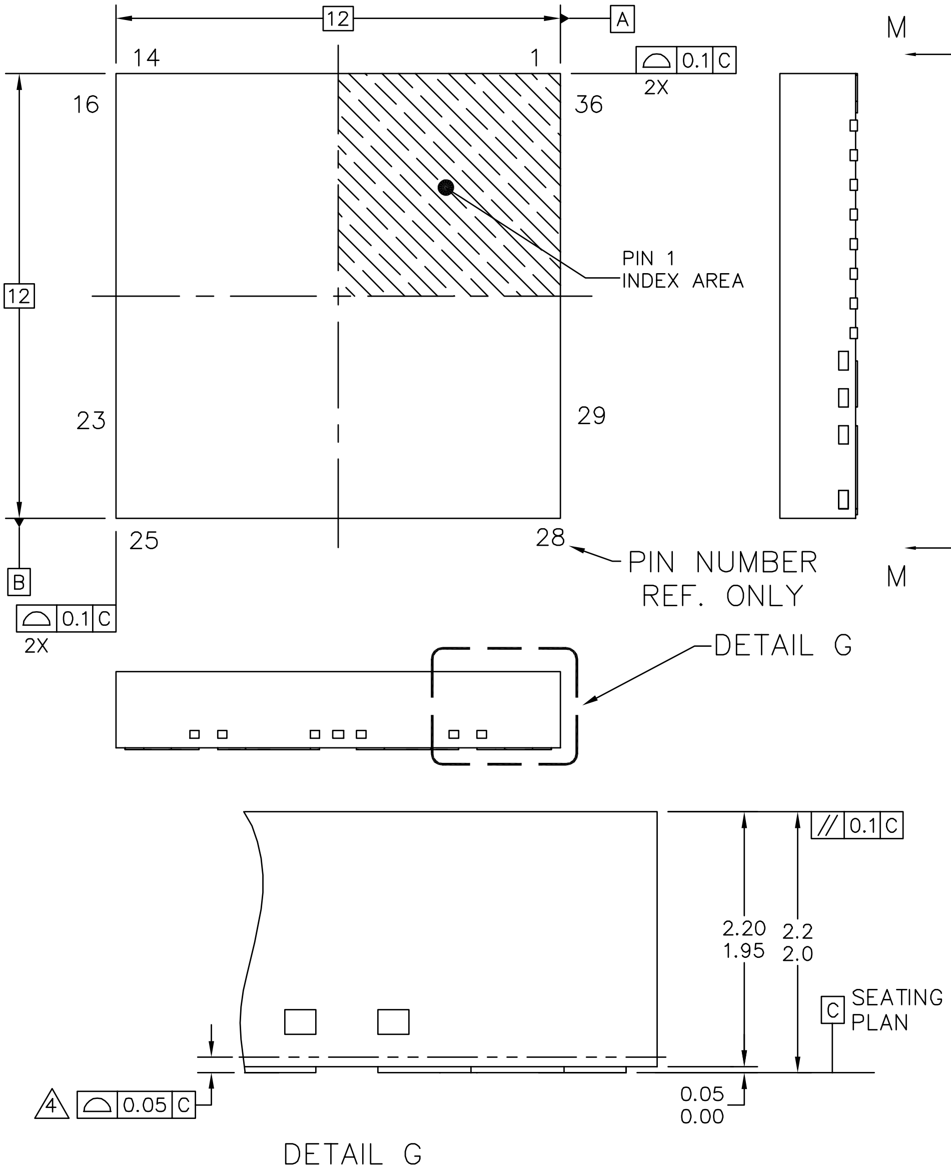
C: One or more function is (are) unavailable during the test and after it.

D: Device's damaged.

PACKAGING

PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” listed below.


12
A
14
1
0.1 C
2X
M
16
36
PIN 1
INDEX AREA
12
23
29
25
28
PIN NUMBER
REF. ONLY
M
B
0.1 C
2X
DETAIL G
0.1 C
2.20
1.95
2.2
2.0
C
SEATING
PLAN
4
0.05 C
0.05
0.00
DETAIL G

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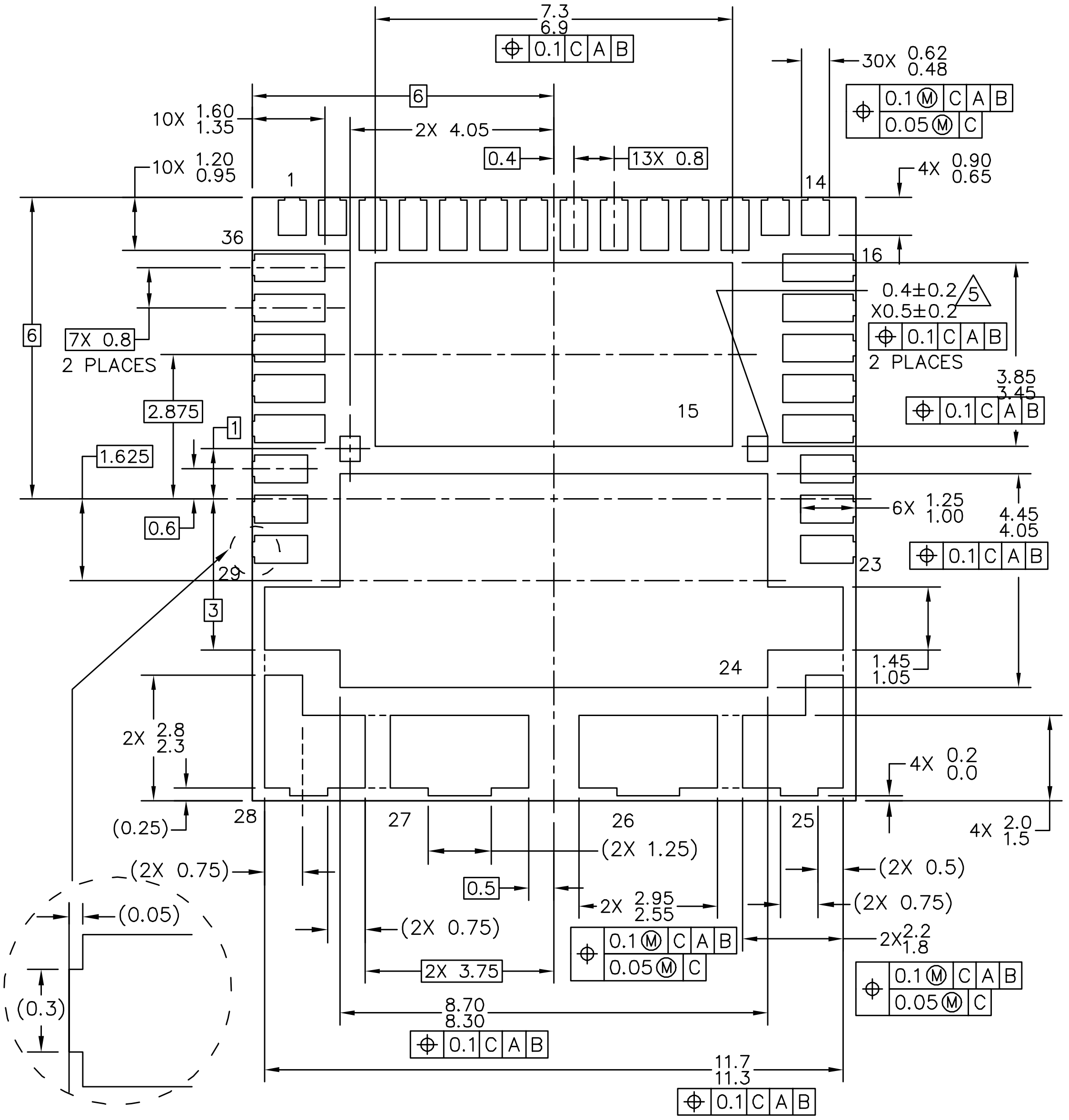
TITLE: POWER QUAD FLAT NON–LEADED PACKAGE (PWR QFN) 36 TERMINAL, 0.8 PITCH(12X12X2.1)	DOCUMENT NO: 98ARL10544D	REV: E
	CASE NUMBER: 1438–06	14 MAR 2005
	STANDARD: NON–JEDEC	

PNB SUFFIX
APNB SUFFIX
36-PIN
NON-LEADED PACKAGE
98ARL10544D
ISSUE E


7.3
6.9
⌖ 0.1 C A B
30X 0.62 0.48
⌖ 0.1 Ⓜ C A B
0.05 Ⓜ C
6
10X 1.60 1.35
2X 4.05
0.4
13X 0.8
10X 1.20 0.95
1
14
4X 0.90 0.65
36
16
0.4±0.2 5
X0.5±0.2
⌖ 0.1 C A B
2 PLACES
6
7X 0.8
2 PLACES
3.85
3.45
⌖ 0.1 C A B
15
2.875
1
1.625
6X 1.25 1.00
4.45
4.05
⌖ 0.1 C A B
0.6
29
23
3
1.45
1.05
24
2X 2.8 2.3
4X 0.2 0.0
(0.25)
28
27
26
25
4X 2.0 1.5
(2X 1.25)
(2X 0.75)
(2X 0.5)
0.5
(0.05)
2X 2.95 2.55
(2X 0.75)
(2X 0.75)
⌖ 0.1 Ⓜ C A B
0.05 Ⓜ C
2X 2.2 1.8
⌖ 0.1 Ⓜ C A B
0.05 Ⓜ C
(0.3)
2X 3.75
8.70
8.30
⌖ 0.1 C A B
11.7
11.3
⌖ 0.1 C A B

VIEW M–M

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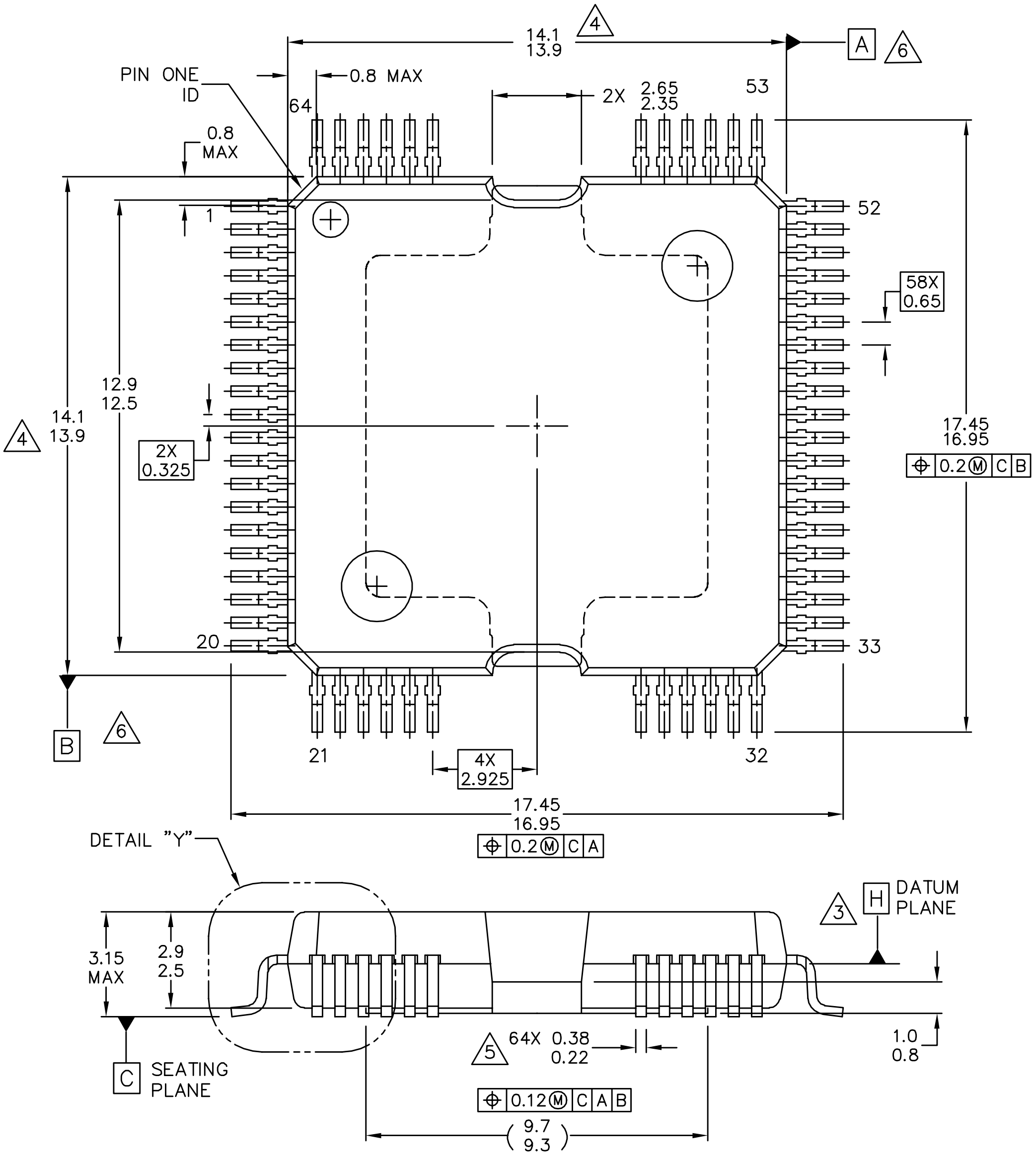
PNB SUFFIX
APNB SUFFIX
36-PIN
NON-LEADED PACKAGE
98ARL10544D
ISSUE E


14.1
13.9
4
A
6
PIN ONE
ID
0.8 MAX
64
2X 2.65
2.35
53
0.8
MAX
1
52
58X
0.65
12.9
12.5
14.1
13.9
4
2X
0.325
17.45
16.95
0.2 Ⓜ C B
20
33
B
6
21
4X
2.925
32
17.45
16.95
0.2 Ⓜ C A
DETAIL "Y"
3
H
DATUM
PLANE
3.15
MAX
2.9
2.5
C
SEATING
PLANE
5
64X 0.38
0.22
1.0
0.8
0.12 Ⓜ C A B
9.7
9.3

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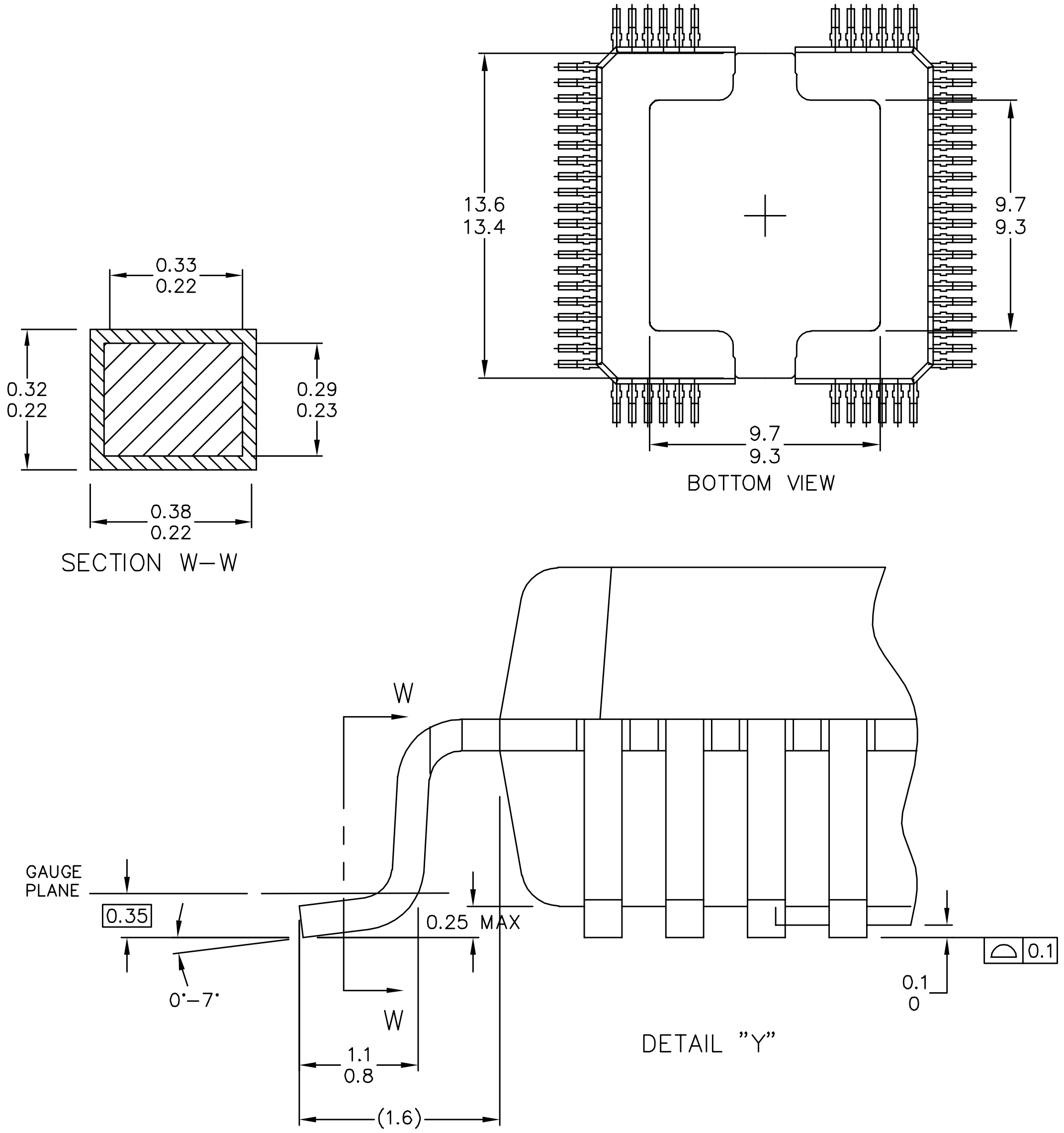
TITLE: 64 LEAD POWER QFP	DOCUMENT NO: 98ARH99043A	REV: D
	CASE NUMBER: 1315–03	23 MAY 2005
	STANDARD: JEDEC MO–188	

FB SUFFIX
64-PIN
PLASTIC PACKAGE
98ARH99043A
ISSUE D


0.33
0.22
0.32
0.22
0.29
0.23
0.38
0.22
SECTION W–W
13.6
13.4
9.7
9.3
9.7
9.3
BOTTOM VIEW
W
GAUGE PLANE
0.35
0.25 MAX
0°–7°
0.1
0.1
0
W
1.1
0.8
(1.6)
DETAIL "Y"

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TITLE: 64 LEAD POWER QFP	DOCUMENT NO: 98ARH99043A	REV: D
	CASE NUMBER: 1315–03	23 MAY 2005
	STANDARD: JEDEC MO–188	

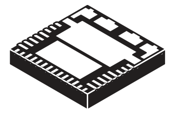
FB SUFFIX
64-PIN
PLASTIC PACKAGE
98ARH99043A
ISSUE D

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 2.0)

33888PNB

36-PIN PQFN



PNB SUFFIX
98ARL10544D
36-PIN PQFN
14 mm x 14 mm

Note For package dimensions, refer to the 33888 device data sheet.

Introduction

This thermal addendum is provided as a supplement to the MC33888 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

Packaging and Thermal Considerations

This package is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R\theta_{JAmn}$.

For *m*, *n* = 1, $R\theta_{JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R\theta_{JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R\theta_{J21}$ and $R\theta_{J22,}$ respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

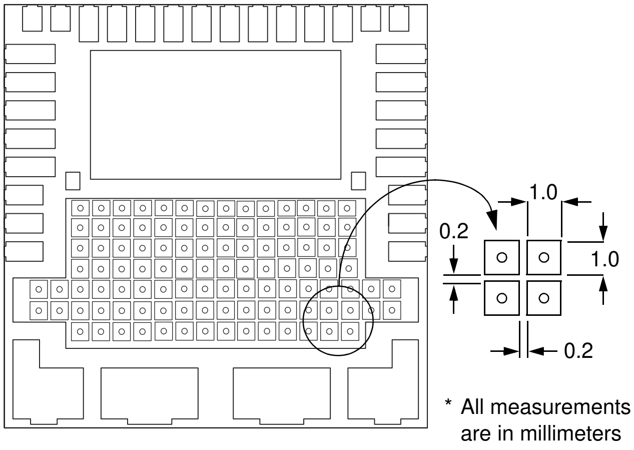
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 16. Thermal Performance Comparison

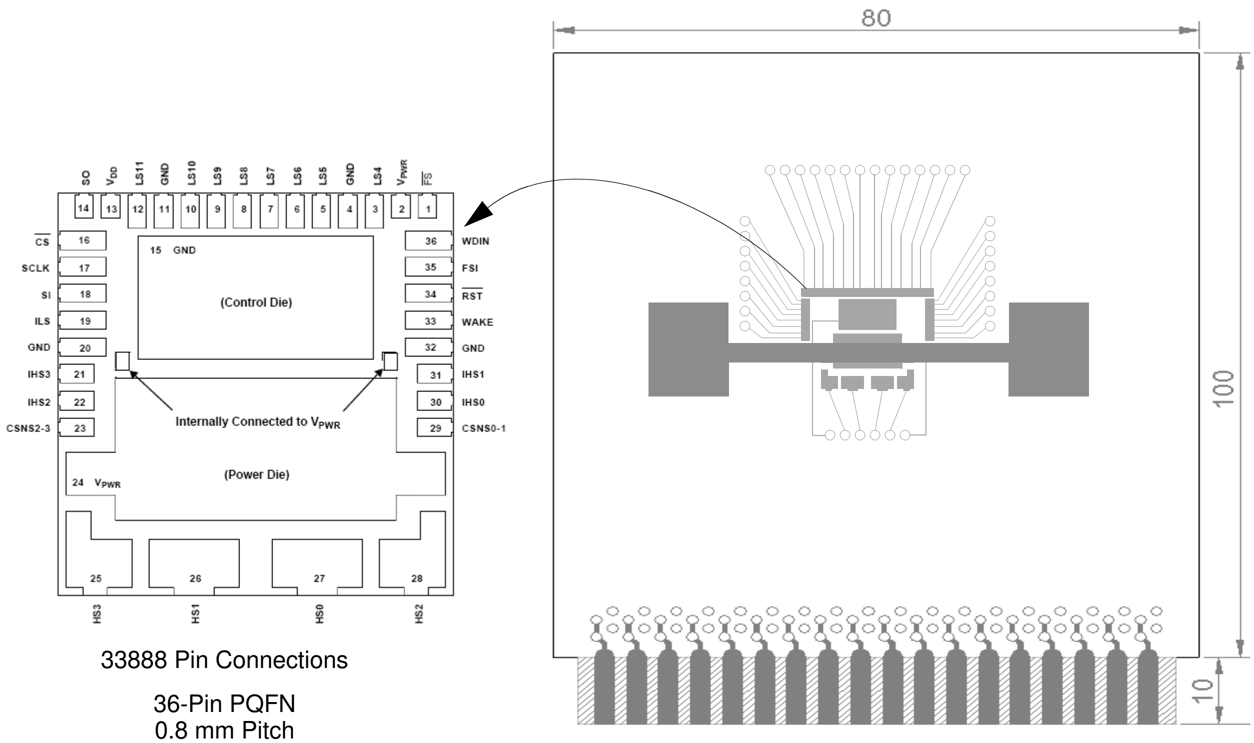
Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	***m* = 1, *n* = 1**	***m* = 1, *n* = 2** ***m* = 2, *n* = 1**	***m* = 2, *n* = 2**
$P_{\theta JAmn}$ (1), (2)	19	18	20
$P_{\theta JAmn}$ (1), (2)	6.0	5.0	6.0
$P_{\theta JAmn}$ (1), (2)	37	36	37
$P_{\theta JAmn}$ (1), (2)	<1	0	1

Notes
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



Note: Recommended via diameter is 0.5 mm. PTH (plated through hole) via must be plugged / filled with epoxy or solder mask in order to minimize void formation and to avoid any solder wicking into the via.

Figure 14. Surface Mount for Power PQFN with Exposed Pads


SO
VDD
LS11
GND
LS10
LS9
LS8
LS7
LS6
LS5
GND
LS4
VPWR
FS
14
13
12
11
10
9
8
7
6
5
4
3
2
1
CS
SCLK
SI
ILS
GND
IHS3
IHS2
CSNS2-3
16
17
18
19
20
21
22
23
15 GND
(Control Die)
Internally Connected to VPWR
24 VPWR
(Power Die)
36
35
34
33
32
31
30
29
WDIN
FSI
RST
WAKE
GND
IHS1
IHS0
CSNS0-1
25
26
27
28
HS3
HS1
HS0
HS2
80
100
10

33888 Pin Connections

36-Pin PQFN
0.8 mm Pitch
12.0 mm x 12.0 mm Body

Figure 15. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area A:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 17. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m = 1, *n* = 1	*m* = 1, *n* = 2 *m* = 2, *n* = 1	*m* = 2, *n* = 2
$P\theta_{JAmn}$	0	37	36	37
	300	29	29	30
	600	28	27	29

$P\theta_{JA}$ is the thermal resistance between die junction and ambient air.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

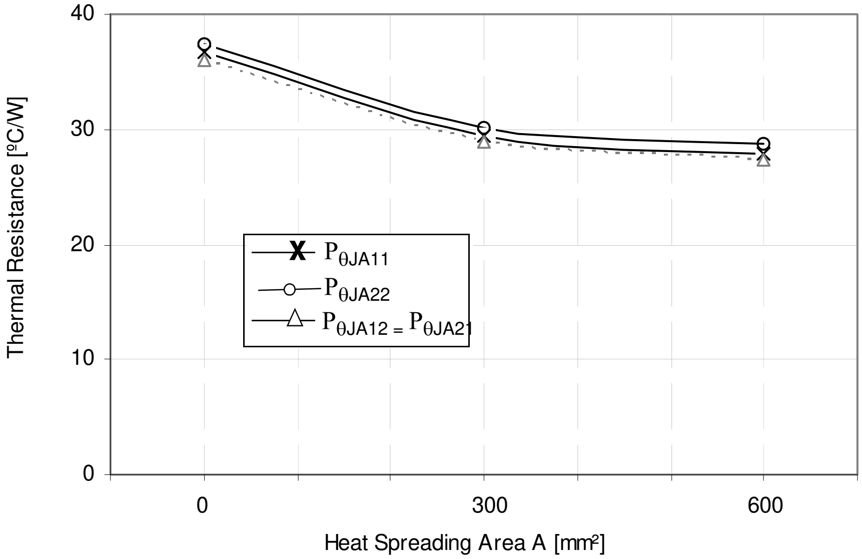


Figure 16. Device on Thermal Test Board $R\theta_{JA}$

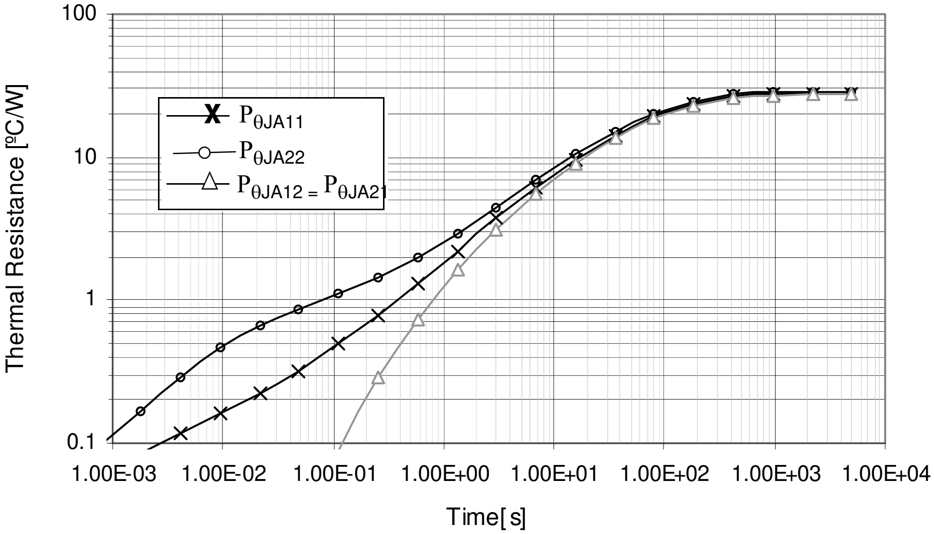


Figure 17. Transient Thermal Resistance $P\theta_{JA}$,
1W Step Response, Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

REVISION	DATE	DESCRIPTION OF CHANGES
5.0	7/2006	• Implemented Revision History page • Converted to Freescale format and updated to the prevailing form and style • Added Thermal Addendum • Added last sentence to Open Load Fault on page 21 • Added Fault Reporting Description, following Table 10. Serial Output Bit Assignment on page 25 • Made numerous changes and description additions to Typical Applications on page 28
6.0	2/2007	• Removed Part Number MC33888PNB/R2 from Ordering Information Block on page 1. • Added Shaffner information and tables to the Typical Applications section of the data sheet, beginning on page 28. • Added titles to Table 11 - Results of Fast Transient Pulses on VPWR on page 29, Table 12 - Rating of Fast Transient Pulses on VPWR on page 30, Table 13 - Results of Fast Transient Pulses on HS1 and HS3 on page 30, Table 14 - Results of Fast Transient Pulses on LS4 and LS5 on page 30, and Table 15 - Rating of Fast Transient Pulses on HS1, HS3, LS4, and LS5 on page 30 • Removed Peak Package Reflow Temperature During Reflow (solder reflow) parameter from Maximum Ratings table on page 9. Added note with instructions from www.freescale.com.

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2/2007