

# Using the TPS84320EVM-692, TPS84620EVM-692 and TPS84621EVM-692

## User's Guide



Literature Number: SLVU415A

August 2011

# **TPS84320EVM-692, TPS84620EVM-692 and TPS84621EVM-692 Integrated Power Solution Evaluation Module**

This user's guide contains background information for the TPS84620/621/320 and support documentation for the TPS84320EVM-692, TPS84620EVM-692 and TPS84621EVM-692 evaluation module (TPS84x2xEVM-692).

## **1 Introduction**

The TPS84620 integrated power solution is designed to provide up to a 6-A output. The TPS84620 contains dual-voltage inputs for the power stage and control circuitry. The power stage input (PVIN) is rated for 1.6 V to 14.5 V whereas the control input (VIN) is rated for 4.5 V to 14.5 V. The TPS84x2xEVM-692 provides both inputs but is designed and tested with PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in [Table 1](#).

### **1.1 Features**

- Complete Integrated Power Solution Allows Small Footprint, Low-Profile Design
- Efficiencies Up To 96%
- Wide-Output Voltage Adjust 1.2 V to 5.5 V, with 1% Reference Accuracy
- Adjustable Switching Frequency

### **1.2 Applications**

- Broadband and Communications Infrastructure
- Automated Test and Medical Equipment
- Compact PCI/PCI Express/PXI Express
- DSP and FPGA Point-of-Load Applications

### **1.3 Background**

This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS84320/620/621 regulator. The TPS84x2xEVM-692 default output voltage is 3.3 V at a 630-kHz switching frequency. The high-side and low-side MOSFETs are incorporated inside the TPS84320/620/621 package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS84320/620/621 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are internal to the TPS84320/620/621, and external resistors and jumpers allow for adjustable output voltage and frequency adjustment. Additionally, the TPS84320/620/621 provides adjustable slow start, tracking, and undervoltage lockout inputs. The absolute maximum input voltage is 15 V for the TPS84x2xEVM-692.

**Table 1. Input Voltage and Output Current Summary**

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS84320EVM-692	PVIN = VIN = 8 V to 14.5 V	0 A to 6 A
TPS84620EVM-692	PVIN = VIN = 4.5 V to 14.5 V	0 A to 3 A
TPS84621EVM-692	PVIN = VIN = 8 V to 14.5 V	0 A to 6 A

## 2 Electrical Characteristics

A summary of the TPS84620EVM-692 performance specifications is provided in [Table 2](#). Specifications are given for an input voltage of 12 V and an output voltage of 3.3 V, unless otherwise specified. The ambient temperature is 25°C for all measurements, unless otherwise noted.

**Table 2. TPS84620EVM-692 Electrical and Performance Specification**

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
Output Voltage	8 V ≤ PVIN = VIN ≤ 14.5 V, ILOAD ≤ ILOAD (max)	5 V	4.925	5.00	5.075	Volts
		3.3 V	3.250	3.30	3.350	
		2.5 V	2.462	2.50	2.538	
		1.8 V	1.773	1.80	1.827	
		1.5 V	1.477	1.50	1.523	
		1.2 V	1.182	1.20	1.218	
Output Current	8 V ≤ PVIN = VIN ≤ 14.5 V		–	–	6.0	Amps
Output ripple voltage, peak-to-peak	PVIN = VIN = 12 V, ILOAD = 6 A	5 V	–	12	–	mV
		3.3 V				
		2.5 V				
		1.8 V				
		1.5 V				
		1.2 V				
Switching frequency	PVIN = VIN = 12 V, ILOAD = 6 A	5 V		780		kHz
		3.3 V		780		
		3.3 V		630		
		2.5 V		630		
		2.5 V		530		
		1.8 V		630		
		1.8 V		480		
		1.5 V		630		
		1.5 V		480		
		1.2 V		580		
	1.2 V	480				
Efficiency, end-to-end	ILOAD = 6 A PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V PVIN = VIN = 5 V PVIN = VIN = 12 V	5 V, 780 kHz		91%		
		3.3 V, 780 kHz		89%		
		3.3 V, 630 kHz		88%		
		2.5 V, 630 kHz		87%		
		2.5 V, 480 kHz		86%		
		1.8 V, 630 kHz		83%		
		1.8 V, 480 kHz		82%		
		1.5 V, 630 kHz		81%		
		1.5 V, 480 kHz		80%		
		1.2 V, 580 kHz		79%		
		1.2 V, 480 kHz		78%		
		Line Regulation				
Load Regulation				±0.1%		
Load Transient Deviation	1 A/μs load step 50% to 100% ILOAD			60		mV
Load Transient Recovery Time	1 A/μs load step 50% to 100% ILOAD			80		μs
Operating Temperature			–40		85	°C
Slow Start				4		ms
Tracking			0 to 1.2	0 to 1.8	0 to 5	V
Synchronization			480		780	kHz

3 Schematic

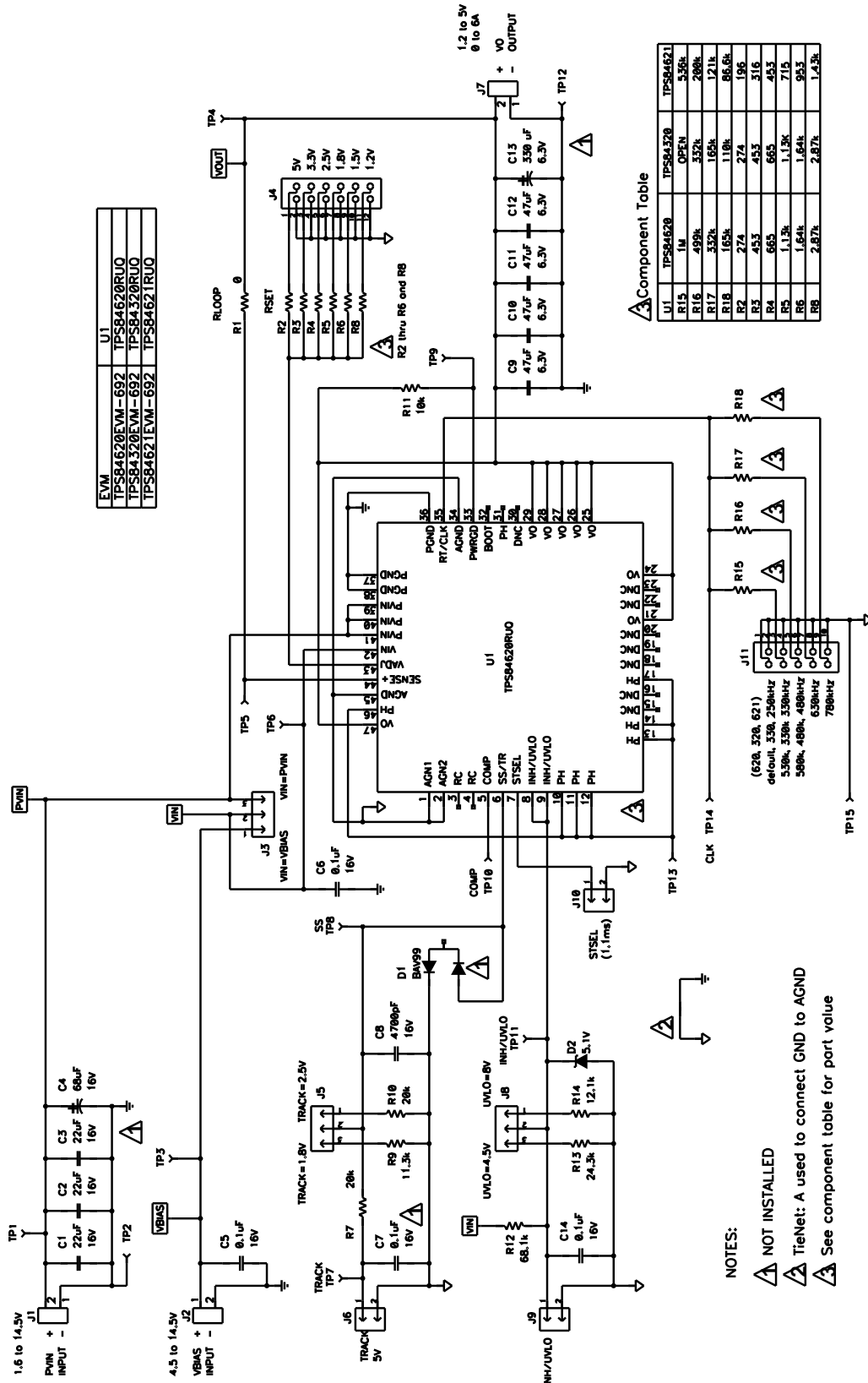


Figure 1. TPS84x2xEVM-692 Schematic

## 4 Modifications

These evaluation modules are designed to provide access to the features of the TPS84320/620/621. Some modifications can be made to these modules.

### 4.1 Output Voltage Setpoint

Select the output voltage at J4. Use the silk screen to select the desired voltage preprogrammed on the module (see [Figure 13](#). If a different voltage is needed, the RSET resistor (any of R2 thru R6 and R8) may be changed to a value listed in the component data sheet ([TPS84620](#), [TPS84621](#) and [TPS84320](#)).

When all jumpers on J4 are open, the default output voltage for the components is selected. See [Table 3](#).

**Table 3. Component Default Output Voltage**

COMPONENT	DEFAULT VOLTAGE
TPS84620	NA, No Default Voltage
TPS84320	0.8 V
TPS84621	0.6 V

### 4.2 Frequency Select

The Switching frequency is selected at J11. [Table 4](#) shows the selection options for each of the three evaluation modules.

**Table 4. Selection Options**

JUMPER POSITION	TPS84620EVM-692	TPS84320EVM-692	TPS84621EVM-692
MIN	480 kHz	330 kHz	250 kHz
1	530 kHz	330 kHz	330 kHz
2	580 kHz	480 kHz	480 kHz
3	630 kHz	630 kHz	630 kHz
MAX	780 kHz	780 kHz	780 kHz

### 4.3 Slow Start Time

The slow start time can be adjusted by changing the value of C8. See the slow start table in the ([TPS84620](#), TPS84621 and TPS84320 data sheets for more information. The EVM is set for a slow start time of 2.8 ms (C8 = 4700 pF and J10 installed).

### 4.4 Track In

The TPS84320/620/621 can track an external voltage during start-up. The J6 connector is provided to allow connection to an external voltage. Ratio-metric or simultaneous tracking can be implemented using the provided resistor dividers with J5. See the ([TPS84620](#), TPS84621 and TPS84320 data sheets for details.

### 4.5 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted as described in the ([TPS84620](#), TPS84621 and TPS84320 data sheets. The EVM provides two selectable UVLO setpoints using the provided resistor dividers and J8. J9 provides an inhibit input.

### 4.6 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected using a jumper across J3 pins 2 and 3 (VIN = PVIN position). The single input voltage is supplied at J1. If desired, input voltage may be separated by moving the J3 jumper to pins 1 and 2 (VIN = VBIAS position). Dual input voltages must then be provided at both J1 and J2.

## 5 Test Setup

This section describes how to properly connect, set up, and use the TPS84x2xEVM-692 evaluation module.

### 5.1 Input/Output Connections

The TPS84x2xEVM-692 is provided with input/output connectors and test points as shown in [Table 5](#). A power supply capable of supplying 4 A must be connected to J1 through a pair of 20 AWG wires. The jumper across J3 must be in place. See [Section 4.6](#) for split input voltage rail operation. The load must be connected to J7 through a pair of 20 AWG wires. The maximum load current capability must be 6 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the  $V_{IN}$  input voltages with TP2 providing a convenient ground reference. TP4 is used to monitor the output voltage with TP12 as the ground reference.

**Table 5. EVM Connectors and Test Points**

REF DES	LABEL	DESCRIPTION
J1	PVIN	Primary VIN connector
J2	VBIAS	VBIAS input voltage input connector
J3	VIN	Jumper used to connect VIN to PVIN. EVM default setting connects VIN to PVIN.
J7	VOUT	VOUT connector
J4	VADJ	VOUT selection. Default VOUT is 3.3 V.
J11	FREQ	Switching frequency selection. Default frequency is 630 kHz.
J6	TR_IN	TRACK IN connector. J5 provides two divider settings.
J5	SS_TR	Track voltage select jumper. Used with J6.
J9	INH_UVLO	Enable jumper. Install shunt to inhibit the power supply.
J8	INH_UVLO	Selects UVLO for power supply turn on. Default setting is for 8-V UVLO.
J10	STSEL	Internal slow start select jumper. Install shunt for internal slow start.
TP1	PVIN	PVIN circuit point
TP3	VBIAS	VBIAS circuit point
TP6	VIN	VIN circuit point
TP4	VOUT	VOUT circuit point
TP2, TP12	GND	Power grounds
TP15	AGND	Analog ground
TP7	TR_IN	Track input
TP8	SS_TR	Tracking input after divider
TP9	PWRGD	Power good status
TP14	RT/CLK	SYNC input
TP10	COMP	Error amplifier output
TP13	PH	Switch node
TP11	INH_UVLO	Inhibit and UVLO input
TP5	SENSE+	VOUT remote sense node connected to J7 pin 2. TP5 can be used for measuring the loop response along with changing R1 to 49.9 $\Omega$ .

## 6 Typical Performance Data

Figure 2 through Figure 12 present characteristic performance data taken from the TPS84620EVM-692 only. For data regarding the TPS84320EVM-692 and the TPS84621EVM-692 please see the TPS84320 and TPS84621 data sheet.

### 6.1 Efficiency vs Input Voltage

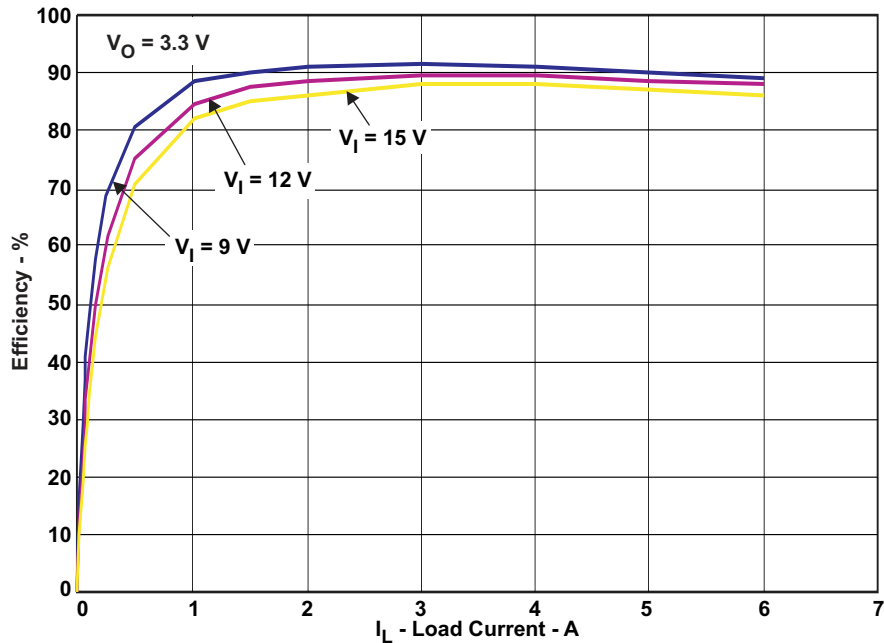


Figure 2. Efficiency vs Voltage at 25°C

### 6.2 Light-Load Efficiency vs Input Voltage

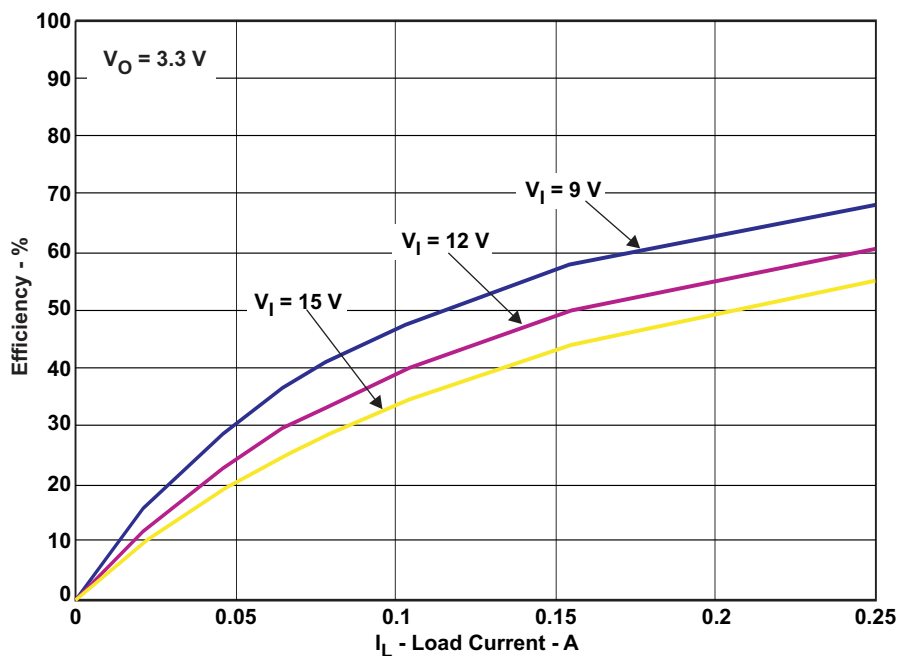


Figure 3. Light-Load Efficiency vs Input Voltage at 25°C



### 6.3 Efficiency vs Output Voltage/Frequency, $P_{VIN} = 12\text{ V}$

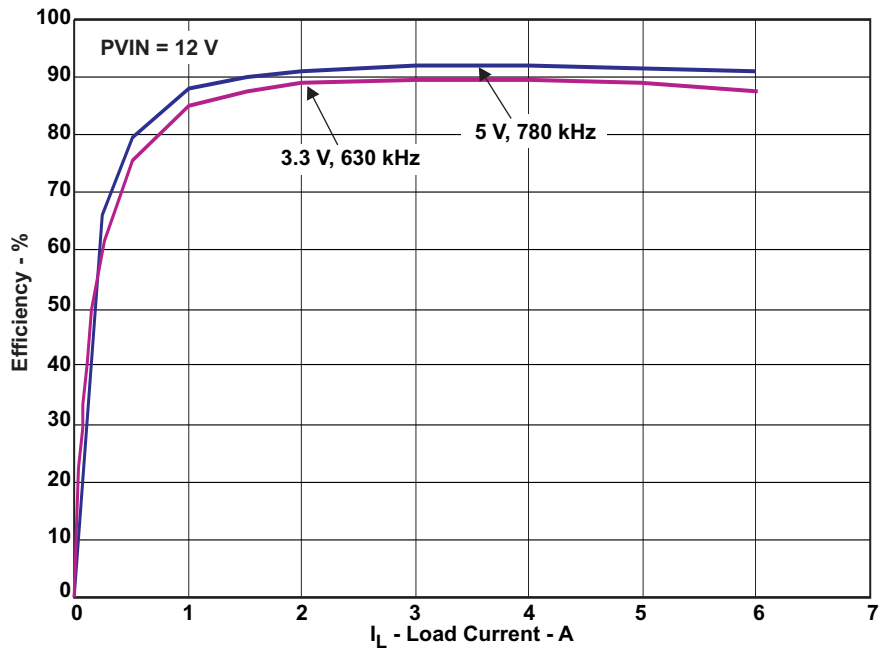


Figure 4. Efficiency vs Output Voltage at 25°C

### 6.4 Efficiency vs Output Voltage/Frequency, $P_{VIN} = 5\text{ V}$

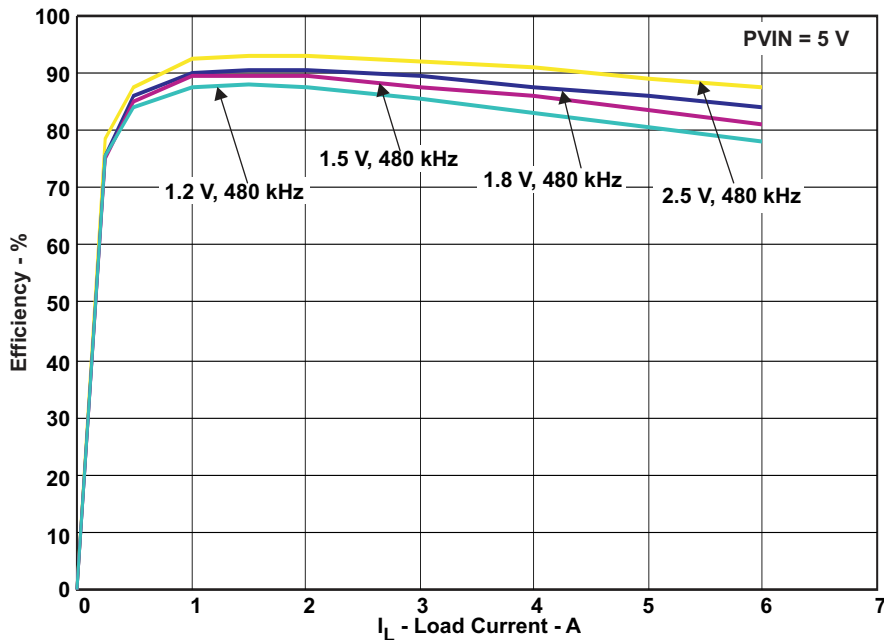


Figure 5. Efficiency vs Output Voltage/Frequency at 25°C

### 6.5 Output Voltage Load Regulation

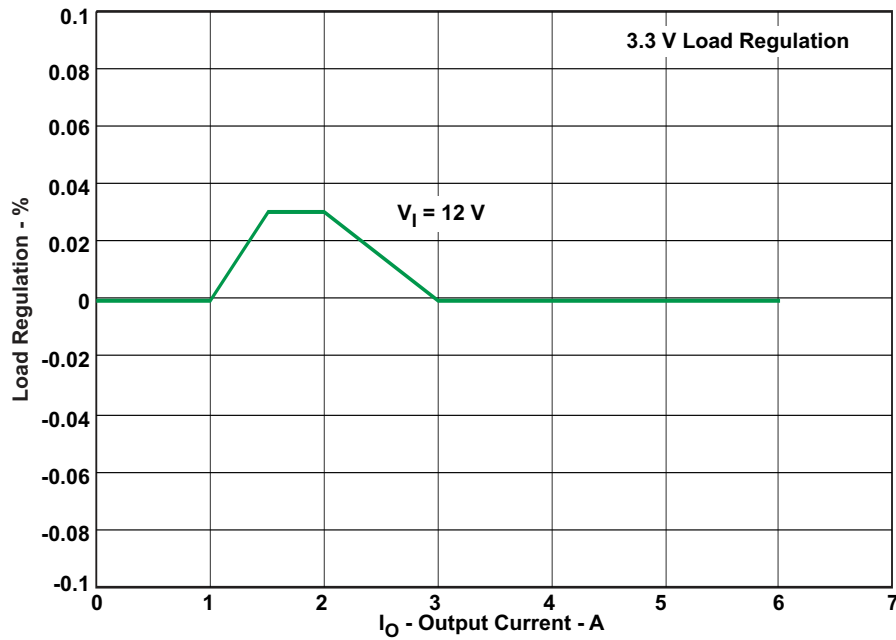


Figure 6. Load Regulation at 25°C

### 6.6 Output Voltage Line Regulation

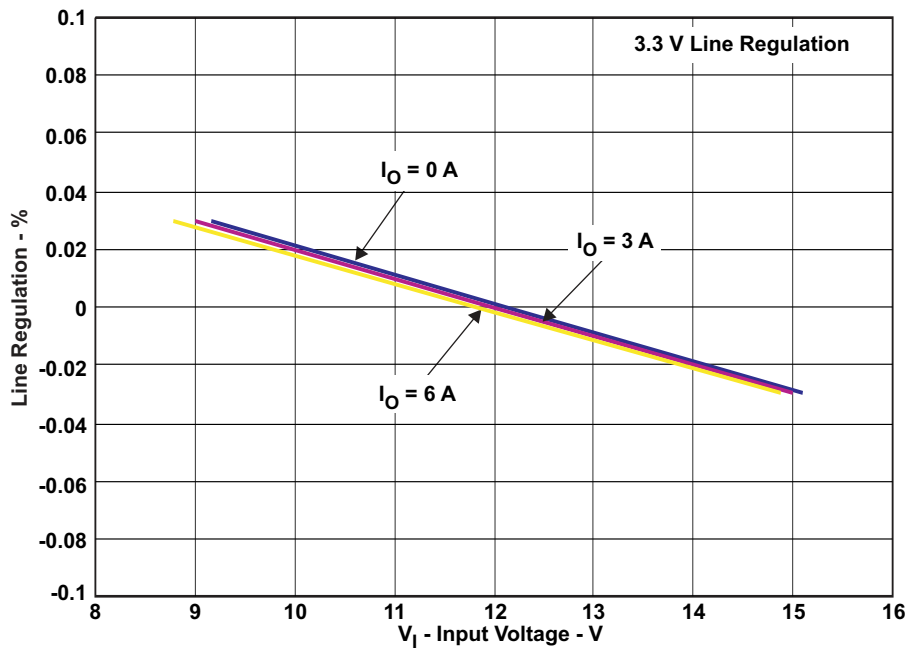


Figure 7. Line Regulation at 25°C

### 6.7 3.3-V TPS84620EVM-692 Response to Load Transients

Figure 8 shows the TPS84620EVM-692 response to load transients. The current step is from 1.5 A to 4.5 A at 12-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

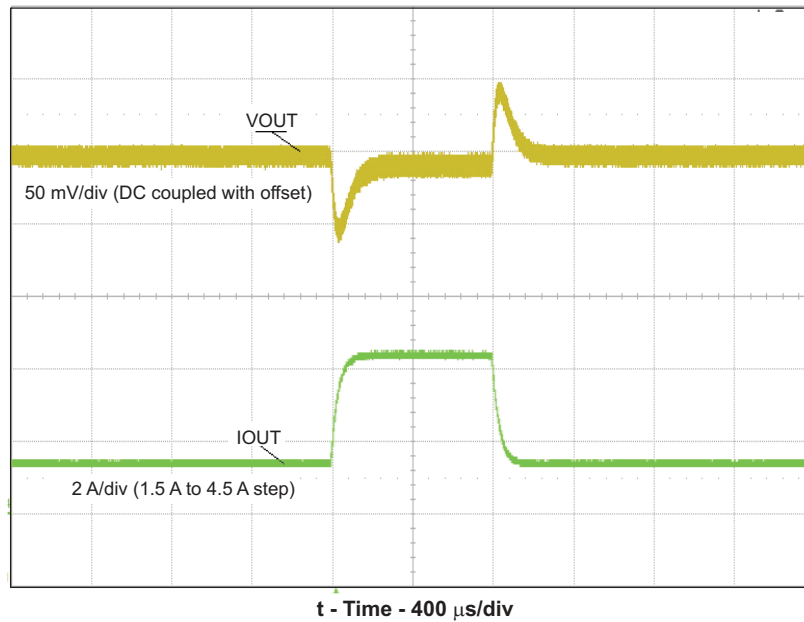


Figure 8. 3.3-V TPS84620EVM-692 Transient Response at 25°C

### 6.8 TPS84620EVM-692 Loop Response

Figure 9 shows the TPS84620EVM-692 loop response. The unity gain bandwidth is 50 kHz, phase margin is 70 degrees, gain margin is 19 dB and the gain slope is  $-1$ .

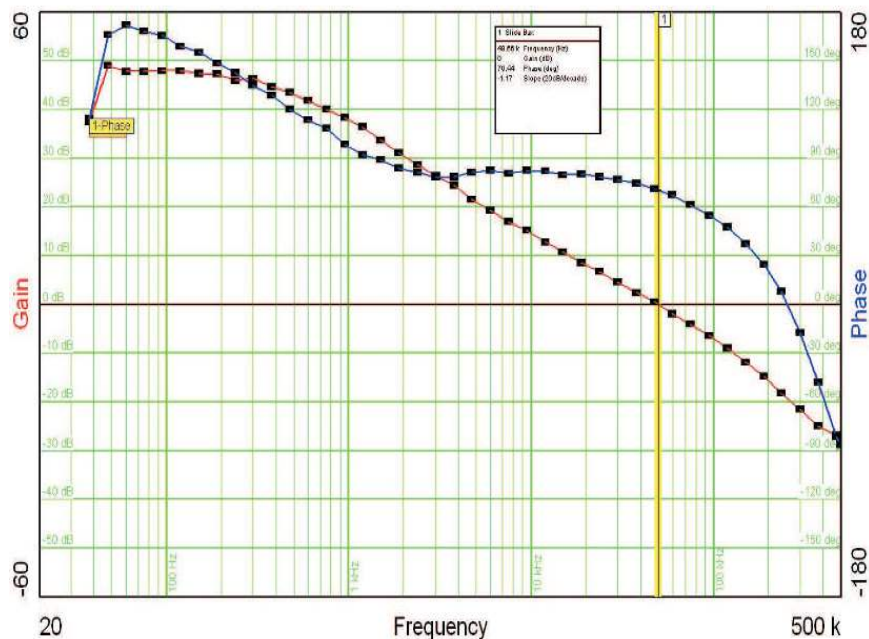
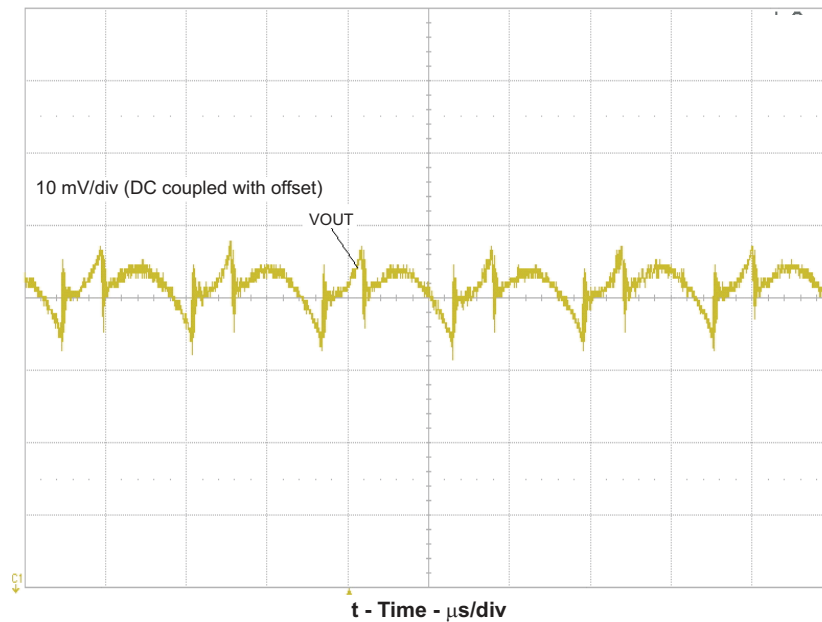


Figure 9. TPS84620EVM-692 Loop Response at 25°C

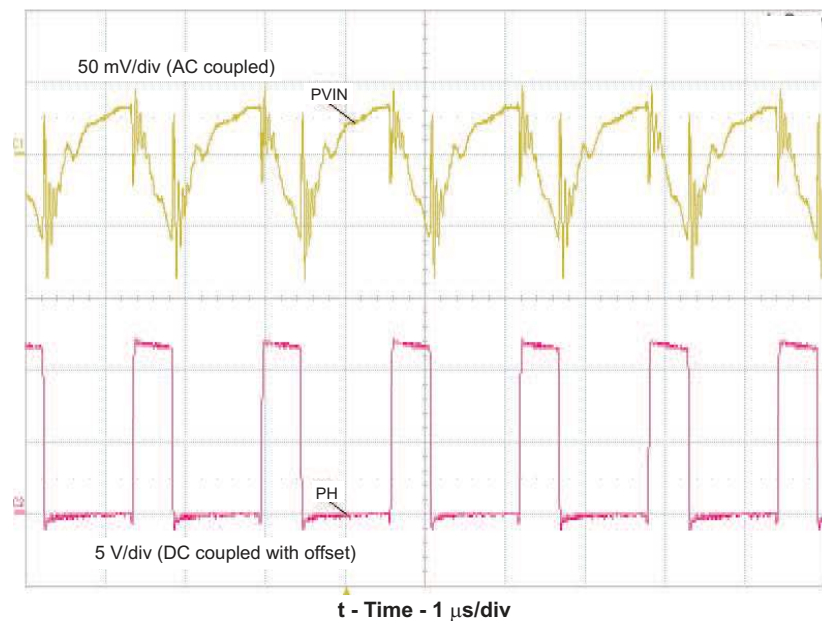
## 6.9 TPS84620EVM-692 Voltage Ripple

Figure 10 shows the TPS84620EVM-692 output voltage ripple when operating from 12 V with an output load of 6 A.



**Figure 10. TPS84620EVM-692 Output Voltage Ripple**

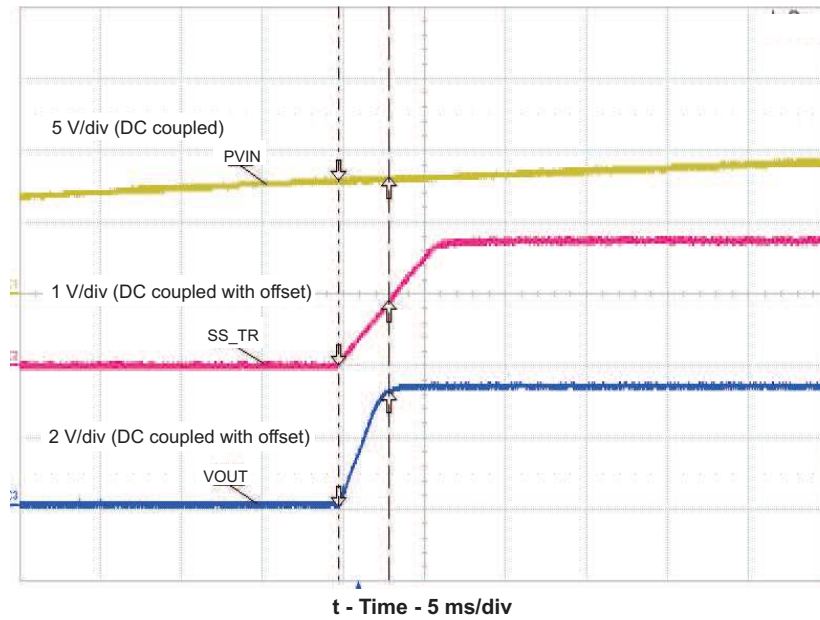
Figure 11 shows the TPS84620EVM-692 input voltage ripple when operating from 12 V with an output load of 6 A.



**Figure 11. TPS84620EVM-692 Input Voltage Ripple**

## 6.10 Power Up

Figure 12 shows the TPS84620EVM-692 start-up waveforms with rising PVIN. In Figure 12, the output starts to rise when PVIN reaches the rising UVLO of 8 V. J9 can also be used to inhibit VOUT when PVIN is present.



**Figure 12. TPS84620EVM-692 Start-Up Waveforms With Rising PVIN**

## 7 Board Layout/Assembly Drawing

This section provides a description of the TPS84x2xEVM-692, board layout, and layer illustrations.

### 7.1 Layout

The board layout for the TPS84x2xEVM-692 is shown in [Figure 14](#) through [Figure 13](#). The topside layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz. copper. A basic set of layout guidelines include:

- Place the input capacitors close to the PVIN and PGND terminals.
- Place the output capacitors close to the VO and PGND terminals.
- AGND is a 0-Vdc reference for the analog control circuitry. Connect AGND to PGND at a single point. AGND terminal 45 provides a means to remove heat from the device and must be connected to an AGND plane with multiple vias as shown in the TPS84620 data sheet, ([SLVSA43](#)).
- The SENSE+ pin (pin 44) provides a remote sense function for the device. Connect the SENSE+ pin to VO near the load.
- Analog control pins: Connect the analog control pins (VADJ, RT/CLK, INH/UVLO, STSEL, and SS/TR) to AGND using the recommended circuit components.

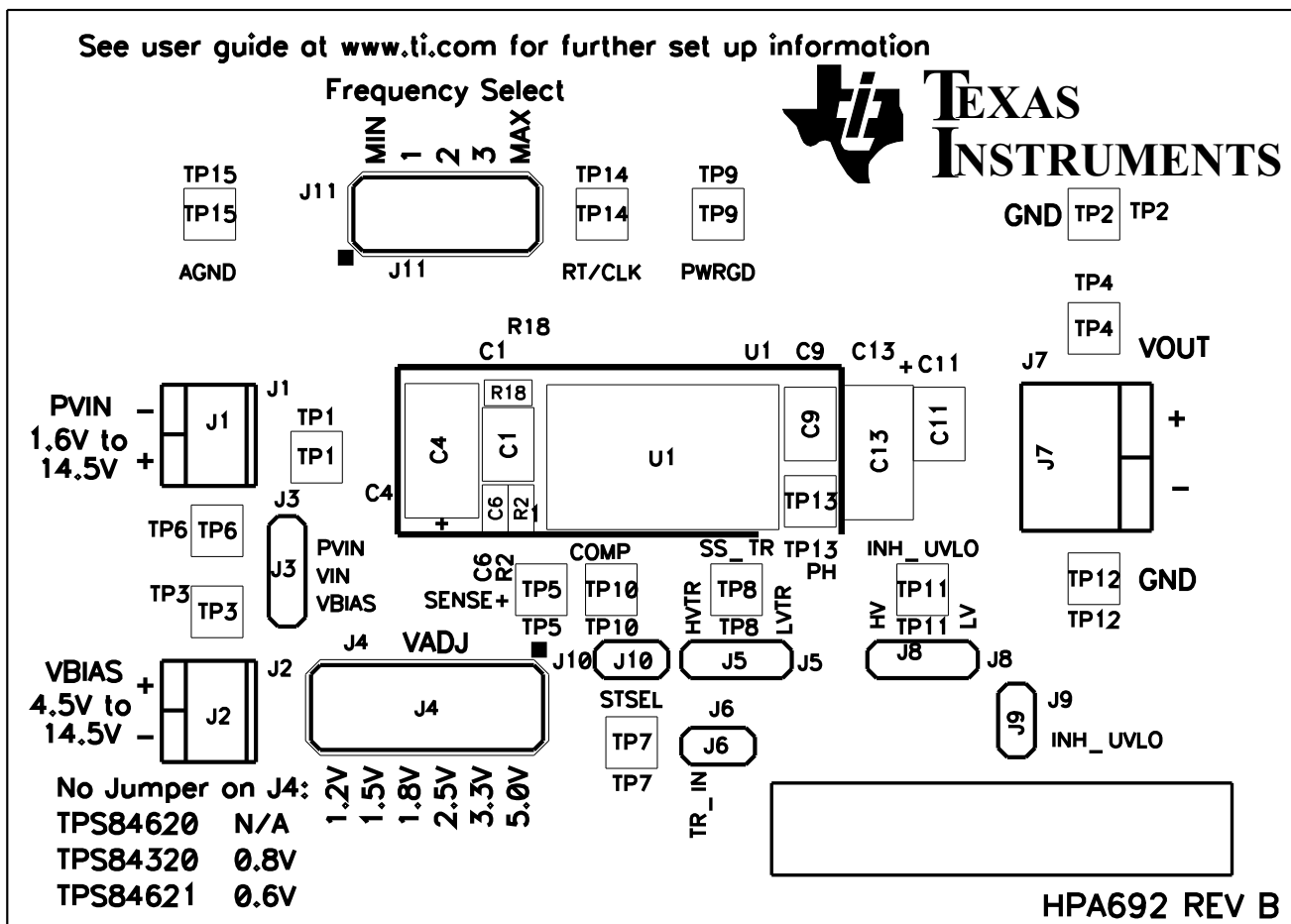
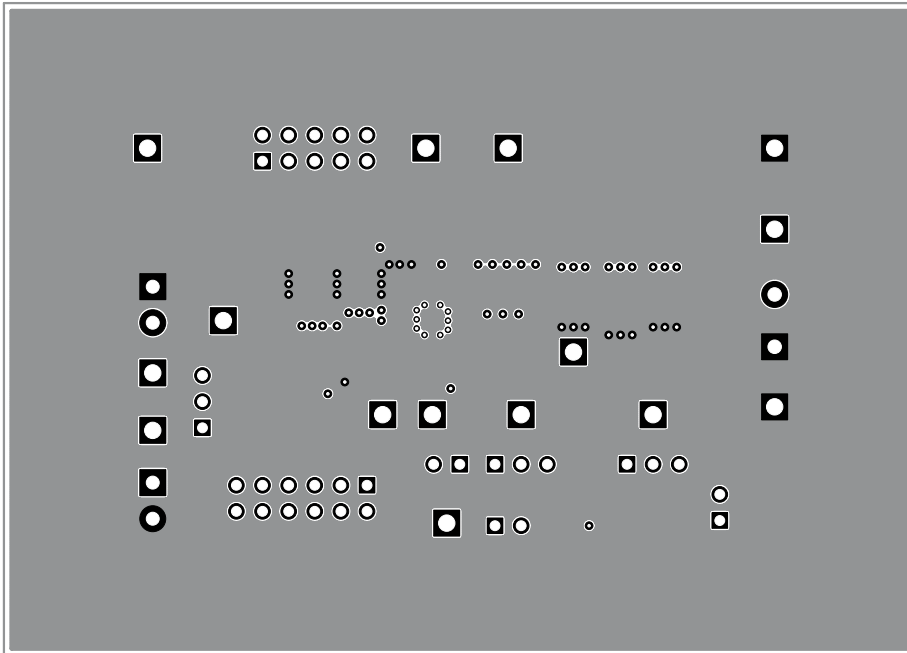
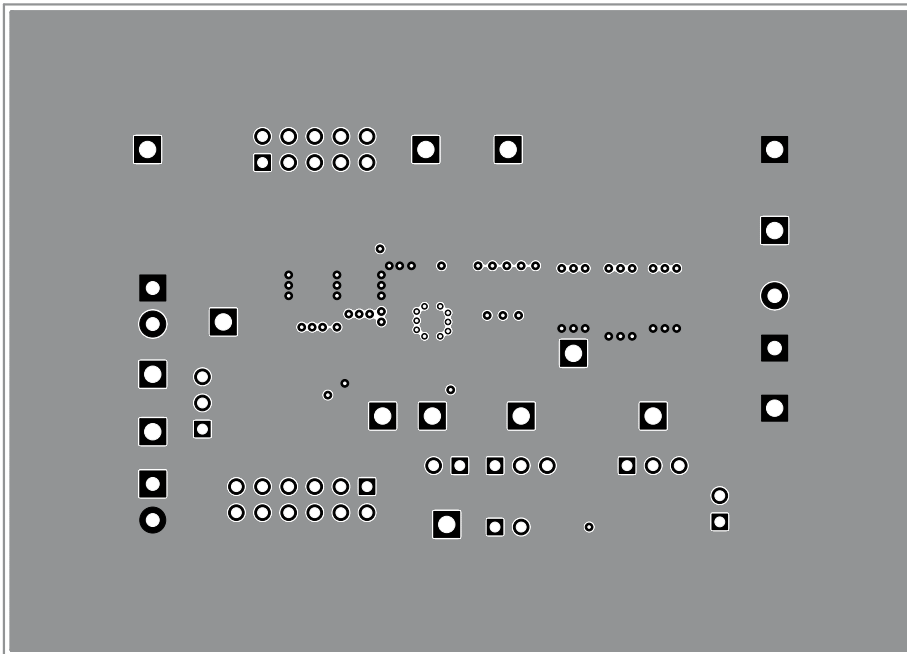


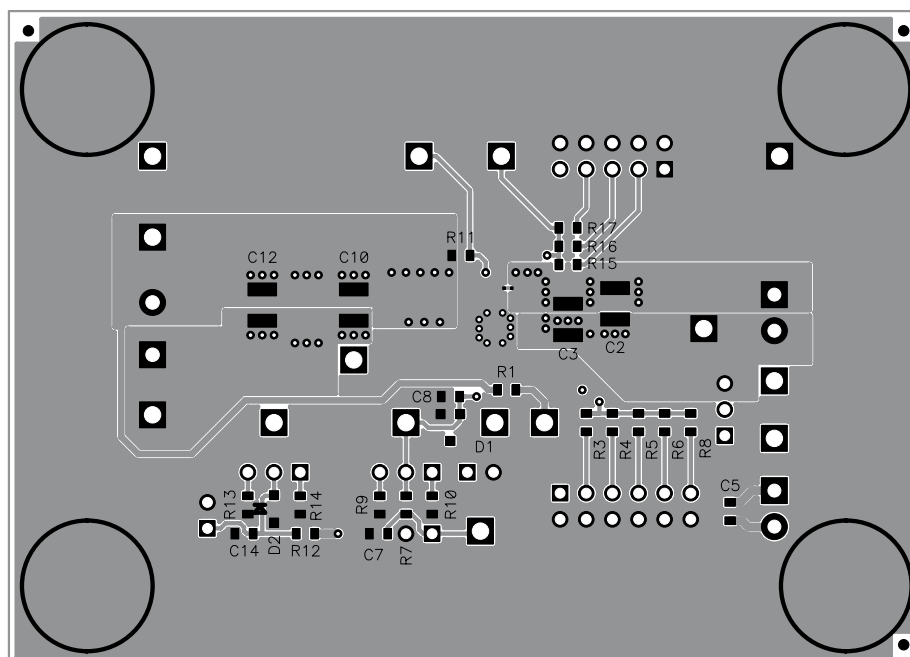
Figure 13. TPS84x2xEVM-692 Top-Side Layer and Assembly



**Figure 14. TPS84x2xEVM-692 Layer 2**



**Figure 15. TPS84x2xEVM-692 Layer 3**



**Figure 16. TPS84x2xEVM-692 Bottom-Side Layer and Assembly**

## 7.2 Estimated Circuit Area

The estimated printed-circuit board area for the components used in this design is 0.55 in<sup>2</sup> (354 mm<sup>2</sup>). This area does not include test point or connectors.



## 8 List of Materials

Table 6 presents the List of Materials for the TPS84320EVM-692, TPS84620EVM-692 and TPS84621EVM-692.

**Table 6. TPS84x2xEVM-692 List of Materials** <sup>(1)(2)(3)(4)(5)(6)</sup>

-003	-002	-001	REF DES	DESCRIPTION	PART NUMBER	MFR
2	2	2	C1, C2	Capacitor, ceramic, 16 V, X5R, 10%, 22 $\mu$ F, 1210	GRM32ER61E226K	Murata
0	0	0	C3	Capacitor, ceramic, 16 V, X5R, 10%, 22 $\mu$ F, 1210	GRM32ER61E226K	Murata
0	0	0	C13	Capacitor, polymer SMT, 6.3 V, -25 to 105°C, $\pm$ 20%, 330 $\mu$ F, 7343(D)	T530D337M006ATE006	Kemet
1	1	1	C4	Capacitor, polymer tantalum, 16 V, 20%, 68 $\mu$ F, 7343(D)	16TQC68M	Sanyo
3	3	3	C5, C6, C14	Capacitor, ceramic, 16 V, X7R, 10%, 0.1 $\mu$ F, 0603	Std	Std
0	0	0	C7	Capacitor, ceramic, 16 V, X7R, 10%, 0.1 $\mu$ F, 0603	Std	Std
1	1	1	C8	Capacitor, ceramic, 16 V, X7R, 10%, 4700 pF, 0603	Std	Std
4	4	4	C9, C10, C11, C12	Capacitor, ceramic, 6.3 V, X5R, 10%, 47 $\mu$ F, 1210	GRM32ER60J476M	Murata
0	0	0	D1	Diode, dual ultra fast, series, 200 mA, 70 V, BAV99, SOT23	BAV99	Fairchild
1	1	1	D2	Diode, Zener, 200 mW, 5.1 V, SOD-323	BZT52C5V1S	Diodes Inc.
2	2	2	J1, J2	Terminal block, 2 pin, 6 A, 3.5 mm, 0.27 inch x 0.25 inch	ED555/2DS	OST
1	1	1	J11	Header, male 2x5 pin, 100-mil spacing, 0.100 inch x 5 inch x 2 inch	PEC05DAAN	Sullins
3	3	3	J3, J5, J8	Header, male 3 pin, 100-mil spacing, 0.100 inch x 3 inch	PEC03SAAN	Sullins
1	1	1	J4	Header, male 2x6 pin, 100-mil spacing, 0.100 inch x 2 inch x 6 inch	PEC06DAAN	Sullins
3	3	3	J6, J9, J10	Header, male 2-pin, 100mil spacing, 0.100 inch x 2 inch	PEC02SAAN	Sullins
1	1	1	J7	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 inch x 0.35 inch	ED120/2DS	OST
1	1	1	R1	Resistor, chip, 1/10 W, -100/+600 ppm/°C, 0 $\Omega$ , 0603	Std	Std

<sup>(1)</sup> These assemblies are ESD sensitive, ESD precautions shall be observed.

<sup>(2)</sup> These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

<sup>(3)</sup> These assemblies must comply with workmanship standards IPC-A-610 Class 2.

<sup>(4)</sup> Ref designators marked with an asterisk (\*\*\*) cannot be substituted. All other components can be substituted with equivalent MFG's components.

<sup>(5)</sup> Install shunts in the following positions (Table 7):

<sup>(6)</sup> Install label after final wash. Text shall be 8 pt font. Text shall be per Table 8.

**Table 6. TPS84x2xEVM-692 List of Materials<sup>(1)(2)(3)(4)(5)(6)</sup> (continued)**

-003	-002	-001	REF DES	DESCRIPTION	PART NUMBER	MFR
1	1	1	R11	Resistor, chip, 1/16 W, 1%, 10 kΩ, 0603	Std	Std
1	1	1	R12	Resistor, chip, 1/16 W, 1%, 68.1 kΩ, 0603	Std	Std
1	1	1	R13	Resistor, chip, 1/16 W, 1%, 24.3 kΩ, 0603	Std	Std
1	1	1	R14	Resistor, chip, 1/16 W, 1%, 12.1 kΩ, 0603	Std	Std
0	0	1	R15	Resistor, chip, 1/16 W, 1%, 1 MΩ, 0603	Std	Std
1	0	0	R15	Resistor, chip, 1/16 W, 1%, 536 kΩ, 0603	Std	Std
0	0	1	R16	Resistor, chip, 1/16 W, 1%, 499 kΩ, 0603	Std	Std
0	1	0	R16	Resistor, chip, 1/16 W, 1%, 332 kΩ, 0603	Std	Std
1	0	0	R16	Resistor, chip, 1/16 W, 1%, 200 kΩ, 0603	Std	Std
0	0	1	R17	Resistor, chip, 1/16 W, 1%, 332 kΩ, 0603	Std	Std
0	1	0	R17	Resistor, chip, 1/16 W, 1%, 165 kΩ, 0603	Std	Std
1	0	0	R17	Resistor, chip, 1/16 W, 1%, 121 kΩ, 0603	Std	Std
0	0	1	R18	Resistor, chip, 1/16 W, 1%, 165 kΩ, 0603	Std	Std
0	1	0	R18	Resistor, chip, 1/16 W, 1%, 110 kΩ, 0603	Std	Std
1	0	0	R18	Resistor, chip, 1/16 W, 1%, 86.6 kΩ, 0603	Std	Std
0	1	1	R2	Resistor, chip, 1/16 W, 1%, 274 Ω, 0603	Std	Std
1	0	0	R2	Resistor, chip, 1/16 W, 1%, 196 Ω, 0603	Std	Std
0	1	1	R3	Resistor, chip, 1/16 W, 1%, 453 Ω, 0603	Std	Std
1	0	0	R3	Resistor, chip, 1/16 W, 1%, 316 Ω, 0603	Std	Std
0	1	1	R4	Resistor, chip, 1/16 W, 1%, 665 Ω, 0603	Std	Std
1	0	0	R4	Resistor, chip, 1/16 W, 1%, 453 Ω, 0603	Std	Std
0	1	1	R5	Resistor, chip, 1/16 W, 1%, 1.13 kΩ, 0603	Std	Std
1	0	0	R5	Resistor, chip, 1/16 W, 1%, 715 Ω, 0603	Std	Std
0	1	1	R6	Resistor, chip, 1/16 W, 1%, 1.64 kΩ, 0603	Std	Std
1	0	0	R6	Resistor, chip, 1/16 W, 1%, 953 Ω, 0603	Std	Std
0	1	1	R8	Resistor, chip, 1/16 W, 1%, 2.87 kΩ, 0603	Std	Std
1	0	0	R8	Resistor, chip, 1/16 W, 1%, 1.43 kΩ, 0603	Std	Std
2	2	2	R7, R10	Resistor, chip, 1/16 W, 1%, 20 kΩ, 0603	Std	Std
0	0	0	R6	Resistor, chip, 1/16 W, 1%, 0603	Std	Std
1	1	1	R9	Resistor, chip, 1/16 W, 1%, 11.3 kΩ, 0603	Std	Std

**Table 6. TPS84x2xEVM-692 List of Materials<sup>(1)(2)(3)(4)(5)(6)</sup> (continued)**

-003	-002	-001	REF DES	DESCRIPTION	PART NUMBER	MFR
4	4	4	TP1, TP3, TP4, TP6	Test point, red, thru hole, 5010, 0.125 inch x 0.125 inch	5010	Keystone
3	3	3	TP2, TP12, TP15	Test point, black, thru hole, 5011, 0.125 inch x 0.125 inch	5011	Keystone
3	3	3	TP5, TP10, TP13	Test point, orange, thru hole, 5013, 0.125 inch x 0.125 inch	5013	Keystone
5	5	5	TP7, TP8, TP9, TP11, TP14	Test point, white, thru hole, 5012, 0.125 inch x 0.125 inch	5012	Keystone
0	0	1	U1	5-V Input, 6-A Sync. Buck, SWIFT Module, QFN	TPS84620RUQ	TI
0	1	0	U1	5-V Input, 3-A Sync. Buck, SWIFT Module, QFN	TPS84320RUQ	TI
1	0	0	U1	5-V Input, 6-A Sync. Buck, SWIFT Module, QFN	TPS84621RUQ	TI
4	4	4		Bumpon hemisphere 0.44 x 0.20 black	SJ-5003	3M
5	5	5		Shunt, black, 100 mil	929950-00	3M
1	1	1	--	PCB, 3.5 inch x 2.5 inch x 0.062 inch	HPA692	Any

**Table 7.**

REF DES	PIN NUMBER
J3	2-3
J4	3-4
J8, J10	1-2
J11	7-8

**Table 8.**

ASSEMBLY NUMBER	TEXT
HPA692-001	TPS84620EVM-692
HPA692-002	TPS84320EVM-692
HPA692-003	TPS84621EVM-692

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Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 55°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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