Low Voltage, 4A DC/DC µModule Regulator with Tracking

FEATURES

- **Complete Standalone Power Supply**
- **±1.75% Max Total DC Output Error (–40°C to 125°C)**
- **Wide Input Voltage Range: 2.375V to 5.5V**
- **4A DC, 5A Peak Output Current**
- **0.8V to 5V Output**
- **Output Voltage Tracking**
- **UltraFast™ Transient Response**
- Power Good Indicator
- Current Mode Control
- Current Foldback Protection, Parallel/Current Sharing
- Up to 95% Efficiency
- Programmable Soft-Start
- Micropower Shutdown: $I_Q \leq 7\mu A$
- Overtemperature Protection
- 9mm × 15mm × 2.32mm LGA and 9mm × 15mm × 3.42mm BGA Packages

APPLICATIONS

- Telecom and Networking Equipment
- Servers
- Storage Cards
- ATCA Cards
- Industrial Equipment

DESCRIPTION

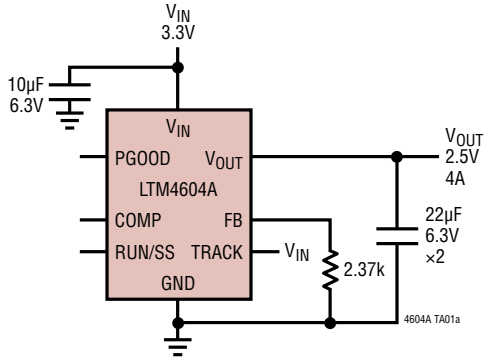
The LTM®4604A is a complete 4A switch mode step-down µModule® (micromodule) regulator with ±1.75% maximum total output voltage error. Included in the package are the switching controller, power FETs, inductor and all support components. Operating over an input voltage range of 2.375V to 5.5V, the LTM4604A supports an output voltage range of 0.8V to 5V, set by a single resistor. This high efficiency design delivers up to 4A continuous current (5A peak). Only input and output capacitors are needed to complete the design.

The 0.630mm LGA pads with 1.27mm pitch simplify PCB layout by providing standard trace routing and via placement. (The LTM4604A has smaller pads than the LTM4604). The low profile package enables utilization of unused space on the bottom of PC boards for high density point of load regulation. High switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability.

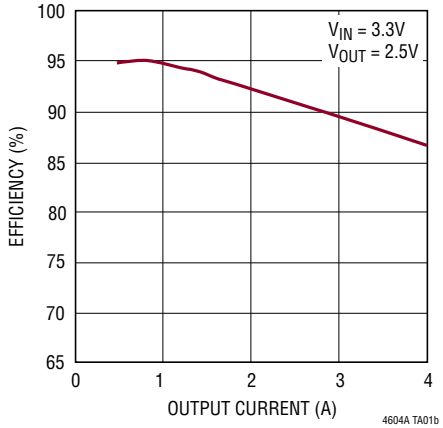
Fault protection features include foldback current protection, thermal shutdown and a programmable soft-start function. The LTM4604A is offered with SnPb (BGA) or RoHS-compliant terminal finish.

TYPICAL APPLICATION

3.3V to 2.5V/4A µModule Regulator



Efficiency vs Output Current



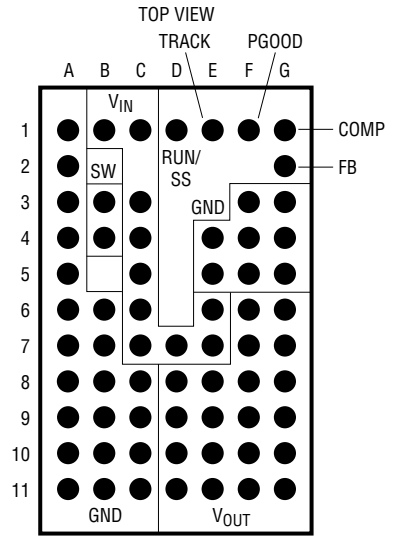
Rev. D

ABSOLUTE MAXIMUM RATINGS (Note 1)

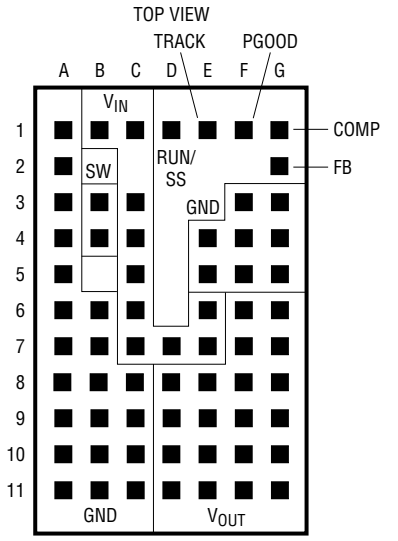
V_{IN}, PGOOD ..... –0.3V to 6V
COMP, RUN/SS, FB, TRACK ..... –0.3V to V_{IN}
SW, V_{OUT} ..... –0.3V to (V_{IN} + 0.3V)

Internal Operating Temperature Range
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature:
BGA ..... 245°C
LGA ..... 260°C

PIN CONFIGURATION



BGA PACKAGE
66-PIN (15mm × 9mm × 3.42mm)
T_{JMAX} = 125°C, θ_{JA} = 25°C/W, $\theta_{JC(BOTTOM)}$ = 7°C/W, $\theta_{JC(TOP)}$ = 50°C/W, WEIGHT = 1.1g



LGA PACKAGE
66-PIN (15mm × 9mm × 2.32mm) 0.630mm PAD
T_{JMAX} = 125°C, θ_{JA} = 25°C/W, $\theta_{JC(BOTTOM)}$ = 7°C/W, $\theta_{JC(TOP)}$ = 50°C/W, WEIGHT = 1.0g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE NOTE 2)
		DEVICE	FINISH CODE			
LTM4604AEV#PBF	Au (RoHS)	LTM4604AV	e4	LGA	4	–40°C to 125°C
LTM4604AIV#PBF	Au (RoHS)	LTM4604AV	e4	LGA	4	–40°C to 125°C
LTM4604AEY#PBF	SAC305 (RoHS)	LTM4604AY	e1	BGA	4	–40°C to 125°C
LTM4604AIY#PBF	SAC305 (RoHS)	LTM4604AY	e1	BGA	4	–40°C to 125°C
LTM4604AIY	SnPb (63/37)	LTM4604AY	e0	BGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Device temperature grade is indicated by a label on the shipping container.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 5V unless otherwise noted. See Figure 15.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage		●	2.375		5.5	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF, C_{OUT} = 22µF × 3, R_{FB} = 5.69k V_{IN} = 2.375V to 5.5V, I_{OUT} = 0A to 4A (Note 3)	 ●	1.482 1.474	1.5 1.5	1.518 1.522	V V
Input Specifications							
$V_{IN(UVLO)}$	Undervoltage Lockout Threshold	I_{OUT} = 0A		1.75	2	2.3	V
$I_{INRUSH(VIN)}$	Peak Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 10µF, C_{OUT} = 22µF × 3, RUN/SS = 0.01µF, V_{OUT} = 1.5V V_{IN} = 3.3V V_{IN} = 5V			 0.7 0.7		 A A
$I_{Q(VIN\ NOLOAD)}$	Input Supply Bias Current	V_{IN} = 3.3V, No Switching V_{IN} = 3.3V, V_{OUT} = 1.5V, Switching Continuous V_{IN} = 5V, No Switching V_{IN} = 5V, V_{OUT} = 1.5V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 5V			60 28 100 35 7		µA mA µA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 2.5V, V_{OUT} = 1.5V, I_{OUT} = 4A V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 4A V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 4A			2.9 2.2 1.45		A A A
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 3.3V, V_{OUT} = 1.5V (Note 3)				4	A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 2.375V to 5.5V, I_{OUT} = 0A	●		0.1	0.2	%
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, 0A to 4A (Note 3) V_{IN} = 3.3V V_{IN} = 5V	 ● ●		 0.3 0.3	 0.6 0.6	 % %
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A V_{IN} = 3.3V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			 10 12		 mV_{P-P} mV_{P-P}
f_S	Output Ripple Voltage Frequency	I_{OUT} = 4A, V_{IN} = 5V, V_{OUT} = 1.5V			1.25		MHz
$\Delta V_{OUT(START)}$	Turn-On Overshoot	V_{OUT} = 1.5V, RUN/SS = 10nF, C_{OUT} = 22µF × 3, I_{OUT} = 0A V_{IN} = 3.3V V_{IN} = 5V			 20 20		 mV mV
t_{START}	Turn-on Time	C_{OUT} = 22µF × 3, V_{OUT} = 1.5V, I_{OUT} = 1A Resistive Load, TRACK = V_{IN} and RUN/SS = Float V_{IN} = 3.3V V_{IN} = 5V			 1.5 1.0		 ms ms
$\Delta V_{OUT(LS)}$	Peak Deviation for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 22µF ×3 Ceramic V_{IN} = 5V, V_{OUT} = 1.5V			 25		 mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load V_{IN} = 5V, V_{OUT} = 1.5V			 10		 µs
$I_{OUT(PK)}$	Output Current Limit	V_{IN} = 3.3V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			8 8		A A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 5V unless otherwise noted. See Figure 15.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Section							
V_{FB}	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	 ●	0.793 0.788	0.8 0.8	0.807 0.808	V V
I_{FB}					0.2		µA
$V_{RUN/SS}$	RUN/SS Pin On/Off Threshold			0.5	0.65	0.8	V
I_{TRACK}	TRACK Pin Current				0.2		µA
$V_{TRACK(OFFSET)}$	Offset Voltage	TRACK = 0.4V			30		mV
$V_{TRACK(RANGE)}$	Tracking Input Range			0		0.8	V
R_{FBHI}	Resistor Between V_{OUT} and FB Pins			4.965	4.99	5.015	kΩ
PGOOD							
ΔV_{PGOOD}	PGOOD Range				±7.5		%
R_{PGOOD}	PGOOD Resistance	Open-Drain Pull-Down			90	150	Ω

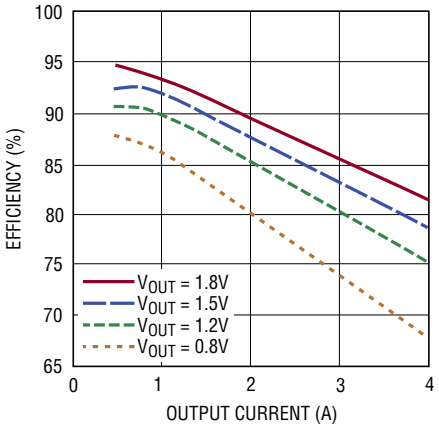
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4604A is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4604AE is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4604AI is guaranteed to meet specifications over the full internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

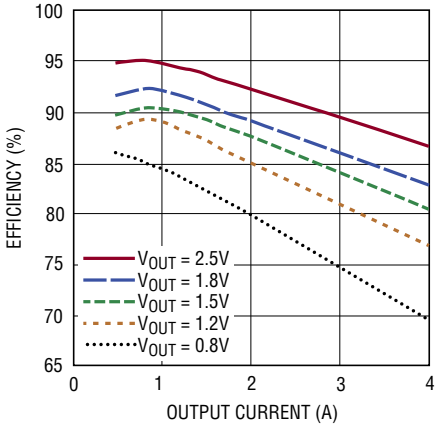
Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

TYPICAL PERFORMANCE CHARACTERISTICS

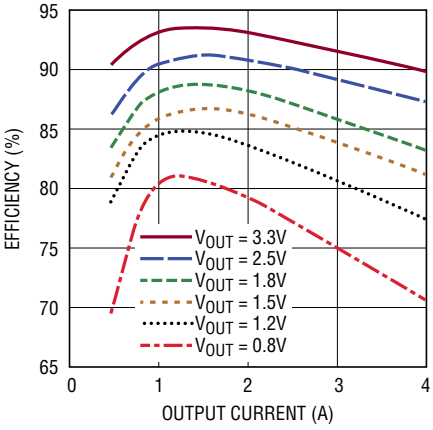
Efficiency vs Output Current
V_{IN} = 2.5V



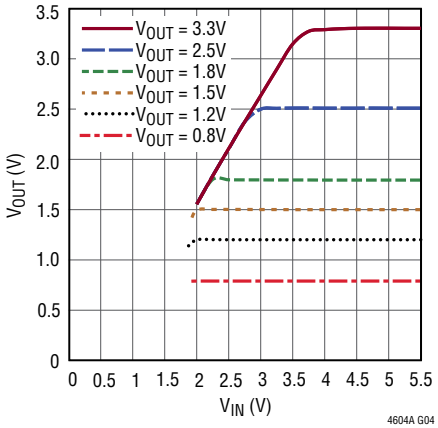
Efficiency vs Output Current
V_{IN} = 3.3V



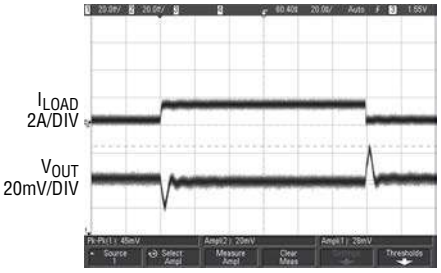
Efficiency vs Output Current
V_{IN} = 5V



Minimum Input Voltage at 4A Load

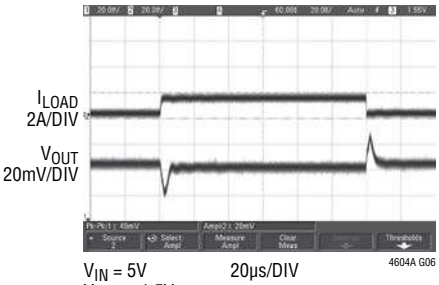


Load Transient Response



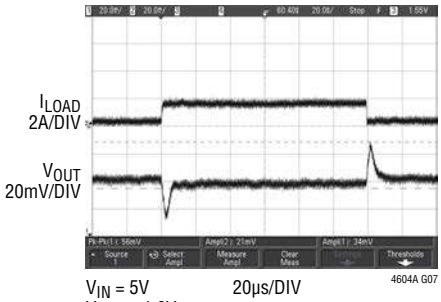
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.2V
C_{OUT} = 4 × 22µF, 6.3V CERAMICS
I_{OUT} = 0A TO 2A

Load Transient Response



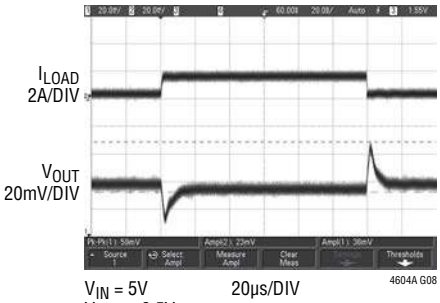
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 4 × 22µF, 6.3V CERAMICS
I_{OUT} = 0A TO 2A

Load Transient Response



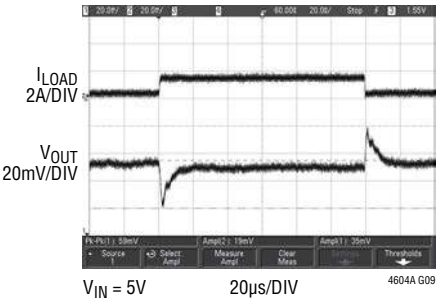
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.8V
C_{OUT} = 3 × 22µF, 6.3V CERAMICS
I_{OUT} = 0A TO 2A

Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 3 × 22µF, 6.3V CERAMICS
I_{OUT} = 0A TO 2A

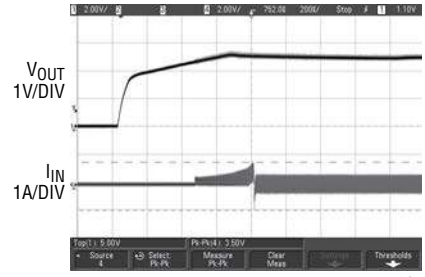
Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 3.3V
C_{OUT} = 2 × 22µF, 6.3V CERAMICS
I_{OUT} = 0A TO 2A

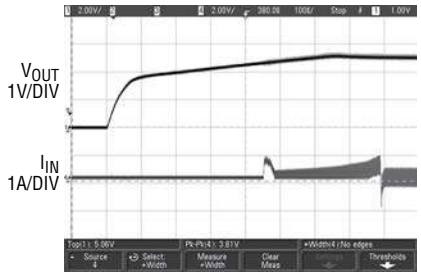
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up



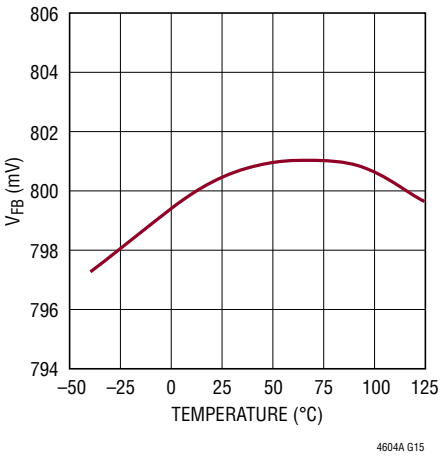
V_{IN} = 5V 200µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 4 × 22µF
NO LOAD
(0.01µF SOFT-START CAPACITOR)

Start-Up

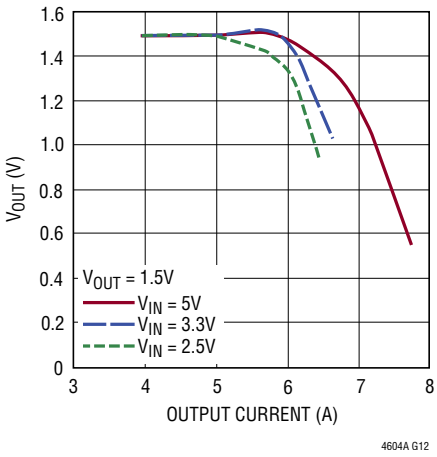


V_{IN} = 5V 200µs/DIV
V_{OUT} = 2.5V
C_{OUT} = 4 × 22µF
4A LOAD
(0.01µF SOFT-START CAPACITOR)

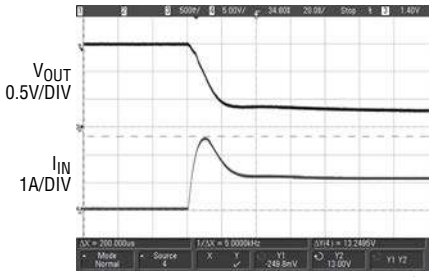
V_{FB} vs Temperature



Current Limit Foldback

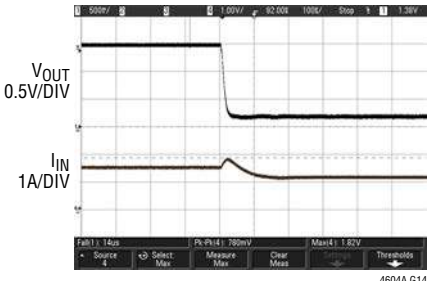


Short-Circuit Protection
1.5V Short, No Load



V_{IN} = 5V 20µs/DIV

Short-Circuit Protection
1.5V Short, 4A Load



V_{IN} = 5V 100µs/DIV

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{IN} (B1, C1, C3-C7, D7, E6 and E7): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT} (D8-D11, E8-E11, F6-F11, G6-G11): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 4.

GND (G3-G5, F3-F5, E4-E5, A1-A11, B6-B11, C8-C11): Power Ground Pins for Both Input and Output Returns.

TRACK (E1): Output Voltage Tracking Pin. When the module is configured as a master output, then a soft-start capacitor is placed on the RUN/SS pin to ground to control the master ramp rate. Slave operation is performed by putting a resistor divider from the master output to ground, and connecting the center point of the divider to this pin on the slave regulator. If tracking is not desired, then connect the TRACK pin to V_{IN}. Load current must be present for tracking. See the Applications Information section.

FB (G2): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT} with a 4.99k precision resistor. Different output voltages can be programmed with an externally connected resistor between FB and GND pins. Two power modules can current share when this pin is connected in parallel with the adjacent module's FB pin. See the Applications Information section.

COMP (G1): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Two power modules can current share when this pin is connected in parallel with the adjacent module's COMP pin.

PGOOD (F1): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±7.5% of the regulation point.

RUN/SS (D1): Run Control and Soft-Start Pin. A voltage above 0.8V will turn on the module, and below 0.5V will turn off the module. This pin has a 1M resistor to V_{IN} and a 1000pF capacitor to GND. The voltage on the RUN/SS pin clamps the control loop's current comparator threshold. A RUN/SS pin voltage of 2.375V upon completion of soft-start guarantees the regulator can deliver full output current. To tun off the module while V_{IN} remains active, the RUN/SS pin should be pulled low with a falling edge ≤ 1µs to ensure the device does not transition slowly through the internal undervoltage lockout threshold. See the Applications Information section for soft-start information.

SW (B3 and B4): Switching Node of the circuit is used for testing purposes. This can be connected to copper on the board to improve thermal performance. Make sure not to connect it to other output pins.

BLOCK DIAGRAM

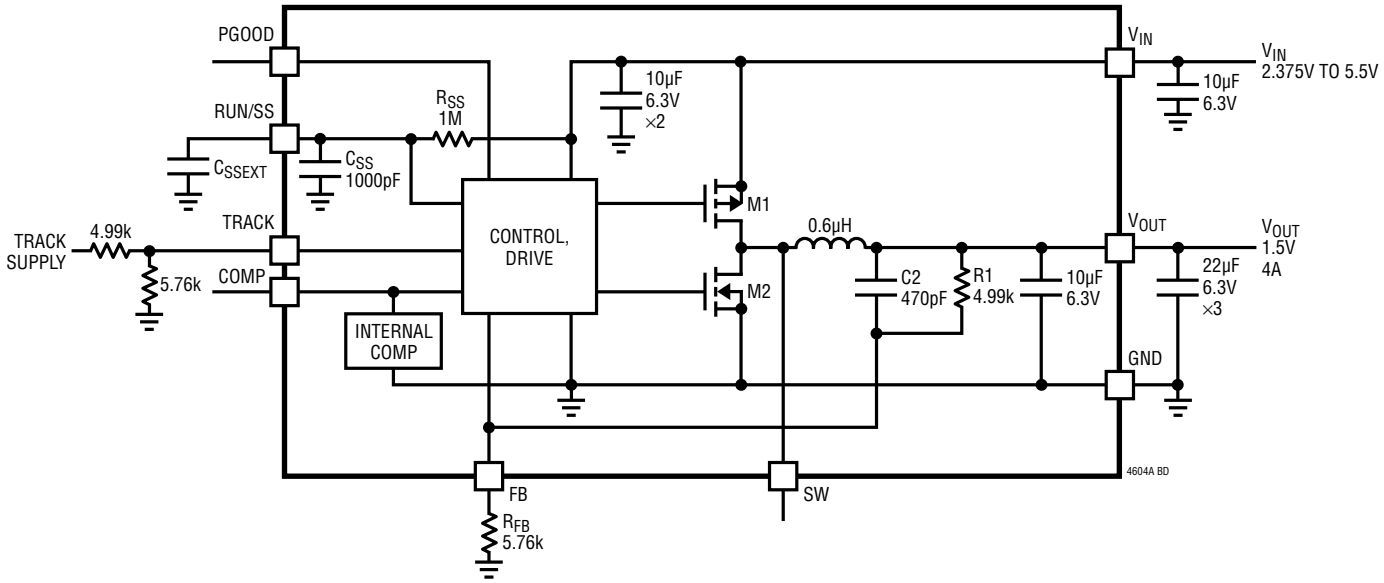


Figure 1. Simplified LTM4604A Block Diagram

DECOUPLING REQUIREMENTS T_A = 25°C. Use Figure 1 Configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 2.375V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 4A			10		µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 2.375V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 4A			66		µF

OPERATION

Power Module Description

The LTM4604A is a standalone non-isolated switch mode DC/DC power supply. It can deliver up to 4A of DC output current with few external input and output capacitors. This module provides a precise regulated output voltage programmable via one external resistor from 0.8V DC to 5.0V DC over a 2.375V to 5.5V input voltage. A typical application schematic is shown in Figure 15.

The LTM4604A has an integrated constant frequency current mode regulator with built-in power MOSFETs with fast switching speed. The typical switching frequency is 1.25MHz. With current mode control and internal feedback loop compensation, the LTM4604A module has sufficient stability margins and good transient performance under a wide range of operating conditions and with a wide range of output capacitors, even all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit. In addition, foldback current limiting is provided in an overcurrent condition while V_{OUT} drops. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±7.5% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET M1 is turned off and bottom FET M2 is turned on and held on until the overvoltage condition clears.

Pulling the RUN/SS pin below 0.5V forces the controller into its shutdown state, turning off both M1 and M2. At low load current, the module works in continuous current mode by default to achieve minimum output voltage ripple.

The TRACK pin is used for power supply tracking. See the Applications Information section.

The LTM4604A is internally compensated to be stable over a wide operating range. Table 4 provides a guideline for input and output capacitance for several operating conditions. The LTpowerCAD® GUI is available for transient and stability analysis.

The FB pin is used to program the output voltage with a single external resistor connected to ground.

APPLICATIONS INFORMATION

A typical LTM4604A application circuit is shown in Figure 15. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 4 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. The LTM4604A is 100% duty cycle capable, but the V_{IN} to V_{OUT} minimum dropout is a function of the load current. A typical 0.5V minimum is sufficient (see Typical Performance Characteristics).

Output Voltage Programming

The PWM controller has an internal 0.8V reference voltage. As shown in the Block Diagram, a 4.99k 0.5% internal feedback resistor connects the V_{OUT} and FB pins together. The output voltage will default to 0.8V with no externally applied feedback resistor. Adding a resistor R_{FB} from the FB pin to GND programs the output voltage:

$$V_{OUT} = 0.8V \bullet \frac{4.99k + R_{FB}}{R_{FB}}$$

Table 1. FB Resistor vs Output Voltage

V_{OUT}	0.8V	1V	1.2V	1.5V	1.8V	2.5V	3.3V
R_{FB}	Open	20k	10k	5.76k	4.02k	2.37k	1.62k

Input Capacitors

The LTM4604A module should be connected to a low AC-impedance DC source. Two 10µF ceramic capacitors are included inside the module. Additional input capacitors are only needed if a large load step is required up to a full 4A level. An input 47µF bulk capacitor is only needed if the input source impedance is compromised by long inductive leads or traces.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated aluminum electrolytic capacitor, OS-CON or polymer capacitor. If a low inductance plane is used to power the device, then no input capacitance is required. The two internal 10µF ceramics are typically rated for 2A to 3A of RMS ripple current. The worst-case ripple current for the 4A maximum current is 2A or less.

Output Capacitors

The LTM4604A is designed for low output voltage ripple. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or an X5R/X7R ceramic capacitor. The typical output capacitance range is 22µF to 100µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 2A/µs transient. The table optimizes the total equivalent ESR and total bulk capacitance to maximize transient performance. The LTpowerCAD GUI is available for further optimization.

Fault Conditions: Current Limit and Overcurrent Foldback

The LTM4604A has current mode control, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient.

To further limit current in the event of an overload condition, the LTM4604A provides foldback current limiting as the output voltage falls. The LTM4604A device has overtemperature shutdown protection that inhibits switching operation around 150°C.

APPLICATIONS INFORMATION

Run Enable and Soft-Start

The RUN/SS pin provides dual functions of enable and soft-start control. The RUN/SS pin is used to control turn on of the LTM4604A. While this pin is below 0.5V, the LTM4604A will be in a 7µA low quiescent current state. A 0.8V threshold will enable the LTM4604A. This pin can be used to sequence LTM4604A devices. The voltage on the RUN/SS pin clamps the control loop's current comparator threshold. A RUN/SS pin voltage of 2.375V upon completion of soft-start guarantees the regulator can deliver full output current. The soft-start control is provided by a 1M pull-up resistor (R_{SS}) and a 1000pF capacitor (C_{SS}) as shown in the Block Diagram. An external capacitor can be applied to the RUN/SS pin to increase the soft-start time. A typical value is 0.01µF. Soft-start time is approximately given by:

$$t_{SOFTSTART} = \ln\left(\frac{V_{IN}}{V_{IN}-1.8V}\right) \bullet R_{SS}\left(C_{SS}+C_{SSEXT}\right)$$

where R_{SS} and C_{SS} are shown in the Block Diagram of Figure 1, 1.8V is the soft-start upper range, and C_{SSEXT} is the additional capacitance for further soft-start control. The soft-start function can also be used to control the output ramp-up time, so that another regulator can be easily tracked. An independent ramp control signal can be applied to the master ramp, otherwise, connect the TRACK pin to V_{IN} to disable tracking. To turn off the module while V_{IN} remains active, the RUN/SS pin should be pulled low with a falling edge ≤1µs to ensure the device does not transition slowly through the internal undervoltage lockout threshold.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4604A uses a very accurate 4.99k resistor for the top feedback resistor. Figure 2 and Figure 3 show an example of coincident tracking.

$$V_{TRACK} = \frac{R_{FB2}}{4.99k + R_{FB2}} \bullet V_{MASTER}$$

V_{TRACK} is the track ramp applied to the slave's TRACK pin. V_{TRACK} applies the track reference for the slave output up to the point of the programmed value at which V_{TRACK} proceeds beyond the 0.8V reference value. The V_{TRACK}

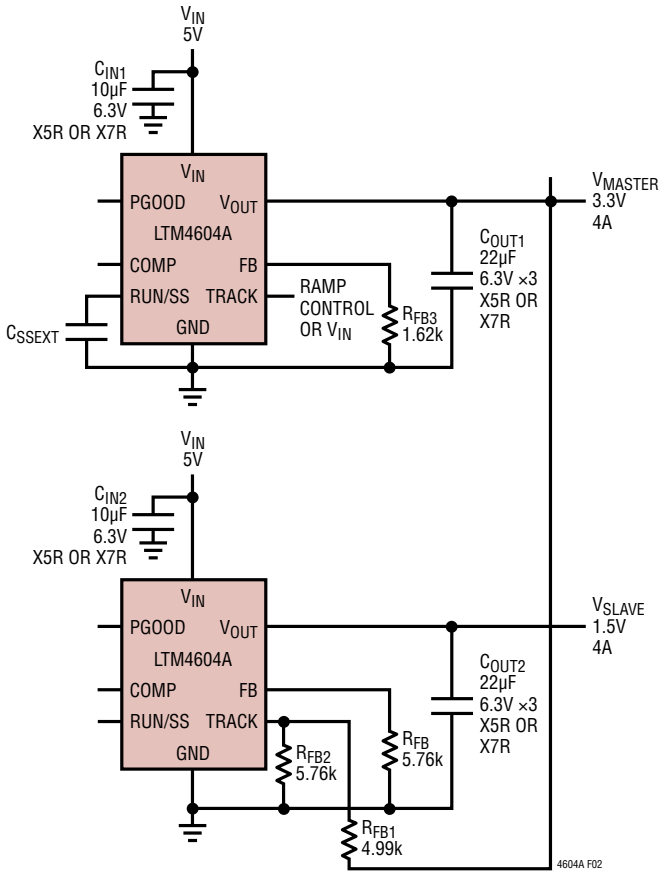


Figure 2. Dual Outputs (3.3V and 1.5V) with Tracking

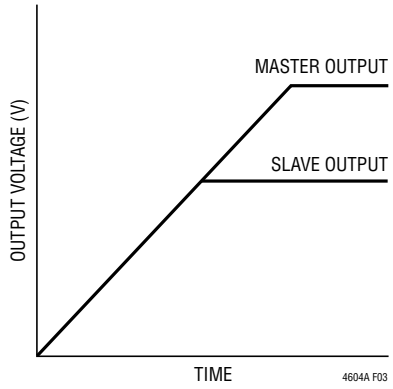


Figure 3. Output Voltage Coincident Tracking

APPLICATIONS INFORMATION

pin must go beyond 0.8V to ensure the slave output has reached its final value. Load current must be present for proper tracking.

Ratiometric modes of tracking can be achieved by selecting different resistor values to change the output tracking ratio. The master output must be greater than the slave output for ratiometric tracking to work. LTspice® can be used to implement different tracking scenarios. The Master and Slave data inputs can be used to implement the correct resistor values for coincident or ratio tracking. The master and slave regulators require load current for tracking down.

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±7.5% window around the regulation point.

COMP Pin

The COMP pin is the external compensation pin. The LTM4604A has already been internally compensated for all output voltages. Table 4 is provided for most application requirements. The LTpowerCAD GUI is available for other control loop optimizations.

Parallel Operation

The LTM4604A device is an inherently current mode controlled device. Parallel modules will have very good current sharing. This will balance the thermals on the design. Figure 16 shows a schematic of the parallel design. The voltage feedback changes with the variable N as more modules are paralleled. The equation:

$$V_{OUT} = 0.8V \bullet \frac{\frac{4.99k}{N} + R_{FB}}{R_{FB}}$$

N is the number of paralleled modules.

Thermal Considerations and Output Current Derating

The power loss curves in Figure 4 and Figure 5 can be used in coordination with the load derating curves in Figure 6 through Figure 13 for calculating an approximate θ_{JA} for the module with and without heat sinking methods with various airflow conditions. Thermal models are derived from several temperature measurements at the bench, and are correlated with thermal analysis software. Table 2 and Table 3 provide a summary of the equivalent θ_{JA} for the noted conditions. These equivalent θ_{JA} parameters are correlated to the measured values and improve with air flow. The maximum junction temperature is monitored while the derating curves are derived.

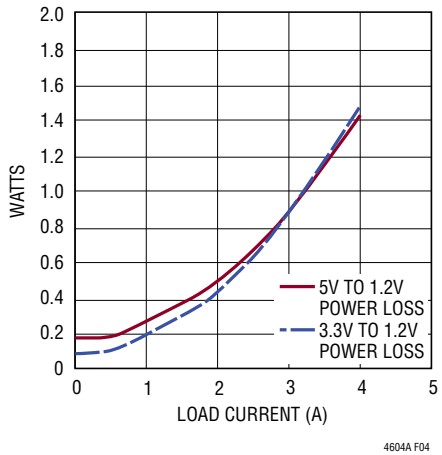


Figure 4. 1.2V Power Loss

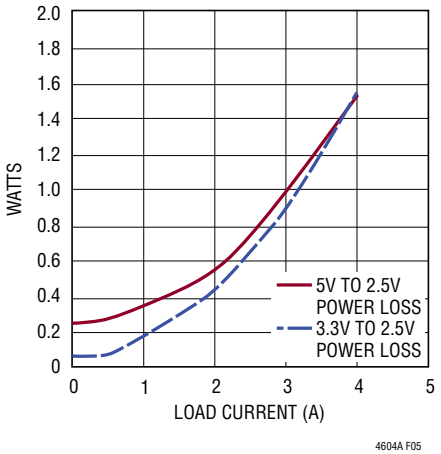


Figure 5. 2.5V Power Loss

APPLICATIONS INFORMATION

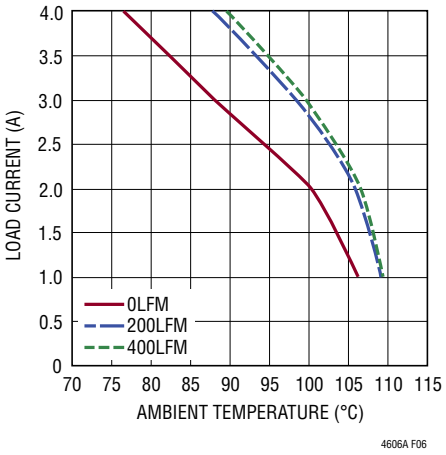


Figure 6. $5V_{IN}$ to $1.2V_{OUT}$ No Heat Sink

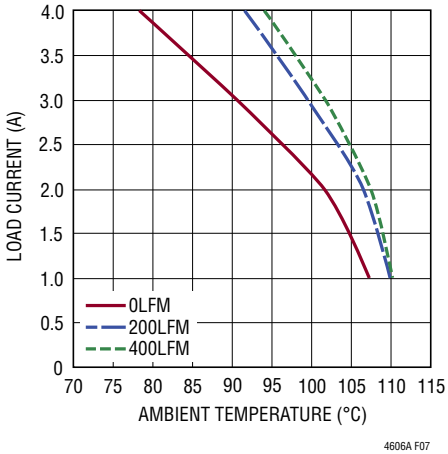


Figure 7. $5V_{IN}$ to $1.2V_{OUT}$ with Heat Sink

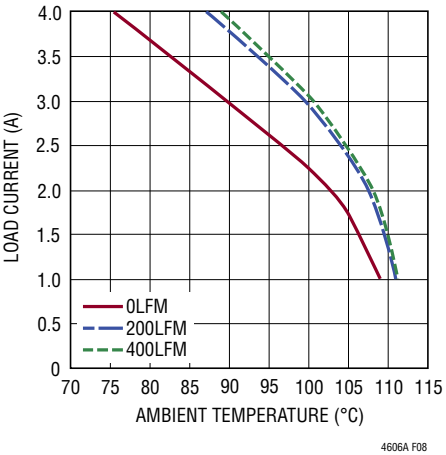


Figure 8. $3.3V_{IN}$ to $1.2V_{OUT}$ No Heat Sink

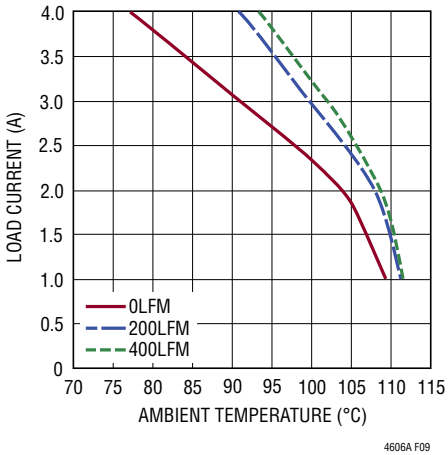


Figure 9. $3.3V_{IN}$ to $1.2V_{OUT}$ with Heat Sink

APPLICATIONS INFORMATION

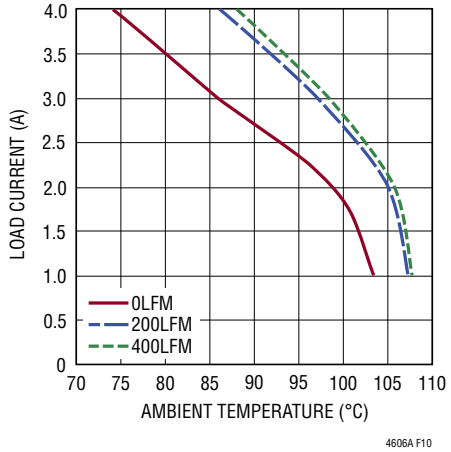


Figure 10. $5V_{IN}$ to $2.5V_{OUT}$ No Heat Sink

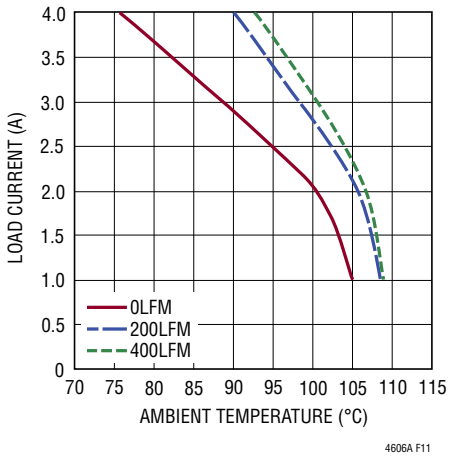


Figure 11. $5V_{IN}$ to $2.5V_{OUT}$ with Heat Sink

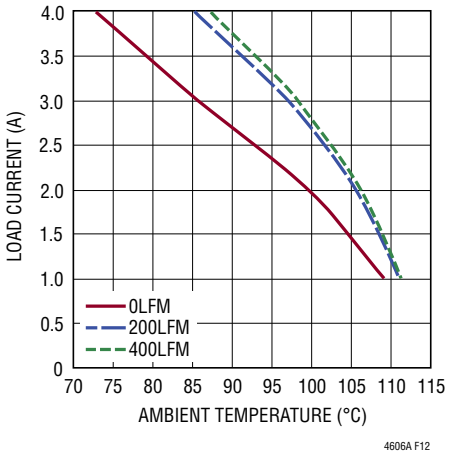


Figure 12. $3.3V_{IN}$ to $2.5V_{OUT}$ No Heat Sink

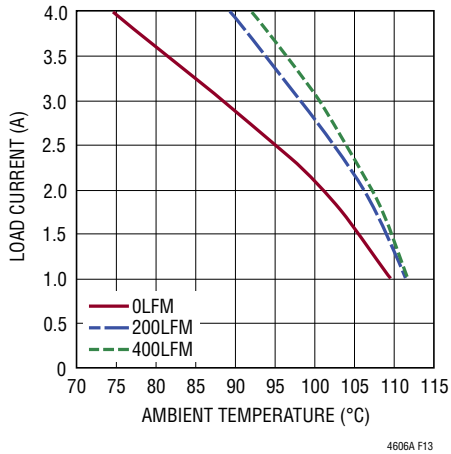


Figure 13. $3.3V_{IN}$ to $2.5V_{OUT}$ with Heat Sink

APPLICATIONS INFORMATION

Table 2. 1.2V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 6, Figure 8	3.3, 5	Figure 4	0	None	25
Figure 6, Figure 8	3.3, 5	Figure 4	200	None	22.5
Figure 6, Figure 8	3.3, 5	Figure 4	400	None	21
Figure 7, Figure 9	3.3, 5	Figure 4	0	BGA Heat Sink	21
Figure 7, Figure 9	3.3, 5	Figure 4	200	BGA Heat Sink	20
Figure 7, Figure 9	3.3, 5	Figure 4	400	BGA Heat Sink	18

Table 3. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 10, Figure 12	3.3, 5	Figure 5	0	None	25
Figure 10, Figure 12	3.3, 5	Figure 5	200	None	21
Figure 10, Figure 12	3.3, 5	Figure 5	400	None	21
Figure 11, Figure 13	3.3, 5	Figure 5	0	BGA Heat Sink	21
Figure 11, Figure 13	3.3, 5	Figure 5	200	BGA Heat Sink	18
Figure 11, Figure 13	3.3, 5	Figure 5	400	BGA Heat Sink	16

Table 4. Output Voltage Response Versus Component Matrix (Refer to Figure 17), 0A to 2A Load Step Typical Measured Values

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT} (CERAMIC)	C_{COMP}	V_{IN} (V)	DROOP (mV)	PEAK-TO-PEAK(mV)	RECOVERY (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)
1.2	10µF	56µF Aluminum	100µF 6.3V	None	2.5	21	43	10	2	10
1.2	10µF	56µF Aluminum	22µF ×4	None	3.3	23	45	10	2	10
1.2	10µF	56µF Aluminum	22µF ×4	None	5	24	46	10	2	10
1.5	10µF	56µF Aluminum	100µF 6.3V	None	2.5	19	41	10	2	5.76
1.5	10µF	56µF Aluminum	22µF ×4	None	3.3	21	43	10	2	5.76
1.5	10µF	56µF Aluminum	22µF ×4	None	5	21	43	10	2	5.76
1.8	10µF	56µF Aluminum	100µF 6.3V	None	2.5	25	50	10	2	4.02
1.8	10µF	56µF Aluminum	22µF ×3	None	3.3	30	60	10	2	4.02
1.8	10µF	56µF Aluminum	22µF ×3	None	5	30	60	10	2	4.02
2.5	10µF	56µF Aluminum	100µF 6.3V	None	2.5	22	45	12	2	2.37
2.5	10µF	56µF Aluminum	22µF ×3	None	3.3	25	55	12	2	2.37
2.5	10µF	56µF Aluminum	22µF ×3	None	5	25	55	12	2	2.37
3.3	10µF	56µF Aluminum	100µF 6.3V	None	2.5	22	50	15	2	1.62
3.3	10µF	56µF Aluminum	22µF ×3	None	3.3	25	56	15	2	1.62
3.3	10µF	56µF Aluminum	22µF ×3	None	5	25	56	15	2	1.62

APPLICATIONS INFORMATION

Safety Considerations

The LTM4604A µModule regulator does not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

Layout Checklist/Example

The high integration of LTM4604A makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pads unless they are capped.
- SW pads can be soldered to board to improve thermal performance.

Figure 14 gives a good example of the recommended layout.

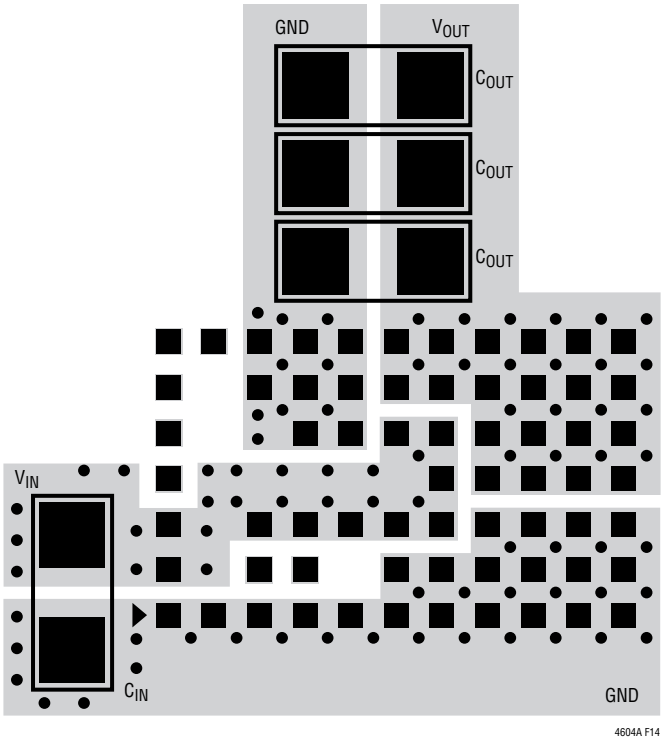


Figure 14. Recommended PCB Layout (LGA Shown, for BGA Use Circle Pads)

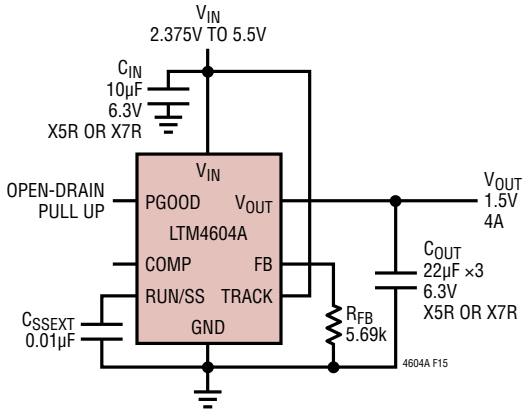


Figure 15. Typical 2.375V to 5.5V Input, 1.5V at 4A Design

TYPICAL APPLICATIONS

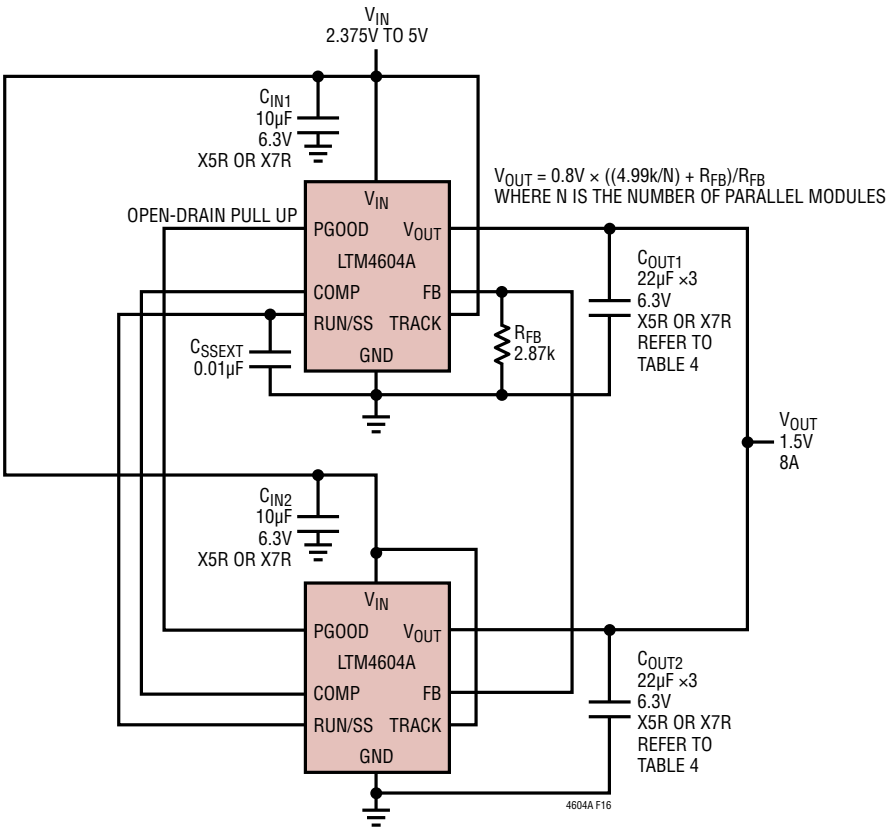


Figure 16. Two LTM4604As in Parallel, 1.5V at 8A Design

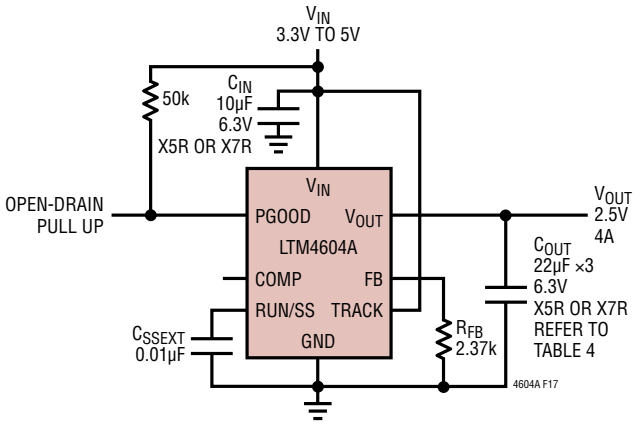
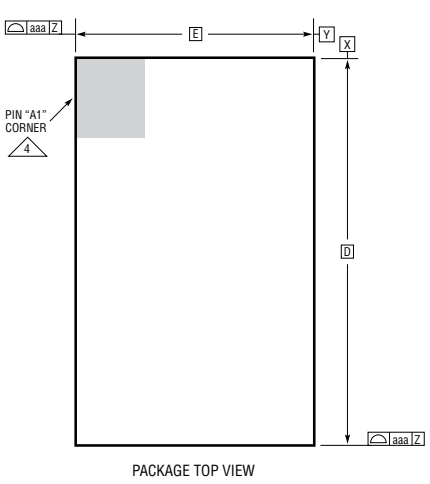


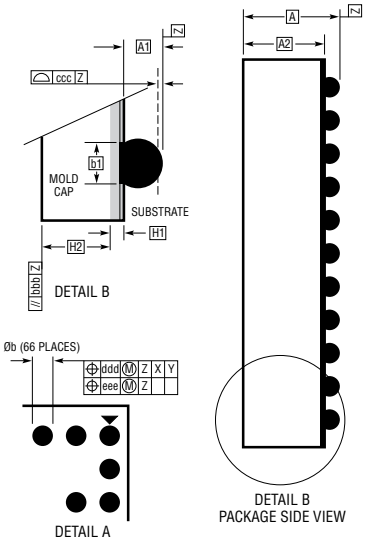
Figure 17. 3.3V to 5V Input, 2.5V at 4A Design

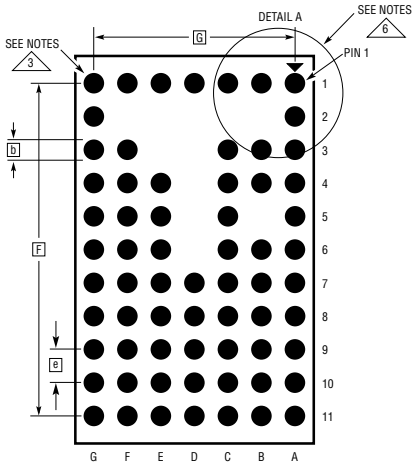
PACKAGE DESCRIPTION

BGA Package
66-Lead (15.00mm × 9.00mm × 3.42mm)
(Reference LTC DWG# 05-08-1954 Rev A)

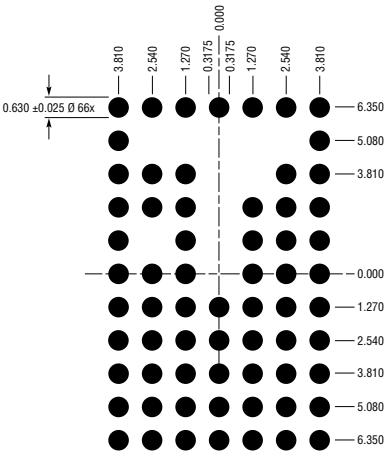


PACKAGE TOP VIEW





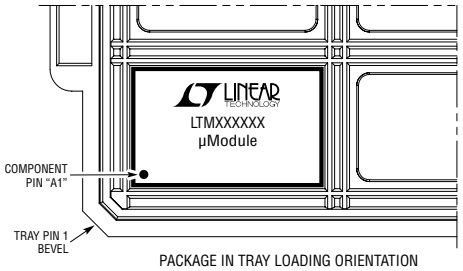
PACKAGE BOTTOM VIEW



SUGGESTED PCB LAYOUT
TOP VIEW

DIMENSIONS				
SYMBOL	**MIN**	**NOM**	**MAX**	**NOTES**
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	BALL HT
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		15.00		
E		9.00		
e		1.27		
F		12.70		
G		7.62		
H1	0.27	0.32	0.37	SUBSTRATE THK
H2	2.45	2.50	2.55	MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 66				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

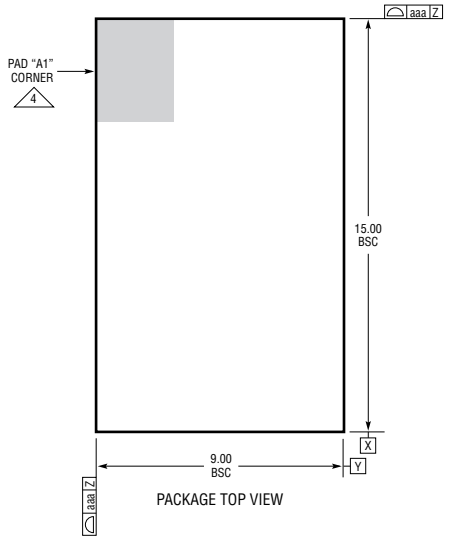


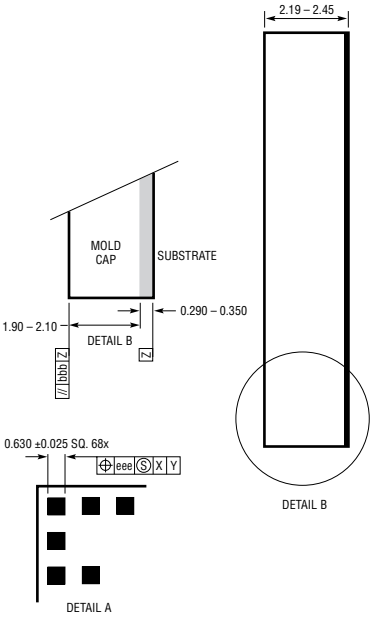
PACKAGE IN TRAY LOADING ORIENTATION

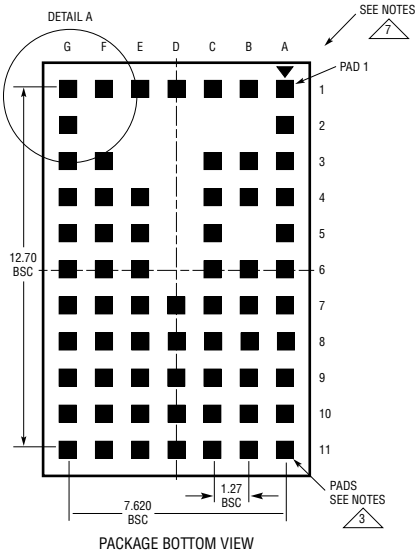
BGA 66 0517 REV A

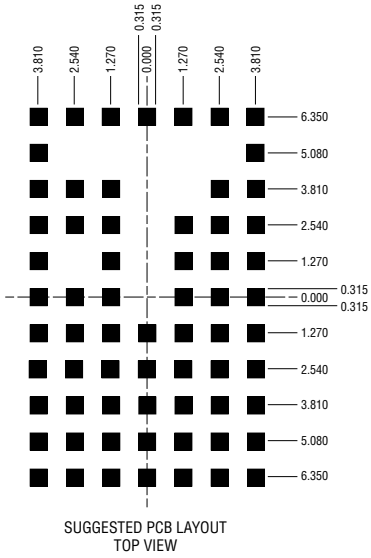
PACKAGE DESCRIPTION

LGA Package
66-Lead (15mm × 9mm × 2.32mm)
(Reference LTC DWG # 05-08-1820 Rev A)



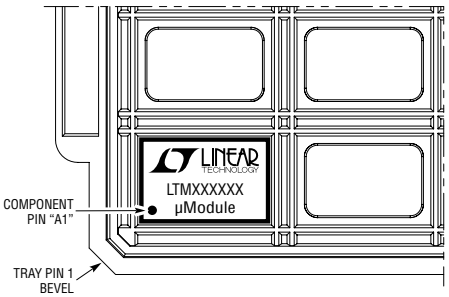






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 66
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

SYMBOL	TOLERANCE
aaa	0.15
bbb	0.10
eee	0.05



PACKAGE DESCRIPTION

Pin Assignment Table
(Arranged by Pin Number)

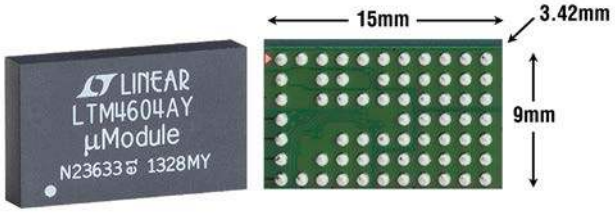
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	B1	V_{IN}	C1	V_{IN}	D1	RUN/SS
A2	GND	B2	–	C2	–	D2	–
A3	GND	B3	SW	C3	V_{IN}	D3	–
A4	GND	B4	SW	C4	V_{IN}	D4	–
A5	GND	B5	–	C5	V_{IN}	D5	–
A6	GND	B6	GND	C6	V_{IN}	D6	–
A7	GND	B7	GND	C7	V_{IN}	D7	V_{IN}
A8	GND	B8	GND	C8	GND	D8	V_{OUT}
A9	GND	B9	GND	C9	GND	D9	V_{OUT}
A10	GND	B10	GND	C10	GND	D10	V_{OUT}
A11	GND	B11	GND	C11	GND	D11	V_{OUT}

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
E1	TRACK	F1	PGOOD	G1	COMP
E2	–	F2	–	G2	FB
E3	–	F3	GND	G3	GND
E4	GND	F4	GND	G4	GND
E5	GND	F5	GND	G5	GND
E6	V_{IN}	F6	V_{OUT}	G6	V_{OUT}
E7	V_{IN}	F7	V_{OUT}	G7	V_{OUT}
E8	V_{OUT}	F8	V_{OUT}	G8	V_{OUT}
E9	V_{OUT}	F9	V_{OUT}	G9	V_{OUT}
E10	V_{OUT}	F10	V_{OUT}	G10	V_{OUT}
E11	V_{OUT}	F11	V_{OUT}	G11	V_{OUT}

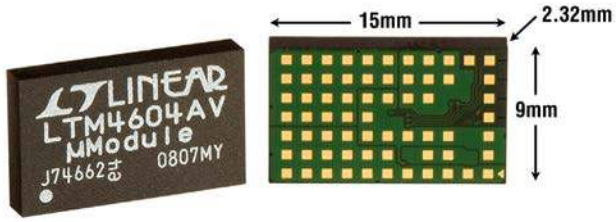
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/13	Added BGA package option	Throughout
		Updated Minimum Input Voltage graph	5
		Added output current information to Load Transient Response curves	5
		Updated RUN/SS pin description	7
		Updated Run Enable and Soft-Start section	11
B	05/14	Add SnPb BGA package option	1, 2
		Update Block Diagram	8
C	09/14	Update Block Diagram	8
D	04/21	Clarified LGA/BGA Reflow temp and updated MSL to 4	2

PACKAGE PHOTOGRAPH

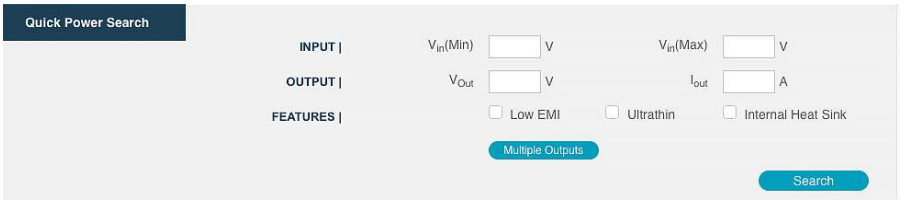


4604A BGA Package



4604A LGA Package

DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. 	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4624	Wider V_{IN} range than LTM4604A, 0.5cm2 solution size (dual sided PCB)	2.375V ≤ V_{IN} ≤ 14V, low V_{IN} requires auxiliary V_{BIAS}, 0.6V ≤ V_{OUT} ≤ 5.5V, 6.25mm x 6.25mm x 5.01mm BGA
LTM4615	Triple output, 4A, 4A, 1.5A	2.375 ≤ V_{IN} ≤ 5.5V, auxiliary V_{BIAS} not required
LTM4644	Wider V_{IN} range (up to 14V), Quad output, 4A each	2.375V ≤ V_{IN} ≤ 14V, low V_{IN} requires auxiliary V_{BIAS}, 0.6V ≤ V_{OUT} ≤ 5.5V, current share to 16A, 9mm x 15mm x 5.01mm BGA
LTM4619	Wider V_{IN} range (up to 26V), Dual output, 4A each	4.5V ≤ V_{IN} ≤ 26.5V, 0.8V ≤ V_{OUT} ≤ 5V, 15mm x 15mm x 2.82mm LGA
LTM8027	Wider V_{IN} range (up to 60V) and V_{OUT} range	4.5V ≤ V_{IN} ≤ 60V, 2.5V ≤ V_{OUT} ≤ 24V, 15mm x 15mm x 4.32mm LGA & 15mm x 15mm x 4.92mm BGA
LTM4608A	More current (8A)	2.7V ≤ V_{IN} ≤ 5.5V, 8A, 9mm x 15mm x 2.82mm LGA