# SN74ALVC164245-EP
# 16-BIT 2.5-V TO 3.3-V/3.3-V TO 5-V LEVEL-SHIFTING TRANSCEIVER WITH 3-STATE OUTPUTS

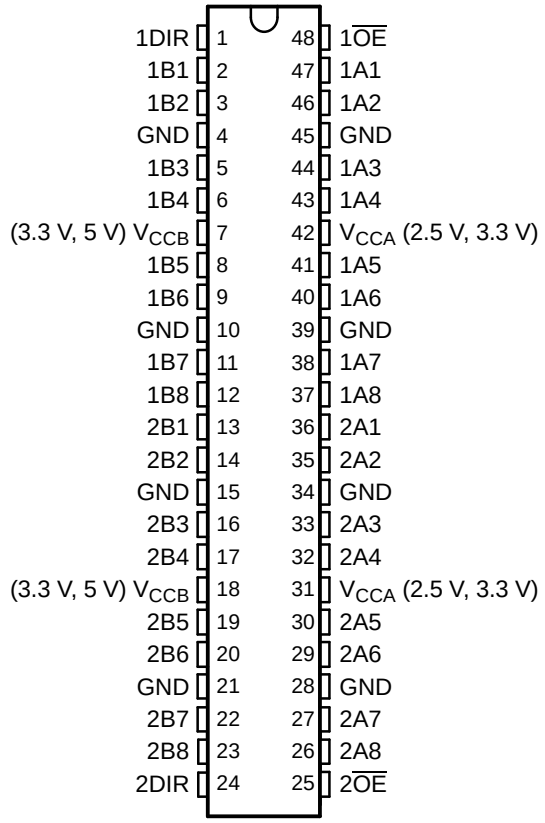
SCAS774A – JUNE 2004 – REVISED SEPTEMBER 2005

## FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree[1]**
- **Member of the Texas Instruments Widebus™ Family**
- **Max $t_{pd}$ of 5.8 ns at 3.3 V**
- **±24-mA Output Drive at 3.3 V**
- **Control Inputs $V_{IH}/V_{IL}$ Levels Are Referenced to $V_{CCA}$ Voltage**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

**DGG OR DL PACKAGE**
**(TOP VIEW)**




## DESCRIPTION/ORDERING INFORMATION

This 16-bit (dual-octal) noninverting bus transceiver contains two separate supply rails. B port has $V_{CCB}$, which is set to operate at 3.3 V and 5 V. A port has $V_{CCA}$, which is set to operate at 2.5 V and 3.3 V. This allows for translation from a 2.5-V to a 3.3-V environment, and vice versa, or from a 3.3-V to a 5-V environment, and vice versa.

The SN74ALVC164245 is designed for asynchronous communication between data buses. The control circuitry (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) is powered by $V_{CCA}$.

To ensure the high-impedance state during power up or power down, the output-enable ($\overline{OE}$) input should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**ORDERING INFORMATION**

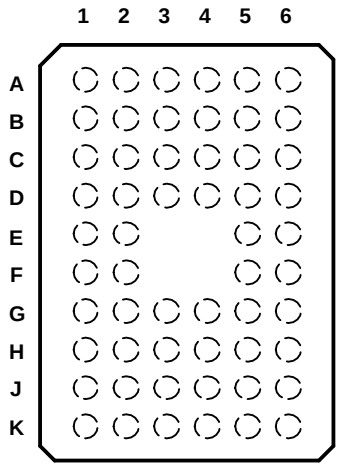
| $T_A$ | PACKAGE[1] | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | SSOP – DL | Reel of 1000 | CALVC164245IDLREP | ALVC164245 |
| | TSSOP – DGG | Reel of 2000 | CALVC164245IDGGREP | ALVC164245 |
| | VFBGA – GQL | Reel of 1000 | CALVC164245IGQLREP | VC4245EP |
| | VFBGA – ZQL (Pb-free) | | CALVC164245IZQLREP | |
| –55°C to 125°C | TSSOP – DGG | Reel of 2000 | CALVC164245MDGGREP | C164245MEP |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

**GQL OR ZQL PACKAGE**
**(TOP VIEW)**




**TERMINAL ASSIGNMENTS**(1)

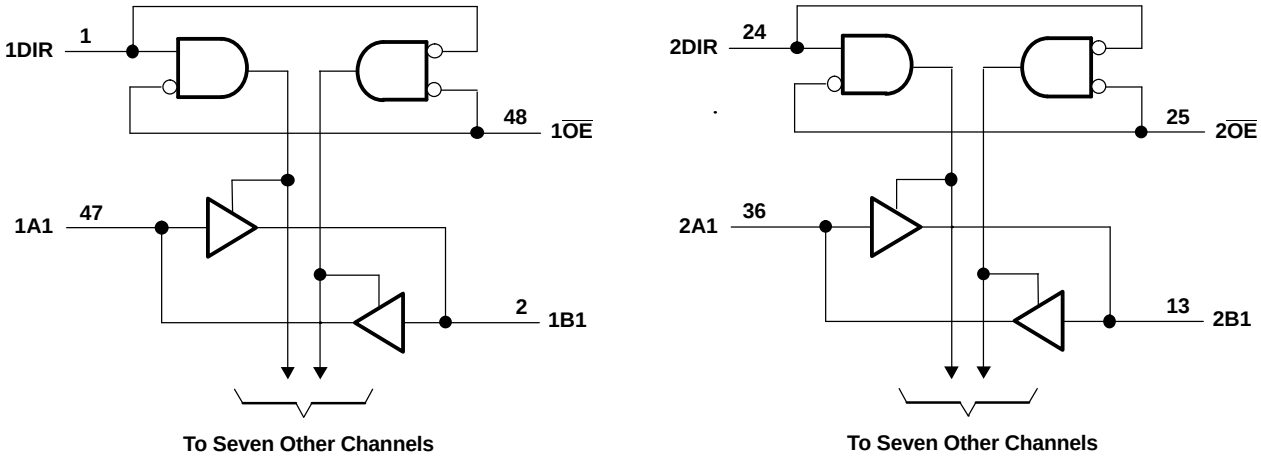
| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **A** | 1DIR | NC | NC | NC | NC | 1$\overline{OE}$ |
| **B** | 1B2 | 1B1 | GND | GND | 1A1 | 1A2 |
| **C** | 1B4 | 1B3 | $V_{CCB}$ | $V_{CCA}$ | 1A3 | 1A4 |
| **D** | 1B6 | 1B5 | GND | GND | 1A5 | 1A6 |
| **E** | 1B8 | 1B7 | | | 1A7 | 1A8 |
| **F** | 2B1 | 2B2 | | | 2A2 | 2A1 |
| **G** | 2B3 | 2B4 | GND | GND | 2A4 | 2A3 |
| **H** | 2B5 | 2B6 | $V_{CCB}$ | $V_{CCA}$ | 2A6 | 2A5 |
| **J** | 2B7 | 2B8 | GND | GND | 2A8 | 2A7 |
| **K** | 2DIR | NC | NC | NC | NC | 2$\overline{OE}$ |

(1) NC – No internal connection

**FUNCTION TABLE**
**(EACH 8-BIT SECTION)**

| INPUTS | | OPERATION |
|---|---|---|
| $\overline{OE}$ | DIR | |
| L | L | B data to A bus |
| L | H | A data to B bus |
| H | X | Isolation |

### LOGIC DIAGRAM (POSITIVE LOGIC)




Pin numbers shown are for the DGG and DL packages.

## Absolute Maximum Ratings(1)

over operating free-air temperature range for $V_{CCB}$ at 5 V and $V_{CCA}$ at 3.3 V (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage range | | –0.5 | 4.6 | V |
| $V_{CCB}$ | | | –0.5 | 6 | |
| $V_I$ | Input voltage range | Except I/O ports(2) | –0.5 | 6 | V |
| | | I/O port A(3) | –0.5 | $V_{CCA}$ + 0.5 | |
| | | I/O port B(2) | –0.5 | $V_{CCB}$ + 0.5 | |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through each $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | DGG package | | 70 | °C/W |
| | | DL package | | 63 | |
| | | GQL/ZQL package | | 42 | |
| $T_{stg}$ | Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 6 V maximum.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions(1)

for $V_{CCB}$ at 3.3 V and 5 V

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCB}$ | Supply voltage | | 3 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | $V_{CCB}$ = 3 V to 3.6 V | | 0.7 | V |
| | | $V_{CCB}$ = 4.5 V to 5.5 V | | 0.8 | |
| $V_{IB}$ | Input voltage | | 0 | $V_{CCB}$ | V |
| $V_{OB}$ | Output voltage | | 0 | $V_{CCB}$ | V |
| $I_{OH}$ | High-level output current | | | –24 | mA |
| $I_{OL}$ | Low-level output current | | | 24 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | CALVC16245I | –40 | 85 | °C |
| | | CALVC16245M | –55 | 125 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Recommended Operating Conditions(1)

for $V_{CCA}$ at 2.5 V and 3.3 V

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | 2.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CCA}$ = 2.3 V to 2.7 V | 1.7 | | V |
| | | $V_{CCA}$ = 3 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CCA}$ = 2.3 V to 2.7 V | | 0.7 | V |
| | | $V_{CCA}$ = 3 V to 3.6 V | | 0.8 | |
| $V_{IA}$ | Input voltage | | 0 | $V_{CCA}$ | V |
| $V_{OA}$ | Output voltage | | 0 | $V_{CCA}$ | V |
| $I_{OH}$ | High-level output current | $V_{CCA}$ = 2.3 V | | –18 | mA |
| | | $V_{CCA}$ = 3 V | | –24 | |
| $I_{OL}$ | Low-level output current | $V_{CCA}$ = 2.3 V | | 18 | mA |
| | | $V_{CCA}$ = 3 V | | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | CALVC16245I | –40 | 85 | °C |
| | | CALVC16245M | –55 | 125 | |

(1) All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range for $V_{CCA}$ = 2.7 V to 3.6 V and $V_{CCB}$ = 4.5 V to 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | CALVC164245I | | | CALVC164245M | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP(1) | MAX | MIN | TYP(1) | MAX | |
| $V_{OH}$ | B to A | $I_{OH}$ = –100 μA | 2.7 V to 3.6 V | | $V_{CC}$ – 0.2 | | | $V_{CC}$ – 0.2 | | | V |
| | | $I_{OH}$ = –12 mA | 2.7 V | | 2.2 | | | 2.2 | | | |
| | | | 3 V | | 2.4 | | | 2.4 | | | |
| | | $I_{OH}$ = –24 mA | 3 V | | 2 | | | 2 | | | |
| | A to B | $I_{OL}$ = 100 μA | | 4.5 V | 4.3 | | | 4.3 | | | |
| | | | | 5.5 V | 5.3 | | | 5.3 | | | |
| | | $I_{OL}$ = 24 mA | | 4.5 V | 3.7 | | | 3.7 | | | |
| | | | | 5.5 V | 4.7 | | | 4.7 | | | |
| $V_{OL}$ | B to A | $I_{OL}$ = 100 μA | 2.7 V to 3.6 V | | | | 0.2 | | | 0.2 | V |
| | | $I_{OL}$ = 12 mA | 2.7 V | | | | 0.4 | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3 V | | | | 0.55 | | | 0.55 | |
| | A to B | $I_{OL}$ = 100 μA | | 4.5 V to 5.5 V | | | 0.2 | | | 0.2 | |
| | | $I_{OL}$ = 24 mA | | 4.5 V to 5.5 V | | | 0.55 | | | 0.55 | |
| $I_I$ | Control inputs | $V_I = V_{CCA}/V_{CCB}$ or GND | 3.6 V | 5.5 V | | | ±5 | | | ±5 | μA |
| $I_{OZ}$(2) | A or B port | $V_O = V_{CCA}/V_{CCB}$ or GND | 3.6 V | 5.5 V | | | ±10 | | | ±10 | μA |
| $I_{CC}$ | | $V_I = V_{CCA}/V_{CCB}$ or GND, $I_O$ = 0 | 5.5 V | 5.5 V | | | 40 | | | 40 | μA |
| $\Delta I_{CC}$(3) | | One input at $V_{CCA}/V_{CCB}$ – 0.6 V, Other inputs at $V_{CCA}/V_{CCB}$ or GND | 3 V to 3.6 V | 4.5 V to 5.5 V | | | 750 | | | 750 | μA |
| $C_i$ | Control inputs | $V_I = V_{CCA}/V_{CCB}$ or GND | 3.3 V | 5 V | | 6.5 | | | 6.5 | | pF |
| $C_{io}$ | A or B port | $V_O = V_{CCA}/V_{CCB}$ or GND | 3.3 V | 3.3 V | | 8.5 | | | 8.5 | | pF |

(1) All typical values are at $V_{CCA}$ = 3.3 V and $V_{CCB}$ = 5 V, $T_A$ = 25°C.
(2) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(3) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than at 0 or the associated $V_{CC}$.

## Electrical Characteristics

over recommended operating free-air temperature range for $V_{CCA}$ = 2.3 V to 2.7 V and $V_{CCB}$ = 3 V to 3.6 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CCA}$ | $V_{CCB}$ | CALVC164245I | | CALVC164245M | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | B to A | $I_{OH}$ = –100 μA | 2.3 V to 2.7 V | 3 V to 3.6 V | $V_{CCA}$ – 0.2 | | $V_{CCA}$ – 0.2 | | V |
| | | $I_{OH}$ = –8 mA | 2.3 V | 3 V to 3.6 V | 1.7 | | 1.7 | | |
| | | $I_{OH}$ = –12 mA | 2.7 V | 3 V to 3.6 V | 1.8 | | 1.8 | | |
| | A to B | $I_{OL}$ = 100 μA | 2.3 V to 2.7 V | 3 V to 3.6 V | $V_{CCB}$ – 0.2 | | $V_{CCB}$ – 0.2 | | |
| | | $I_{OL}$ = 18 mA | 2.3 V to 2.7 V | 3 V | 2.2 | | 2.2 | | |
| $V_{OL}$ | B to A | $I_{OL}$ = 100 μA | 2.3 V to 2.7 V | 3 V to 3.6 V | | 0.2 | | 0.2 | V |
| | | $I_{OL}$ = 12 mA | 2.3 V | 3 V to 3.6 V | | 0.6 | | 0.6 | |
| | A to B | $I_{OL}$ = 100 μA | 2.3 V to 2.7 V | 3 V to 3.6 V | | 0.2 | | 0.2 | |
| | | $I_{OL}$ = 18 mA | 2.3 V | 3 V | | 0.55 | | 0.55 | |
| $I_I$ | Control inputs | $V_I = V_{CCA}/V_{CCB}$ or GND | 2.3 V to 2.7 V | 3 V to 3.6 V | | ±5 | | ±5 | μA |
| $I_{OZ}$ (1) | A or B port | $V_O = V_{CCA}/V_{CCB}$ or GND | 2.3 V to 2.7 V | 3 V to 3.6 V | | ±10 | | ±10 | μA |
| $I_{CC}$ | | $V_I = V_{CCA}/V_{CCB}$ or GND, $I_O$ = 0 | 2.3 V to 2.7 V | 3 V to 3.6 V | | 20 | | 40 | μA |
| $\Delta I_{CC}$ (2) | | One input at $V_{CCA}/V_{CCB}$ – 0.6 V, Other inputs at $V_{CCA}/V_{CCB}$ or GND | 2.3 V to 2.7 V | 3 V to 3.6 V | | 750 | | 750 | μA |

(1) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than at 0 or the associated $V_{CC}$.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CALVC16245I | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | | | |
| | | | $V_{CCA}$ = 2.5 V ± 0.2 V | | $V_{CCA}$ = 2.7 V | | $V_{CCA}$ = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | | 7.6 | | 5.9 | 1 | 5.8 | ns |
| | B | A | | 7.6 | | 6.7 | 1.2 | 5.8 | |
| $t_{en}$ | $\overline{OE}$ | B | | 11.5 | | 9.3 | 1 | 8.9 | ns |
| $t_{dis}$ | $\overline{OE}$ | B | | 10.5 | | 9.2 | 2.1 | 9.5 | ns |
| $t_{en}$ | $\overline{OE}$ | A | | 12.3 | | 10.2 | 2 | 9.1 | ns |
| $t_{dis}$ | $\overline{OE}$ | A | | 9.3 | | 9 | 2.9 | 8.6 | ns |

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CALVC16245M | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CCB}$ = 3.3 V ± 0.3 V | | $V_{CCB}$ = 5 V ± 0.5 V | | | | |
| | | | $V_{CCA}$ = 2.5 V ± 0.2 V | | $V_{CCA}$ = 2.7 V | | $V_{CCA}$ = 3.3 V ± 0.3 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{pd}$ | A | B | | 8.6 | | 6.9 | 1 | 6.8 | ns |
| | B | A | | 8.6 | | 7.7 | 1.2 | 6.8 | |
| $t_{en}$ | $\overline{OE}$ | B | | 12.5 | | 10.3 | 1 | 9.9 | ns |
| $t_{dis}$ | $\overline{OE}$ | B | | 11.5 | | 10.2 | 2.1 | 10.5 | ns |
| $t_{en}$ | $\overline{OE}$ | A | | 14.5 | | 11.2 | 2 | 10.1 | ns |
| $t_{dis}$ | $\overline{OE}$ | A | | 11.3 | | 11 | 2.9 | 10.6 | ns |

## Operating Characteristics

$T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | $V_{CCB}$ = 3.3 V | $V_{CCB}$ = 5 V | UNIT |
|---|---|---|---|---|---|
| | | | $V_{CCA}$ = 2.5 V | $V_{CCA}$ = 3.3 V | |
| | | | TYP | TYP | |
| $C_{pd}$ Power dissipation capacitance | Outputs enabled (B) | $C_L$ = 50 pF, f = 10 MHz | 55 | 56 | pF |
| | Outputs disabled (B) | | 27 | 6 | |
| | Outputs enabled (A) | $C_L$ = 50 pF, f = 10 MHz | 118 | 56 | |
| | Outputs disabled (A) | | 58 | 6 | |

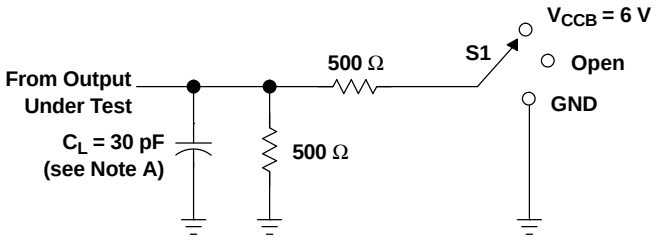
## Power-Up Considerations(1)

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. To guard against such power-up problems, take these precautions:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device ($V_{CCA}$ for all four of these devices).
3. Tie $\overline{OE}$ to $V_{CCA}$ with a pullup resistor so that it ramps with $V_{CCA}$.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with $V_{CCA}$. Otherwise, keep DIR low.

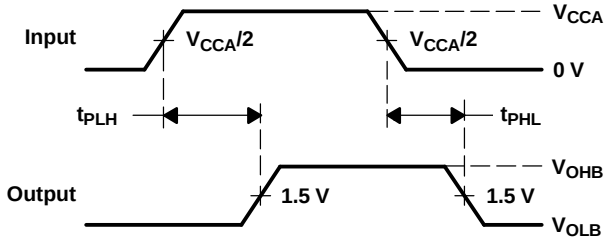
(1) Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

## PARAMETER MEASUREMENT INFORMATION
## $V_{CCA}$ = 2.5 V ± 0.2 V to $V_{CCB}$ = 3.3 V ± 0.3 V

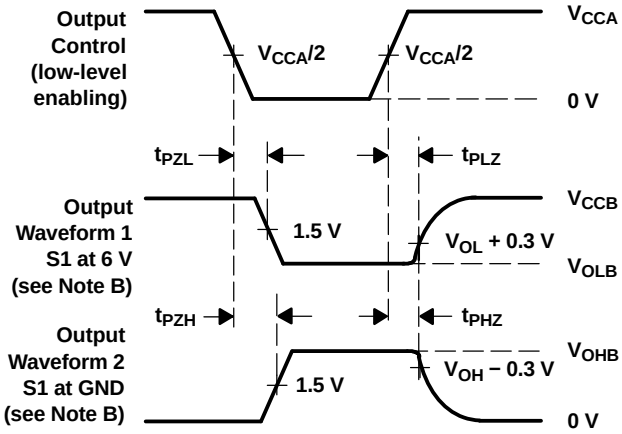



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CCB}$ = 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

LOAD CIRCUIT




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

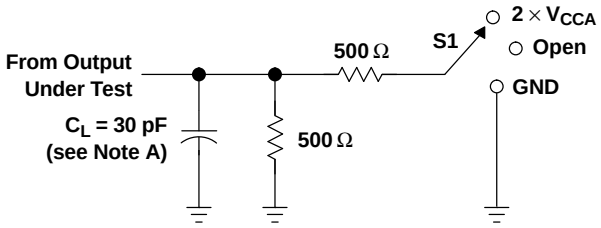



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, $Z_O$ = 50 Ω, $t_r$≤2 ns, $t_f$≤2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

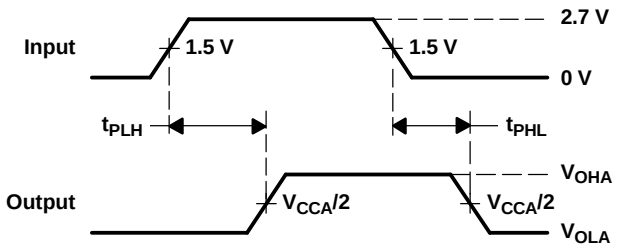
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CCB}$ = 3.3 V ± 0.3 V to $V_{CCA}$ = 2.5 V ± 0.2 V

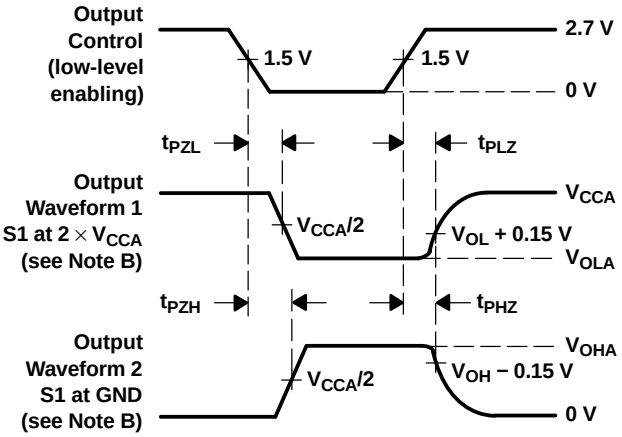



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CCA}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

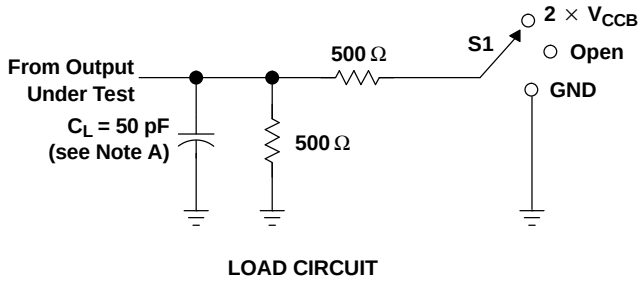



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, $Z_O$ = 50 Ω, $t_r$≤2 ns, $t_f$≤2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

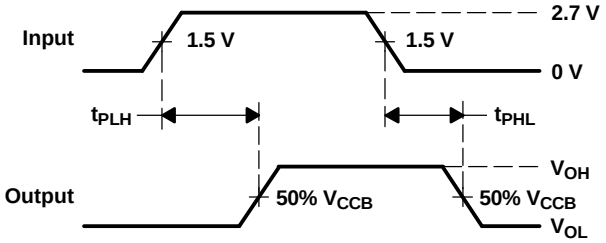
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CCA}$ = 3.3 V ± 0.3 V to $V_{CCB}$ = 5 V ± 0.5 V

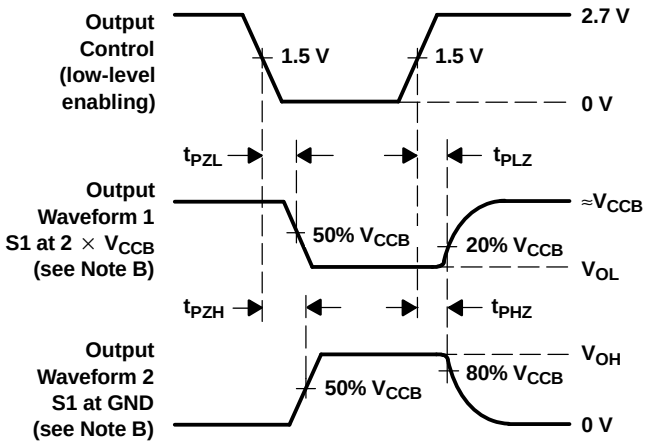



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CCB}$ |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

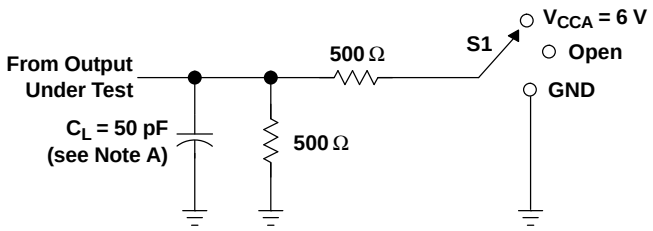



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

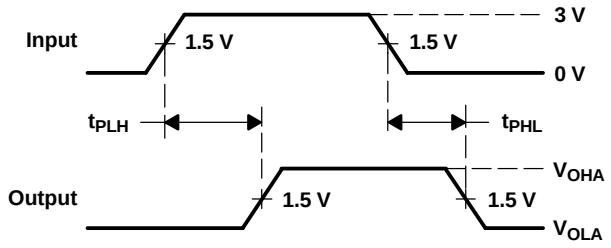
**Figure 3. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CCB}$ = 5 V ± 0.5 V to $V_{CCA}$ = 2.7 V and 3.3 V ± 0.3 V

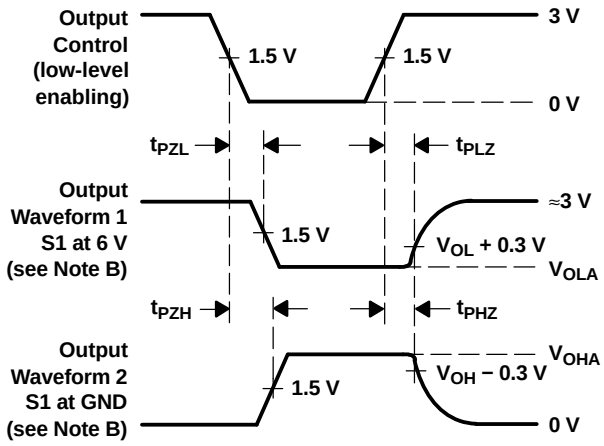



LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CCA}$ = 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

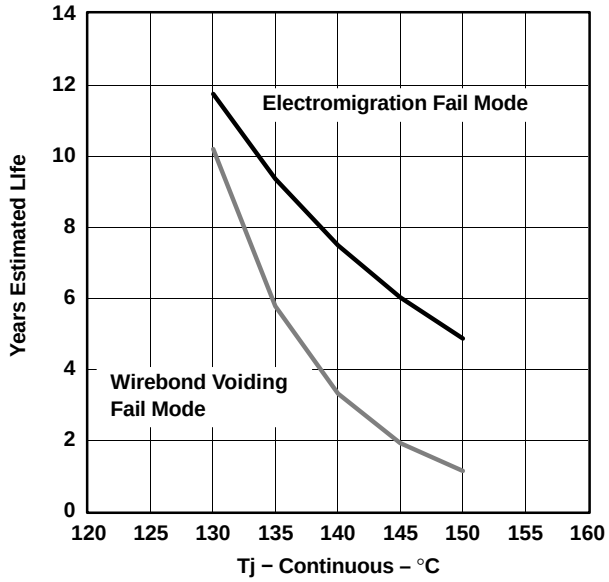



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 4. Load Circuit and Voltage Waveforms**

**74ALVC164245MDGG*EP**
**Estimated Device Life at Elevated Temperatures Electromigration and Wirebond Voiding Fail Modes**




A. Silicon operating life design goal is 10 years at 105°C junction temperature.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CALVC164245IDGGREP | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVC164245 | Samples |
| CALVC164245IDLREP | ACTIVE | SSOP | DL | 48 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVC164245 | Samples |
| CALVC164245MDGGREP | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | C164245MEP | Samples |
| V62/05612-01XE | ACTIVE | SSOP | DL | 48 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVC164245 | Samples |
| V62/05612-01YE | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVC164245 | Samples |
| V62/05612-02YE | ACTIVE | TSSOP | DGG | 48 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | C164245MEP | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN74ALVC164245-EP :**

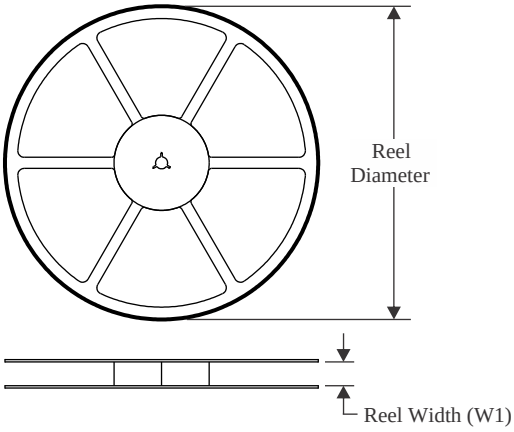
- Catalog: SN74ALVC164245

NOTE: Qualified Version Definitions:

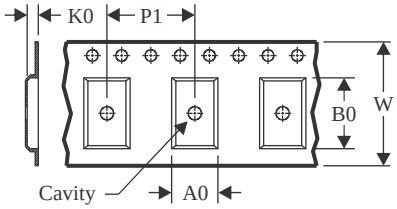
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

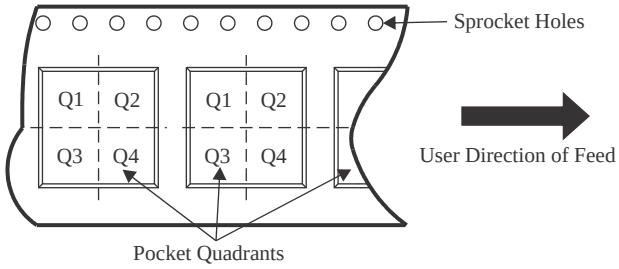



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

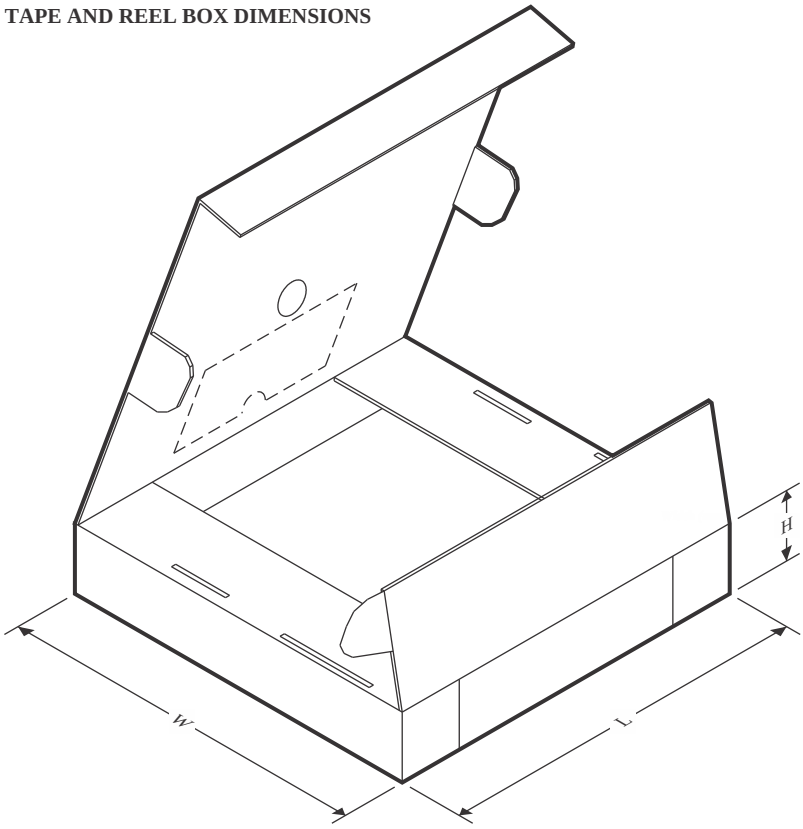
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CALVC164245IDGGREP | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |
| CALVC164245IDLREP | SSOP | DL | 48 | 1000 | 330.0 | 32.4 | 11.35 | 16.2 | 3.1 | 16.0 | 32.0 | Q1 |
| CALVC164245MDGGREP | TSSOP | DGG | 48 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |

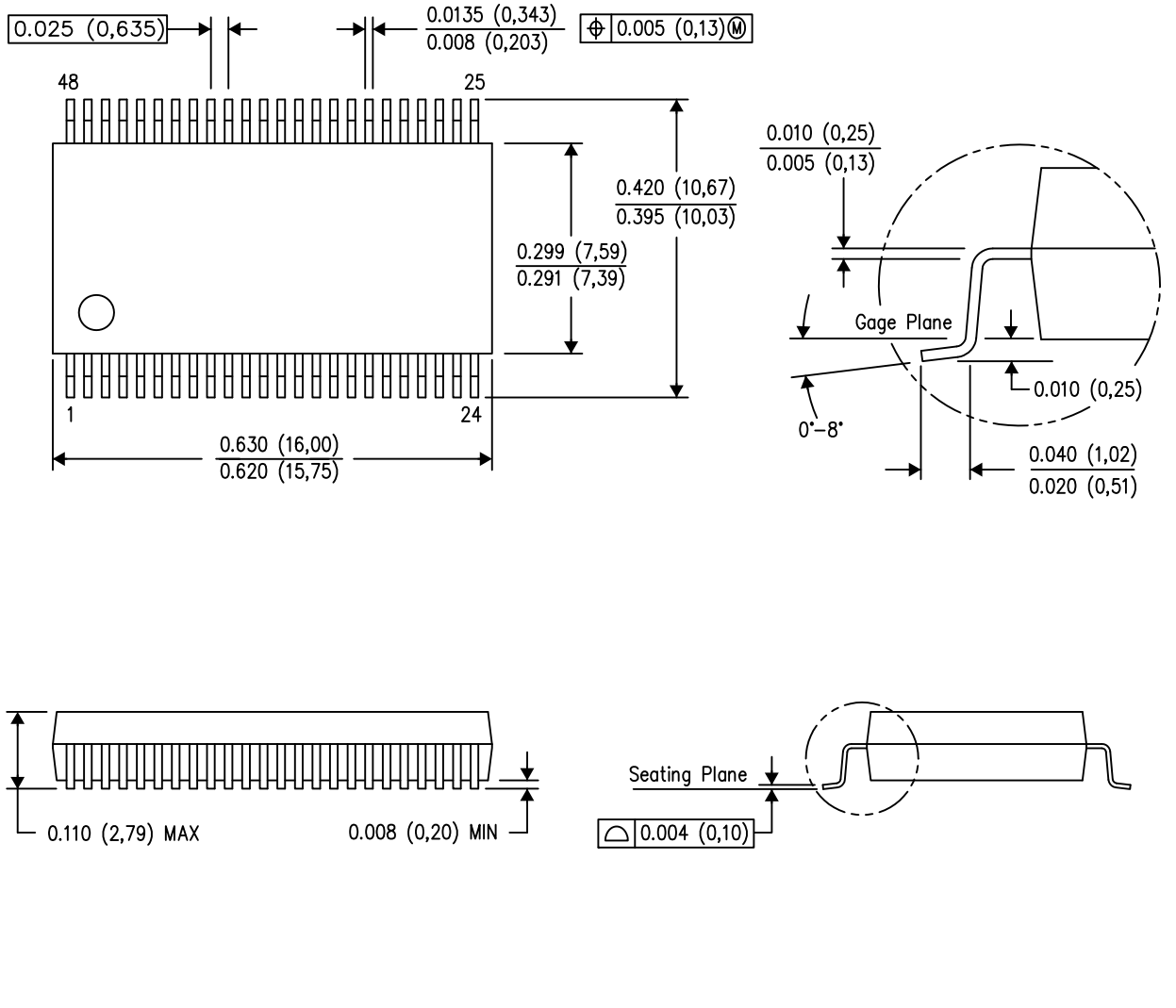
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CALVC164245IDGGREP | TSSOP | DGG | 48 | 2000 | 367.0 | 367.0 | 45.0 |
| CALVC164245IDLREP | SSOP | DL | 48 | 1000 | 367.0 | 367.0 | 55.0 |
| CALVC164245MDGGREP | TSSOP | DGG | 48 | 2000 | 356.0 | 356.0 | 41.0 |

DL (R–PDSO–G48) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

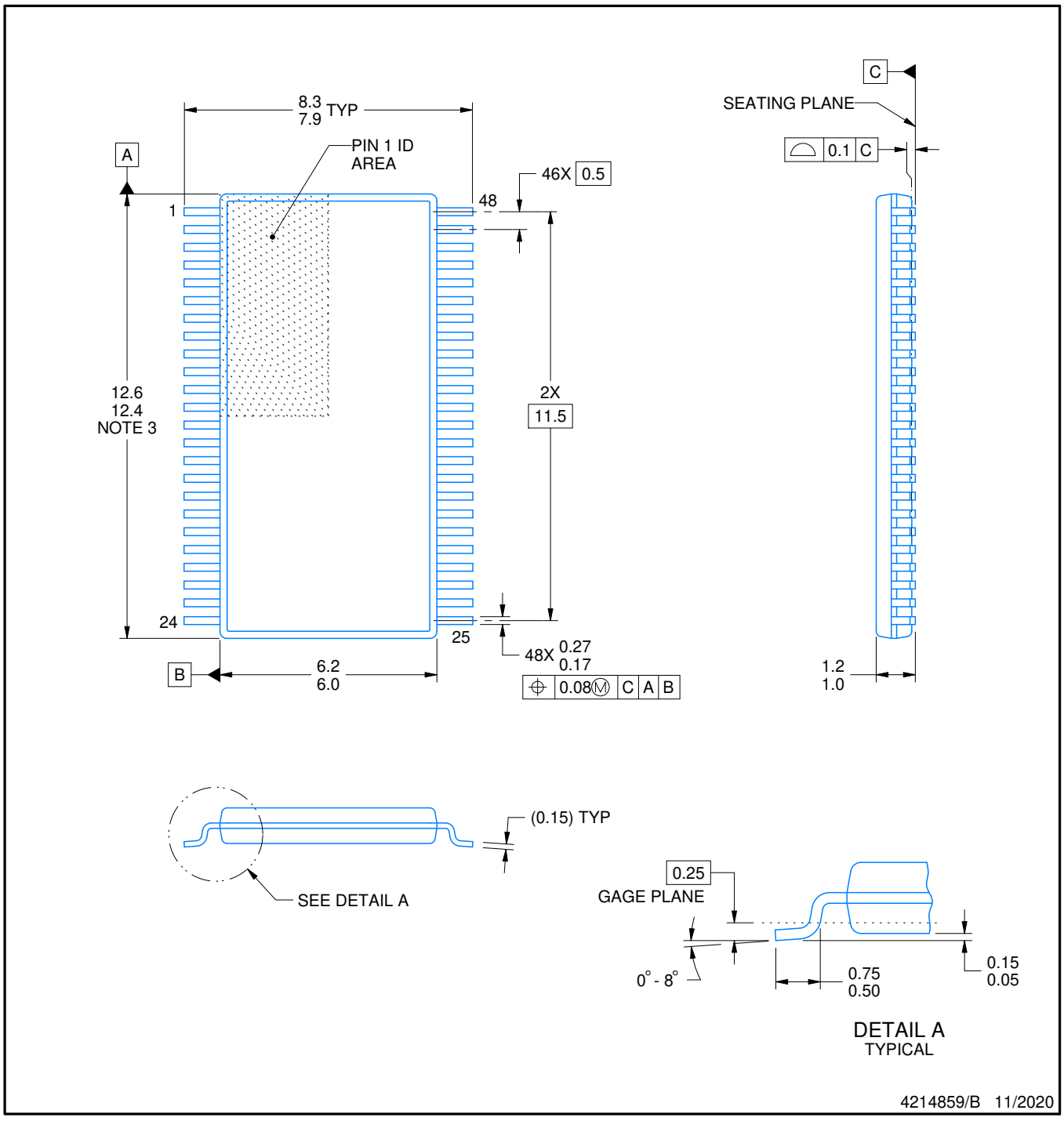
PowerPAD is a trademark of Texas Instruments.

# PACKAGE OUTLINE

## DGG0048A

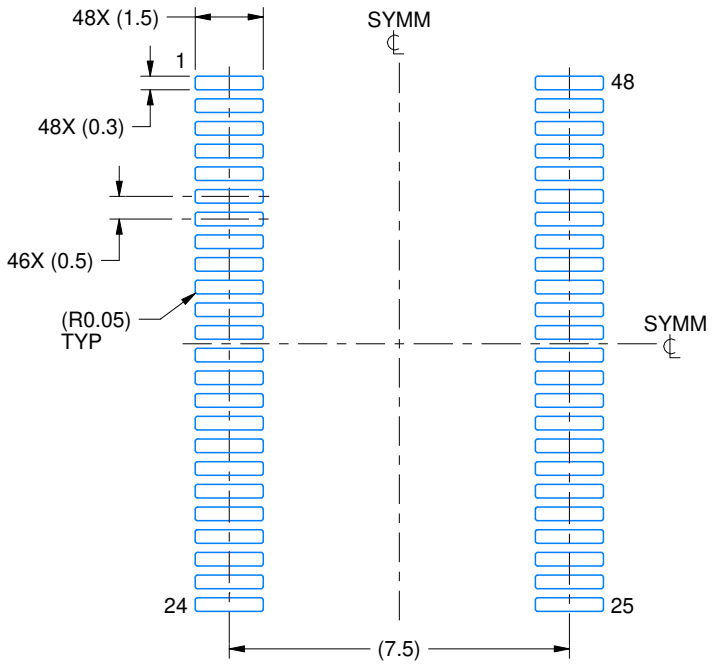
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

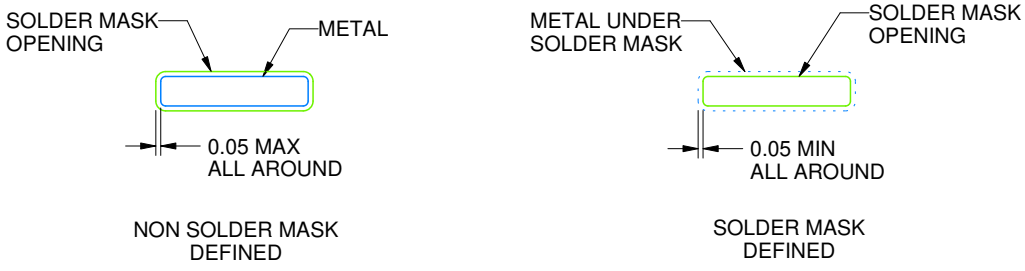



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
SCALE:6X

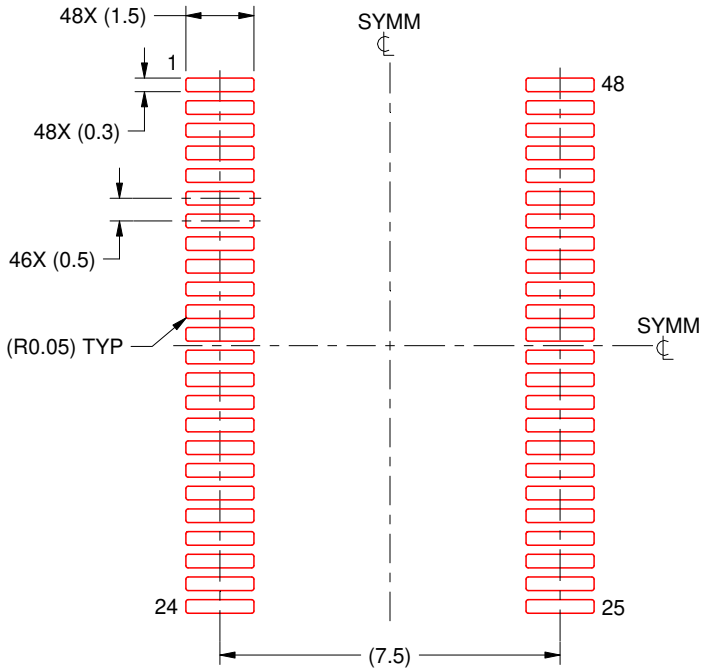



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4214859/B 11/2020

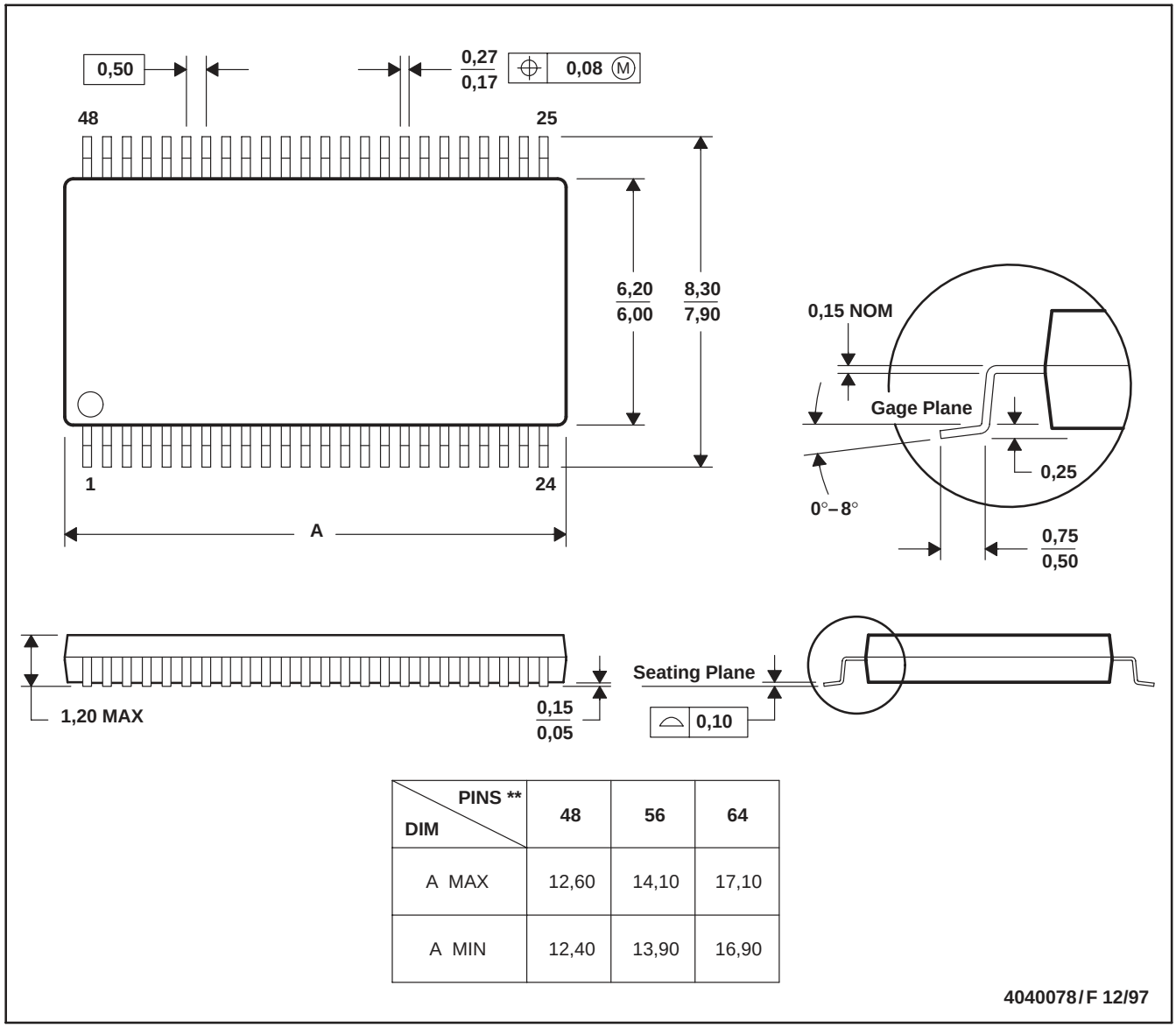
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MTSS003D – JANUARY 1995 – REVISED JANUARY 1998

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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