

FAN5026

Dual DDR/Dual-Output PWM Controller

Features

- Highly flexible dual synchronous switching PWM controller includes modes for:
 - DDR mode with in-phase operation for reduced channel interference
 - 90° phase shifted two-stage DDR Mode for reduced input ripple
 - Dual Independent regulators 180° phase shifted
- Complete DDR Memory power solution
 - VTT Tracks VDDQ/2
 - VDDQ/2 Buffered Reference Output
- Lossless current sensing on low-side MOSFET or Precision current sensing using sense resistor
- VCC Under-voltage Lockout
- Wide power input range: 3 to 16V
- Excellent dynamic response with Voltage Feed-Forward and Average Current Mode control
- Power-Good Signal
- Supports DDR-II and HSTL
- TSSOP28 package

Applications

- DDR V_{DDQ} and V_{TT} voltage generation
- Desktop computer
- Graphics cards

General Description

The FAN5026 PWM controller provides high efficiency and regulation for two output voltages adjustable in the range from 0.9V to 5.5V that are required to power I/O, chip-sets, and memory banks in high-performance computers, set top boxes, and VGA cards. Synchronous rectification contributes to high efficiency over a wide range of loads. Efficiency is even further enhanced by using MOSFET's $R_{DS(ON)}$ as a current sense component.

Feed-forward ramp modulation, average current mode control scheme, and internal feedback compensation provide fast response to load transients. Out-of-phase operation with 180° phase shift reduces input current ripple. The controller can be transformed into a complete DDR memory power supply solution by activating a designated pin. In DDR mode of operation one of the channels tracks the output voltage of another channel and provides output current sink and source capability — features essential for proper powering of DDR chips. The buffered reference voltage required by this type of memory is also provided. The FAN5026 monitors these outputs and generates separate PGx (power good) signals when the soft-start is completed and the output is within $\pm 10\%$ of its set point. A built-in over-voltage protection prevents the output voltage from going above 120% of the set point. Normal operation is automatically restored when the over-voltage conditions go away. Under-voltage protection latches the chip off when either output drops below 75% of its set value after the soft-start sequence for this output is completed. An adjustable over-current function monitors the output current by sensing the voltage drop across the lower MOSFET. If precision current-sensing is required, an external current-sense resistor may optionally be used.

Ordering Information

Part Number	Temperature Range	Package	Packing
FAN5026MTC	-40°C to 85°C	TSSOP-28	Rails
FAN5026MTCX	-40°C to 85°C	TSSOP-28	Tape and Reel

Block Diagrams

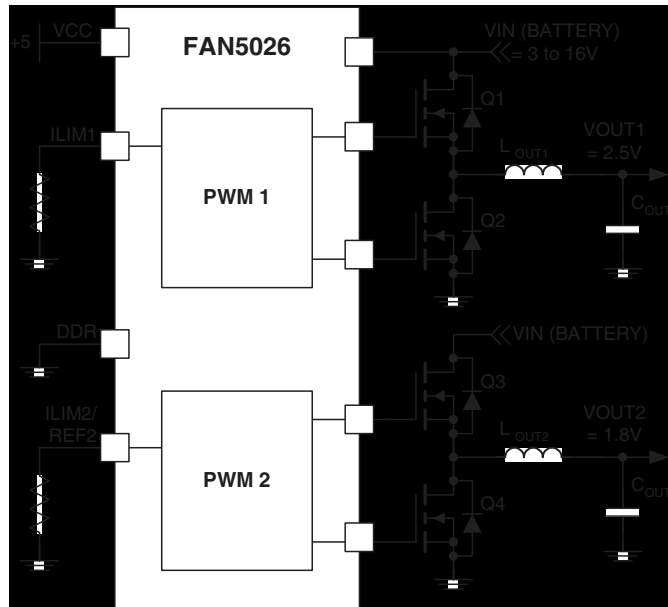


Figure 1. Dual Output Regulator

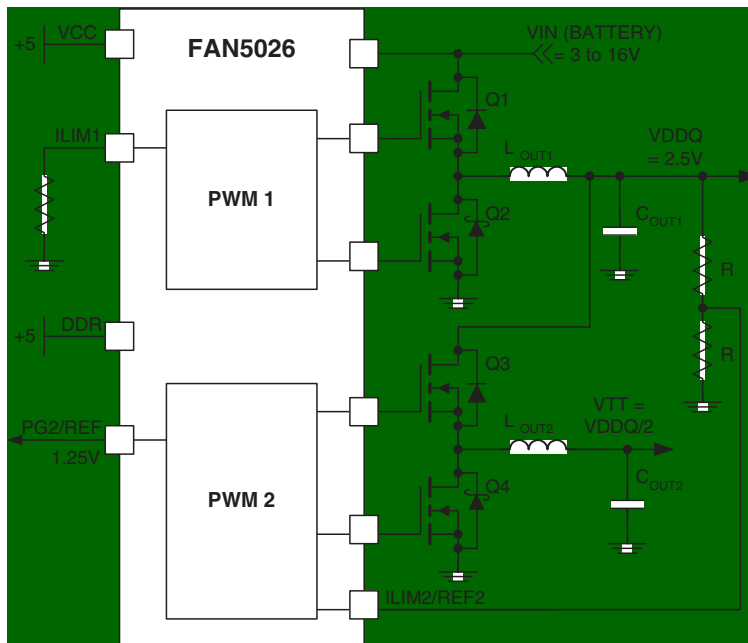
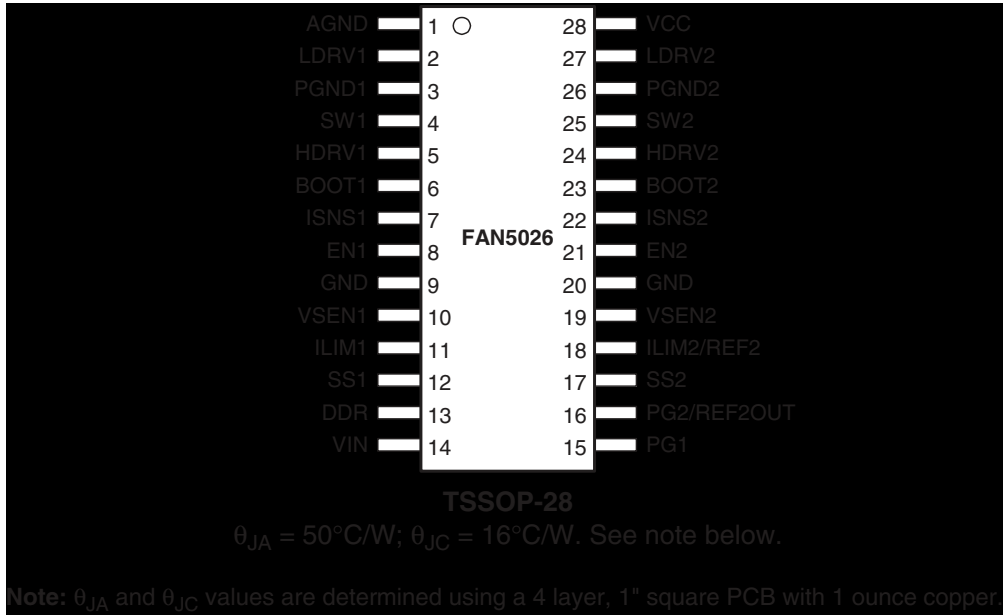


Figure 2. Typical Application

Pin Configurations



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	AGND	Analog Ground. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin.
2 27	LDRV1 LDRV2	Low-Side Drive. The low-side (lower) MOSFET driver output. Connect to gate of low-side MOSFET.
3 26	PGND1 PGND2	Power Ground. The return for the low-side MOSFET driver. Connect to source of low-side MOSFET.
4 25	SW1 SW2	Switching Node. Return for the high-side MOSFET driver and a current sense input. Connect to source of high-side MOSFET and low-side MOSFET drain.
5 24	HDRV1	High-Side Drive. High-side (upper) MOSFET driver output. Connect to gate of high-side MOSFET.
6 23	BOOT1 BOOT2	BOOT. Positive supply for the upper MOSFET driver. Connect as shown in Figure 3.
7 22	ISNS1 ISNS2	Current Sense Input. Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback.
8 21	EN1 EN2	Enable. Enables operation when pulled to logic high. Toggling EN will also reset the regulator after a latched fault condition. These are CMOS inputs whose state is indeterminate if left open.
9 20	GND	Ground. These pins should be tied to AGND for proper operation.
10 19	VSEN1 VSEN2	Output Voltage Sense. The feedback from the outputs. Used for regulation as well as PG, under-voltage and over-voltage protection and monitoring.
11	ILIM1	Current Limit 1. A resistor from this pin to GND sets the current limit.
12 17	SS1 SS2	Soft Start. A capacitor from this pin to GND programs the slew rate of the converter during initialization. During initialization, this pin is charged with a 5μA current source.

Pin Definitions (Continued)

Pin Number	Pin Name	Pin Function Description
13	DDR	DDR Mode Control. High = DDR mode. Low = 2 separate regulators operating 180° out of phase.
14	VIN	Input Voltage. Normally connected to battery, provides voltage feed-forward to set the amplitude of the internal oscillator ramp. When using the IC for 2-step conversion from 5V input, connect through 100K to ground, which will set the appropriate ramp gain and synchronize the channels 90° out of phase.
15	PG1	Power Good Flag. An open-drain output that will pull LOW when VSEN is outside of a $\pm 10\%$ range of the 0.9V reference.
16	PG2 / REF2OUT	Power Good 2. When not in DDR Mode: Open-drain output that pulls LOW when the VOUT is out of regulation or in a fault condition Reference Out 2. When in DDR Mode, provides a buffered output of REF2. Typically used as the VDDQ/2 reference.
18	ILIM2 / REF2	Current Limit 2. When not in DDR Mode, A resistor from this pin to GND sets the current limit. Reference for reg #2 when in DDR Mode. Typically set to VOUT1/2.
28	VCC	VCC. This pin powers the chip as well as the LDRV buffers. The IC starts to operate when voltage on this pin exceeds 4.6V (UVLO rising) and shuts down when it drops below 4.3V (UVLO falling).

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter	Min.	Typ.	Max.	Units
VCC Supply Voltage			6.5	V
VIN			18	V
BOOT, SW, ISNS, HDRV			24	V
BOOT to SW			6.5	V
All Other Pins	-0.3		VCC+0.3	V
Junction Temperature (T_J)	-40		150	°C
Storage Temperature	-65		150	°C
Lead Soldering Temperature, 10 seconds			300	°C

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC		4.75	5	5.25	V
Supply Voltage VIN				16	V
Ambient Temperature (T_A)	note 1	-40		85	°C

Electrical Specifications

Recommended operating conditions, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
Power Supplies					
VCC Current	LDRV, HDRV Open, VSEN forced above regulation point		2.2	3.0	mA
	Shut-down (EN=0)			30	μA
VIN Current – Sinking	VIN = 15V	10		30	μA
VIN Current – Sourcing	VIN = 0V		-15	-30	μA
VIN Current – Shut-down				1	μA
UVLO Threshold	Rising VCC	4.3	4.55	4.75	V
	Falling	4.1	4.25	4.45	V
UVLO Hysteresis			300		mV
Oscillator					
Frequency		255	300	345	KHz
Ramp Amplitude, pk-pk	VIN = 16V		2		V
Ramp Amplitude, pk-pk	VIN = 5V		1.25		V
Ramp Offset			0.5		V
Ramp / VIN Gain	VIN ≥ 3V		125		mV/V
Ramp / VIN Gain	1V < VIN < 3V		250		mV/V
Reference and Soft Start					
Internal Reference Voltage		0.891	0.9	0.909	V
Soft Start Current (I _{SS})	at start-up		-5		μA
Soft Start Complete Threshold			1.5		V
PWM Converters					
Load Regulation	I _{OUTX} from 0 to 5A, VIN from 5 to 15V	-2		+2	%
VSEN Bias Current		50	80	120	nA
Under-Voltage Shutdown	as % of set point. 2μS noise filter	70	75	80	%
Over-Voltage Threshold	as % of set point. 2μS noise filter	115	120	125	%
I _{SNS} Over-Current Threshold	R _{LIM} = 68.5KΩ see Figure 10.	112	140	168	μA
Minimum Duty Cycle		10			%
Output Drivers					
HDRV Output Resistance	Sourcing		12	15	Ω
	Sinking		2.4	4	Ω
LDRV Output Resistance	Sourcing		12	15	Ω
	Sinking		1.2	2	Ω
PG (Power Good Output) and Control pins					
Lower Threshold	as % of set point, 2μS noise filter	-86		-94	%
Upper Threshold	as % of set point, 2μS noise filter	108		116	%
PG Output Low	IPG = 4mA			0.5	V
Leakage Current	V _{PULLUP} = 5V			1	μA
PG2/REF2OUT Voltage	DDR = 1, 0 mA < I _{REF2OUT} ≤ 10mA	99		1.01	% V _{REF2}
DDR, EN Inputs					
Input High		2			V
Input Low				0.8	V

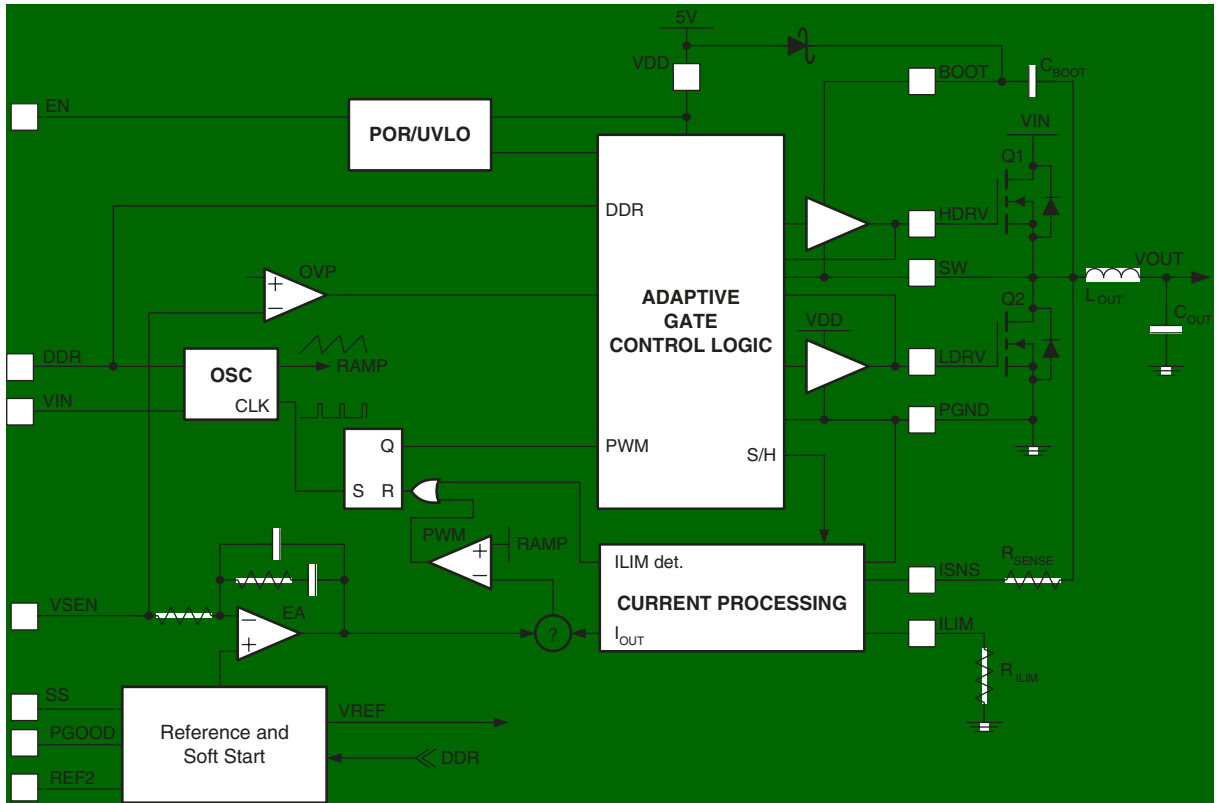


Figure 3. IC Block Diagram

Typical Applications



Figure 4. DDR Regulator Application

Table 1. DDR Regulator BOM

Description	Qty	Ref.	Vendor	Part Number
Capacitor 68μF, Tantalum, 25V, ESR 150mΩ	1	C1	AVX	TPSV686*025#0150
Capacitor 10nF, Ceramic	2	C2, C3	Any	
Capacitor 68μF, Tantalum, 6V, ESR 1.8Ω	1	C4	AVX	TAJB686*006
Capacitor 150nF, Ceramic	2	C5, C7	Any	
Capacitor 180μF, Specialty Polymer 4V, ESR 15mΩ	2	C6A, C6B	Panasonic	EEFUE0G181R
Capacitor 1000μF, Specialty Polymer 4V, ESR 10mΩ	1	C8	Kemet	T510E108(1)004AS4115
Capacitor 0.1μF, Ceramic	1	C9	Any	
1.82KΩ, 1% Resistor	3	R1, R2, R6	Any	
56.2KΩ, 1% Resistor	1	R3	Any	
10KΩ, 5% Resistor	1	R4	Any	
3.24KΩ, 1% Resistor	1	R5	Any	
1.5KΩ, 1% Resistor	2	R7, R8	Any	
Schottky Diode 30V	2	D1, D2	Fairchild	BAT54
Inductor 6.4μH, 6A, 8.64mΩ	1	L1	Panasonic	ETQ-P6F6R4HFA
Inductor 0.8μH, 6A, 2.24mΩ	1	L2	Panasonic	ETQ-P6F0R8LFA
Dual MOSFET with Schottky	2	Q1, Q2	Fairchild	FDS6986S (note 1)
DDR Controller	1	U1	Fairchild	FAN5026

Notes:

- Suitable for applications of 4A continuous, 6A peak for VDDQ. If continuous operation above 6A is required use single SO-8 packages for Q1A (FDS6612A) and Q1B (FDS6690S) respectively. Using FDS6690S, change R7 to 1200Ω. Refer to Power MOSFET Selection, page 14 for more information.
- C6 = 2 X 180μF in parallel.

Typical Applications (Continued)

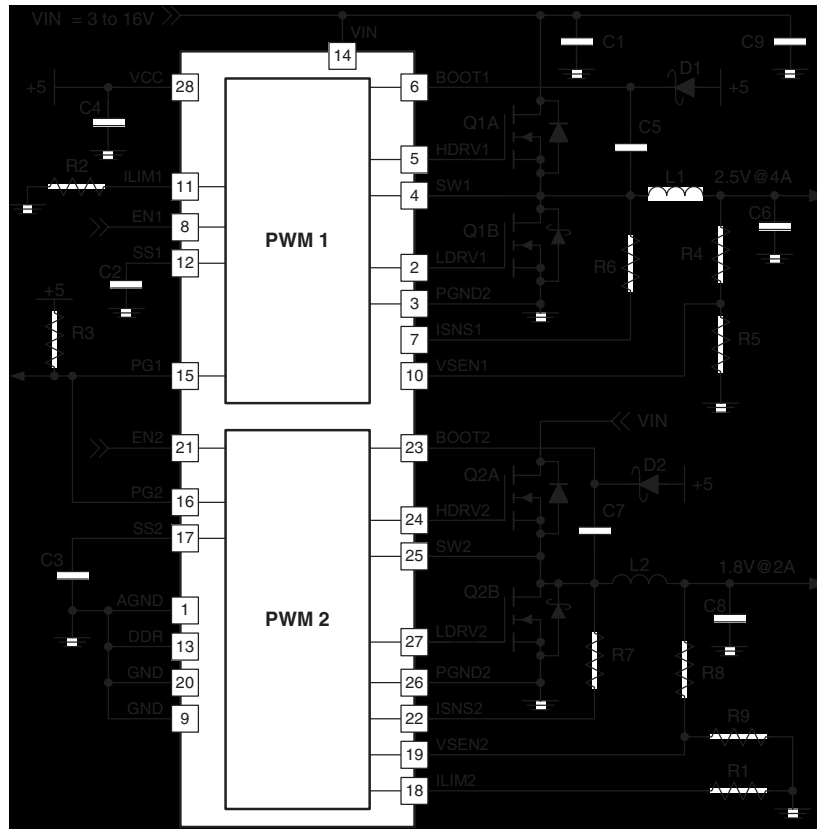


Figure 5. Dual Regulator Application

Table 2. Dual Regulator BOM

Description	Qty	Ref.	Vendor	Part Number
Capacitor 68μF, Tantalum, 25V, ESR 95mΩ	1	C1	AVX	TPSV686*025#095
Capacitor 10nF, Ceramic	2	C2, C3	Any	
Capacitor 68μF, Tantalum, 6V, ESR 1.8Ω	1	C4	AVX	TAJB686*006
Capacitor 150nF, Ceramic	2	C5, C7	Any	
Capacitor 330μF, Poscap, 4V, ESR 40mΩ	2	C6, C8	Sanyo	4TPB330ML
Capacitor 0.1μF, Ceramic	2	C9	Any	
56.2KΩ, 1% Resistor	1	R1, R2	Any	
10KΩ, 5% Resistor	1	R3	Any	
3.24KΩ, 1% Resistor	1	R4	Any	
1.82KΩ, 1% Resistor	3	R5, R8, R9	Any	
1.5KΩ, 1% Resistor	2	R6, R7	Any	
Schottky Diode 30V	2	D1, D2	Fairchild	BAT54
Inductor 6.4μH, 6A, 8.64mΩ	2	L1, L2	Panasonic	ETQ-P6F6R4HFA
Dual MOSFET with Schottky	1	Q1	Fairchild	FDS6986S (note 1)
DDR Controller	1	U1	Fairchild	FAN5026

Note:

1. If currents above 4A continuous required, use single SO-8 packages for Q1A/Q2A (FDS6612A) and Q1B/Q2B (FDS6690S) respectively. Using FDS6690S, change R6/R7 as required. Refer to Power MOSFET Selection, page 14 for more information.

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

The two synchronous buck converters can operate from either an unregulated DC source (such as a notebook battery) with voltage ranging from 5.0V to 16V, or from a regulated system rail of 3.3V to 5V. In either mode of operation the IC is biased from a +5V source. The PWM modulators use an average current mode control with input voltage feed-forward for simplified feedback loop compensation and improved line regulation. Both PWM controllers have integrated feedback loop compensation that dramatically reduces the number of external components.

The FAN5026 can be configured to operate as a complete DDR solution. When the DDR pin is set high, the second channel can provide the capability to track the output voltage of the first channel. The PWM2 converter is prevented from going into hysteretic mode if the DDR pin is set high. In DDR mode, a buffered reference voltage (buffered voltage of the REF2 pin), required by DDR memory chips, is provided by the PG2 pin.

Converter Modes and Synchronization

Table 3. Converter Modes and Synchronization

Mode	VIN	VIN Pin	DDR Pin	PWM 2 w.r.t. PWM1
DDR1	Battery	VIN	HIGH	IN PHASE
DDR2	+5V	R to GND	HIGH	+ 90°
DUAL	ANY	VIN	LOW	+ 180°

When used as a dual converter (as in Figure 5), out-of-phase operation with 180 degree phase shift reduces input current ripple.

For the “2-step” conversion (where the VTT is converted from VDDQ as in Figure 4) used in DDR mode, the duty cycle of the second converter is nominally 50% and the optimal phasing depends on VIN. The objective is to keep noise generated from the switching transition in one converter from influencing the “decision” to switch in the other converter.

When VIN is from the battery, it's typically higher than 7.5V. As shown in Figure 6, 180° operation is undesirable since the turn-on of the VDDQ converter occurs very near the decision point of the VTT converter.

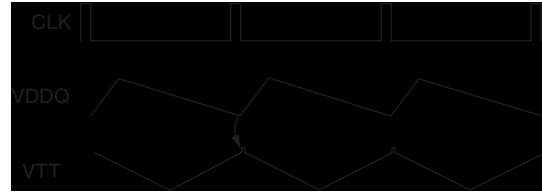


Figure 6. Noise-Susceptible 180° Phasing for DDR1

In-phase operation is optimal to reduce inter-converter interference when VIN is higher than 5V, (when VIN is from a battery), as can be seen in Figure 7. Since the duty cycle of PWM1 (generating VDDQ) is short, its switching point occurs far away from the decision point for the VTT regulator, whose duty cycle is nominally 50%.



Figure 7. Optimal In-Phase Operation for DDR1

When VIN ≈ 5V, 180° phase shifted operation can be rejected for the same reasons demonstrated Figure 6. In-phase operation with VIN ≈ 5V is even worse, since the switch point of either converter occurs near the switch point of the other converter as seen in Figure 8. In this case, as VIN is a little higher than 5V it will tend to cause early termination of the VTT pulse width. Conversely, VTT's switch point can cause early termination of the VDDQ pulse width when VIN is slightly lower than 5V.



Figure 8. Noise-Susceptible In-Phase Operation for DDR2

These problems are nicely solved by delaying the 2nd converter's clock by 90° as shown in Figure 9. In this way, all switching transitions in one converter take place far away from the decision points of the other converter.

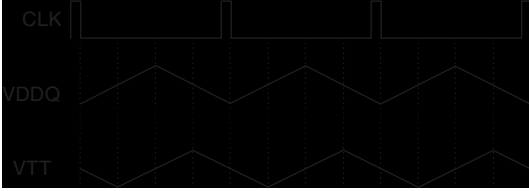


Figure 9. Optimal 90° Phasing for DDR2

Initialization and Soft Start

Assuming EN is high, FAN5026 is initialized when VCC exceeds the rising UVLO threshold. Should VCC drop below the UVLO threshold, an internal Power-On Reset function disables the chip.

The voltage at the positive input of the error amplifier is limited by the voltage at the SS pin which is charged with a 5µA current source. Once C_{SS} has charged to VREF (0.9V) the output voltage will be in regulation. The time it takes SS to reach 0.9V is:

$$T_{0.9} = \frac{0.9 \times C_{SS}}{5} \quad (1)$$

where T_{0.9} is in seconds if C_{SS} is in µF.

When SS reaches 1.5V, the Power Good outputs are enabled and hysteretic mode is allowed. The converter is forced into PWM mode during soft start.

Current Processing Section

The following discussion refers to Figure 10.

The current through R_{SENSE} resistor (I_{SNs}) is sampled shortly after Q2 is turned on. That current is held, and summed with the output of the error amplifier. This effectively creates a current mode control loop. The resistor connected to ISNSx pin (R_{SENSE}) sets the gain in the current feedback loop. For stable operation, the voltage induced by the current feedback at the PWM comparator input should be set to 30% of the ramp amplitude at maximum load current and line voltage. The following expression estimates the recommended value of R_{SENSE} as a function of the maximum load current (I_{LOAD(MAX)}) and the value of the MOSFET's R_{DS(ON)}:

$$R_{SENSE} = \frac{I_{LOAD(MAX)} \cdot R_{DS(ON)} \cdot 4.1K}{30\% \cdot 0.125 \cdot V_{IN(MAX)}} - 100 \quad (2a)$$

R_{SENSE} must, however, be kept higher than:

$$R_{SENSE(MIN)} = \frac{I_{LOAD(MAX)} \cdot R_{DS(ON)}}{150\mu A} - 100 \quad (2b)$$

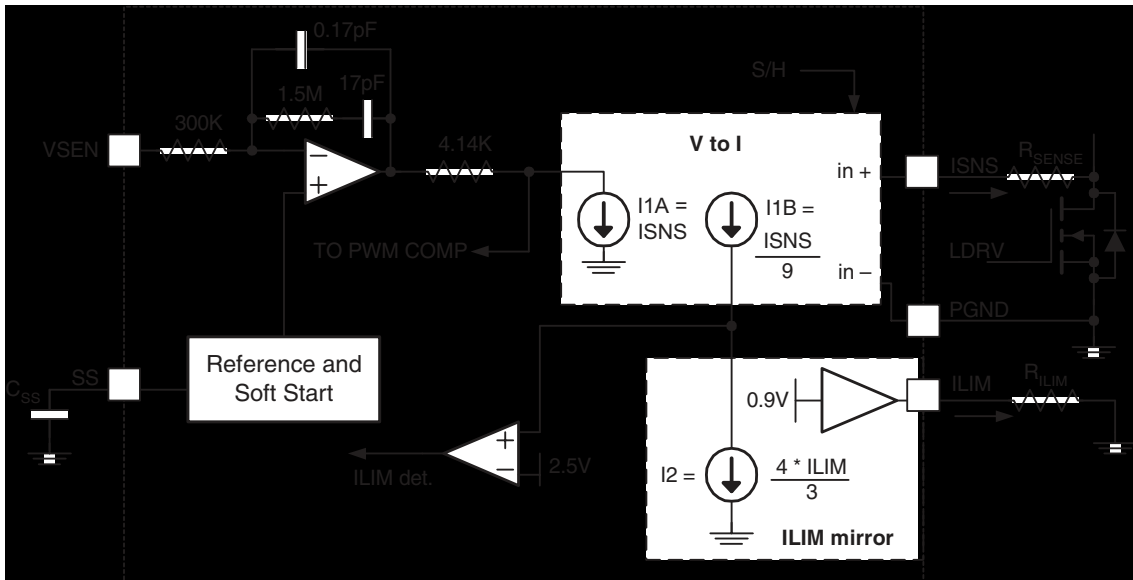


Figure 10. Current Limit / Summing Circuits

Setting the Current Limit

A ratio of ISNS is also compared to the current established when a 0.9 V internal reference drives the ILIM pin. The threshold is determined at the point when the $\frac{ISNS}{9} > \frac{ILIM \times 4}{3}$. Since

$$ISNS = \frac{I_{LOAD} \times R_{DS(ON)}}{100 + R_{SENSE}} \quad \text{therefore,}$$

$$I_{LIMIT} = \frac{0.9V}{R_{ILIM}} \times \frac{4}{3} \times \frac{9 \times (100 + R_{SENSE})}{R_{DS(ON)}} \quad (3a)$$

or

$$R_{ILIM} = \frac{10.8}{I_{LIMIT}} \times \frac{(100 + R_{SENSE})}{R_{DS(ON)}} \quad (3b)$$

Since the tolerance on the current limit is largely dependent on the ratio of the external resistors, it is fairly accurate if the voltage drop on the Switching Node side of R_{SENSE} is an accurate representation of the load current. When using the MOSFET as the sensing element, the variation of $R_{DS(ON)}$ causes proportional variation in the ISNS. This value not only varies from device to device, but also has a typical junction temperature coefficient of about 0.4%/°C (consult the MOSFET datasheet for actual values), so the actual current limit set point will decrease proportional to increasing MOSFET die temperature. A factor of 1.6 in the current limit setpoint should compensate for all MOSFET $R_{DS(ON)}$ variations, assuming the MOSFET's heat sinking will keep its operating die temperature below 125°C.

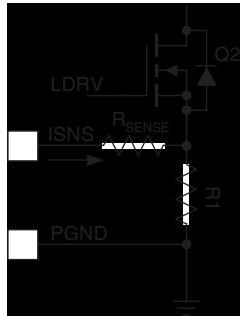


Figure 11. Improving Current Sensing Accuracy

More accurate sensing can be achieved by using a resistor (R1) instead of the $R_{DS(ON)}$ of the FET as shown in Figure 11. This approach causes higher losses, but yields greater accuracy in both V_{DROOP} and I_{LIMIT} . R1 is a low value (e.g. 10mΩ) resistor.

Current limit (I_{LIMIT}) should be set sufficiently high as to allow inductor current to rise in response to an output load transient. Typically, a factor of 1.3 is sufficient. In addition, since I_{LIMIT} is a peak current cut-off value, we will need to multiply $I_{LOAD(MAX)}$ by the inductor ripple current (we'll use 25%). For example, in Figure 5 the target for I_{LIMIT} would be:

$$I_{LIMIT} > 1.2 \times 1.25 \times 1.6 \times 6A \approx 14A \quad (4)$$

Gate Driver Section

The adaptive gate control logic translates the internal PWM control signal into the MOSFET gate drive signals providing necessary amplification, level shifting and shoot-through protection. Also, it has functions that help optimize the IC performance over a wide range of operating conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate-to-source voltages of both upper and lower MOSFETs. The lower MOSFET drive is not turned on until the gate-to-source voltage of the upper MOSFET has decreased to less than approximately 1 volt. Similarly, the upper MOSFET is not turned on until the gate-to-source voltage of the lower MOSFET has decreased to less than approximately 1 volt. This allows a wide variety of upper and lower MOSFETs to be used without a concern for simultaneous conduction, or shoot-through.

There must be a low-resistance, low-inductance path between the driver pin and the MOSFET gate for the adaptive dead-time circuit to work properly. Any delay along that path will subtract from the delay generated by the adaptive dead-time circuit and shoot-through may occur.

Frequency Loop Compensation

Due to the implemented current mode control, the modulator has a single pole response with -1 slope at frequency determined by load

$$F_{PO} = \frac{1}{2\pi R_O C_O} \quad (5)$$

where R_O is load resistance and C_O is load capacitance. For this type of modulator, Type 2 compensation circuit is usually sufficient. To reduce the number of external components and simplify the design task, the PWM controller has an internally compensated error amplifier. Figure 12 shows a Type 2 amplifier and its response along with the responses of a current mode modulator and of the converter. The Type 2 amplifier, in addition to the pole at the origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole.

$$F_Z = \frac{1}{2\pi R_2 C_1} = 6kHz \quad (6a)$$

$$F_P = \frac{1}{2\pi R_2 C_2} = 600kHz \quad (6b)$$

This region is also associated with phase 'bump' or reduced phase shift. The amount of phase shift reduction depends the width of the region of flat gain and has a maximum value of 90 degrees. To further simplify the converter compensation, the modulator gain is kept independent of the input voltage variation by providing feed-forward of V_{IN} to the oscillator ramp.

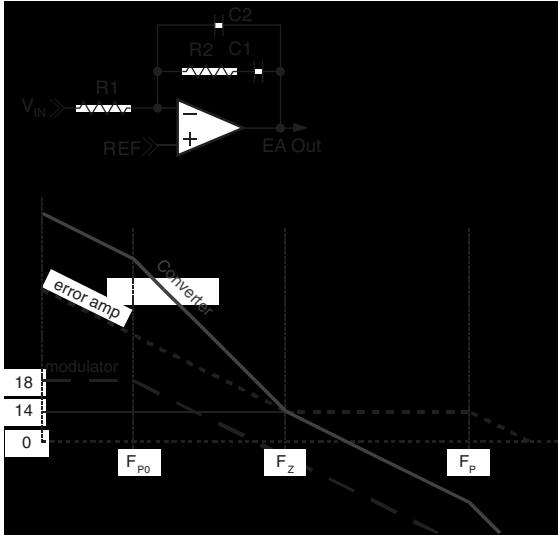


Figure 12. Compensation

The zero frequency, the amplifier high frequency gain and the modulator gain are chosen to satisfy most typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation plenty of phase margin is easily achieved due to zero-pole pair phase ‘boost’.

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 10kHz...50kHz range gives some additional phase ‘boost’. Fortunately, there is an opposite trend in mobile applications to keep the output capacitor as small as possible.

If a larger inductor value or low ESR values are called for by the application, additional phase margin can be achieved by putting a zero at the LC crossover frequency. This can be achieved with a capacitor across the feedback resistor (e.g. R5 from Figure 5) as shown below.

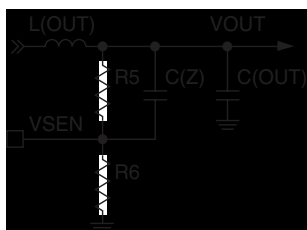


Figure 13. Improving Phase Margin

The optimal value of C(Z) is:

$$C(Z) = \frac{\sqrt{L(OUT) \times C(OUT)}}{R5} \tag{7}$$

Protection

The converter output is monitored and protected against extreme overload, short circuit, over-voltage and under-voltage conditions.

A sustained overload on an output sets the PGx pin low and latches-off the whole chip. Operation can be restored by cycling the VCC voltage or by toggling the EN pin.

If VOUT drops below the under-voltage threshold, the chip shuts down immediately.

Over-Current Sensing

If the circuit’s current limit signal (“ILIM det” as shown in Figure 10) is high at the beginning of a clock cycle, a pulse-skipping circuit is activated and HDRV is inhibited. The circuit continues to pulse skip in this manner for the next 8 clock cycles. If at any time from the 9th to the 16th clock cycle, the “ILIM det” is again reached, the over-current protection latch is set, disabling the chip. If “ILIM det” does not occur between cycle 9 and 16, normal operation is restored and the over-current circuit resets itself.



Figure 14. Over-Current Protection Waveforms

Over-Voltage / Under-Voltage Protection

Should the VSNS voltage exceed 120% of VREF (0.9V) due to an upper MOSFET failure, or for other reasons, the overvoltage protection comparator will force LDRV high. This action actively pulls down the output voltage and, in the event of the upper MOSFET failure, will eventually blow the battery fuse. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

This OVP scheme provides a ‘soft’ crowbar function which helps to tackle severe load transients and does not invert the output voltage when activated — a common problem for latched OVP schemes.

Similarly, if an output short-circuit or severe load transient causes the output to droop to less than 75% of its regulation set point. Should this condition occur, the regulator will shut down.

Over-Temperature Protection

The chip incorporates an over temperature protection circuit that shuts the chip down when a die temperature of about 150°C is reached. Normal operation is restored at die temperature below 125°C with internal Power On Reset asserted, resulting in a full soft-start cycle.

Design and Component Selection Guidelines

As an initial step, define operating input voltage range, output voltage, minimum and maximum load currents for the controller.

Setting the Output Voltage

The internal reference is 0.9V. The output is divided down by a voltage divider to the VSEN pin (for example, R5 and R6 in Figure 4). The output voltage therefore is:

$$\frac{0.9V}{R6} = \frac{V_{OUT} - 0.9V}{R5} \quad (8a)$$

To minimize noise pickup on this node, keep the resistor to GND (R6) below 2K. We selected R6 at 1.82K. Then choose R5:

$$R5 = \frac{(1.82K) \times (V_{OUT} - 0.9)}{0.9} = 3.24K \quad (8b)$$

For DDR applications converting from 3.3V to 2.5V, or other applications requiring high duty cycles, the duty cycle clamp must be disabled by tying the converter's FPWM to GND. When converter's FPWM is GND, the converter's maximum duty cycle will be greater than 90%. When using as a DDR converter with 3.3V input, set up the converter for In-Phase synchronization by tying the VIN pin to +5V.

Output Inductor Selection

The minimum practical output inductor value is the one that keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the minimum current somewhere from 15% to 35% of the nominal current. At light load, the controller can automatically switch to hysteretic mode of operation to sustain high efficiency. The following equations help to choose the proper value of the output filter inductor.

$$\Delta I = 2 \times I_{MIN} = \frac{\Delta V_{OUT}}{ESR} \quad (9)$$

where ΔI is the inductor ripple current and ΔV_{OUT} is the maximum ripple allowed.

$$L = \frac{V_{IN} - V_{OUT}}{F_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \quad (10)$$

for this example we'll use:

$$\begin{aligned} V_{IN} &= 12V, V_{OUT} = 2.5V \\ \Delta I &= 25\% \times 6A = 1.5A \\ F_{SW} &= 300KHz. \end{aligned}$$

therefore
 $L \approx 4.4\mu H$

Output Capacitor Selection

The output capacitor serves two major functions in a switching power supply. Along with the inductor it filters the sequence of pulses produced by the switcher, and it supplies the load transient currents. The output capacitor requirements are usually dictated by ESR, Inductor ripple current (ΔI) and the allowable ripple voltage (ΔV).

$$ESR < \frac{\Delta V}{\Delta I} \quad (11)$$

In addition, the capacitor's ESR must be low enough to allow the converter to stay in regulation during a load step. The ripple voltage due to ESR for the converter in Figure 5 is 120mV P-P. Some additional ripple will appear due to the capacitance value itself:

$$\Delta V = \frac{\Delta I}{C_{OUT} \times 8 \times F_{SW}} \quad (12)$$

which is only about 1.5mV for the converter in Figure 5 and can be ignored.

The capacitor must also be rated to withstand the RMS current which is approximately 0.3 X (ΔI), or about 400mA for the converter in Figure 5. High frequency decoupling capacitors should be placed as close to the loads as physically possible.

Input Capacitor Selection

The input capacitor should be selected by its ripple current rating.

Two-Stage Converter Case

In DDR mode (Figure 4), the VTT power input is powered by the VDDQ output, therefore all of the input capacitor ripple current is produced by the VDDQ converter. A conservative estimate of the output current required for the 2.5V regulator is:

$$I_{REG1} = I_{VDDQ} + \frac{I_{VTT}}{2}$$

As an example, if average I_{VDDQ} is 3A, and average I_{VTT} is 1A, I_{VDDQ} current will be about 3.5A. If average input voltage is 12V, RMS input ripple current will be:

$$I_{RMS} = I_{OUT(MAX)} \sqrt{D - D^2} \quad (13)$$

where D is the duty cycle of the PWM1 converter:

$$D < \frac{V_{OUT}}{V_{IN}} = \frac{2.5}{12} \quad (14)$$

therefore:

$$I_{RMS} = 3.5 \sqrt{\frac{2.5}{12} - \left(\frac{2.5}{12}\right)^2} = 1.42A \quad (15)$$

Dual Converter 180° Phased

In Dual mode (Figure 5), both converters contribute to the capacitor input ripple current. With each converter operating 180° out of phase, the RMS currents add in the following fashion:

$$I_{RMS} = \sqrt{I_{RMS(1)}^2 + I_{RMS(2)}^2} \text{ or} \quad (16a)$$

$$I_{RMS} = \sqrt{(I_1)^2(D_1 - D_1^2) + (I_2)^2(D_2 - D_2^2)} \quad (16b)$$

which for the dual 3A converters of Figure 5, calculates to:

$$I_{RMS} = 1.51A$$

Power MOSFET Selection

Losses in a MOSFET are the sum of its switching (P_{SW}) and conduction (P_{COND}) losses.

In typical applications, the FAN5026 converter's output voltage is low with respect to its input voltage, therefore the Lower MOSFET (Q2) is conducting the full load current for most of the cycle. Q2 should therefore be selected to minimize conduction losses, thereby selecting a MOSFET with low $R_{DS(ON)}$.

In contrast, the high-side MOSFET (Q1) has a much shorter duty cycle, and its conduction loss will therefore have less of an impact. Q1, however, sees most of the switching losses, so Q1's primary selection criteria should be gate charge.

High-Side Losses

Figure shows a MOSFET's switching interval, with the upper graph being the voltage and current on the Drain to Source and the lower graph detailing V_{GS} vs. time with a constant current charging the gate. The x-axis there-

fore is also representative of gate charge (Q_G). $C_{ISS} = C_{GD} + C_{GS}$, and it controls t_1 , t_2 , and t_4 timing. C_{GD} receives the current from the gate driver during t_3 (as V_{DS} is falling). The gate charge (Q_G) parameters on the lower graph are either specified or can be derived from MOSFET datasheets.

Assuming switching losses are about the same for both the rising edge and falling edge, Q1's switching losses, occur during the shaded time when the MOSFET has voltage across it and current through it.

These losses are given by:

$$P_{UPPER} = P_{SW} + P_{COND}$$

$$P_{SW} = \left(\frac{V_{DS} \times I_L}{2} \times 2 \times t_S \right) F_{SW} \quad (17a)$$

$$P_{COND} = \left(\frac{V_{OUT}}{V_{IN}} \right) \times I_{OUT}^2 \times R_{DS(ON)} \quad (17b)$$

where:

P_{UPPER} is the upper MOSFET's total losses, and P_{SW} and P_{COND} are the switching and conduction losses for a given MOSFET. $R_{DS(ON)}$ is at the maximum junction temperature (T_J). t_S is the switching period (rise or fall time) and is t_2+t_3 Figure .

The driver's impedance and C_{ISS} determine t_2 while t_3 's period is controlled by the driver's impedance and Q_{GD} . Since most of t_S occurs when $V_{GS} = V_{SP}$ we can use a constant current assumption for the driver to simplify the calculation of t_S :

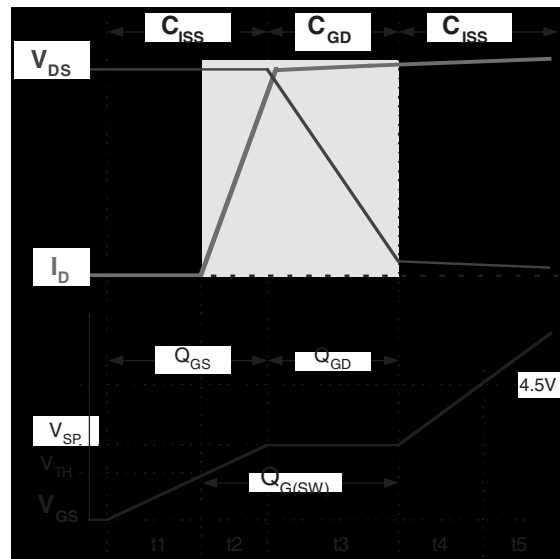


Figure 15. Switching Losses and Q_G

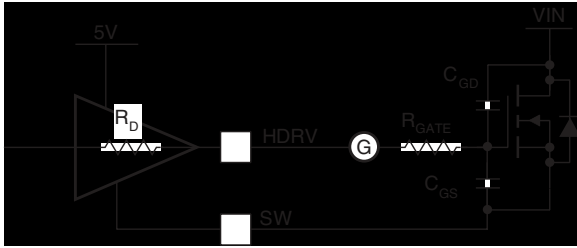


Figure 16. Drive Equivalent Circuit

$$t_s = \frac{Q_{G(SW)}}{I_{DRIVER}} \approx \frac{Q_{G(SW)}}{\left(\frac{V_{CC} - V_{SP}}{R_{DRIVER} + R_{GATE}} \right)} \quad (18)$$

Most MOSFET vendors specify Q_{GD} and Q_{GS} . $Q_{G(SW)}$ can be determined as: $Q_{G(SW)} = Q_{GD} + Q_{GS} - Q_{TH}$ where Q_{TH} is the gate charge required to get the MOSFET to its threshold (V_{TH}). For the high-side MOSFET, $V_{DS} = V_{IN}$, which can be as high as 20V in a typical portable application. Care should also be taken to include the delivery of the MOSFET's gate power (P_{GATE}) in calculating the power dissipation required for the FAN5026:

$$P_{GATE} = Q_G \times V_{CC} \times F_{SW} \quad (19)$$

where Q_G is the total gate charge to reach V_{CC} .

Low-Side Losses

Q2, however, switches on or off with its parallel shottky diode conducting, therefore $V_{DS} \approx 0.5V$. Since P_{SW} is proportional to V_{DS} , Q2's switching losses are negligible and we can select Q2 based on $R_{DS(ON)}$ only.

Conduction losses for Q2 are given by:

$$P_{COND} = (1 - D) \times I_{OUT}^2 \times R_{DS(ON)} \quad (20)$$

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the highest operating junction temperature and

$$D = \frac{V_{OUT}}{V_{IN}}$$

is the minimum duty cycle for the converter.

Since $D_{MIN} < 20\%$ for portable computers, $(1-D) \approx 1$ produces a conservative result, further simplifying the calculation.

The maximum power dissipation ($P_{D(MAX)}$) is a function of the maximum allowable die temperature of the low-side MOSFET, the θ_{J-A} , and the maximum allowable ambient temperature rise:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{J-A}} \quad (21)$$

θ_{J-A} , depends primarily on the amount of PCB area that can be devoted to heat sinking (see FSC app note AN-1029 for SO-8 MOSFET thermal information).

Layout Considerations

Switching converters, even during normal operation, produce short pulses of current which could cause substantial ringing and be a source of EMI if layout constraints are not observed.

There are two sets of critical components in a DC-DC converter. The switching power components process large amounts of energy at high rate and are noise generators. The low power components responsible for bias and feedback functions are sensitive to noise.

A multi-layer printed circuit board is recommended. Dedicate one solid layer for a ground plane. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels.

Notice all the nodes that are subjected to high dV/dt voltage swing such as SW, HDRV and LDRV, for example. All surrounding circuitry will tend to couple the signals from these nodes through stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces. It is not recommended to use High Density Interconnect Systems, or micro-vias on these signals. The use of High Density Interconnect Systems or micro-vias on these signals is not recommended. The use of normal thermal vias is left to the discretion of the designer.

Keep the wiring traces from the IC to the MOSFET gate and source as short as possible and capable of handling peak currents of 2A. Minimize the area within the gate-source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components like the soft-start capacitor and current sense resistors as close as possible to the respective pins of the IC.

The FAN5026 utilizes advanced packaging technologies with lead pitches of 0.6mm. High performance analog semiconductors utilizing narrow lead spacing may require special considerations in PWB design and manufacturing. It is critical to maintain proper cleanliness of the area surrounding these devices. It is not recommended to use any type of rosin or acid core solder, or the use of flux in either the manufacturing or touch up process as these may contribute to corrosion or enable electromigration and/or eddy currents near the sensitive low current signals. When chemicals such as these are used on or near the PWB, it is suggested that the entire PWB be cleaned and dried completely before applying power.

Mechanical Dimensions

28-Pin TSSOP

