HV5622

32-Channel Serial-to-Parallel Converter With Open Drain Outputs

Features

- 100 mA Minimum Sink Current
- 8 MHz Shift Register Speed
- Polarity and Blanking Inputs
- CMOS-compatible Inputs
- Forward and Reverse Shifting Options
- Diode to V_{PP} allows Efficient Power Recovery

Applications

- Inkjet and Electrostatic Print Heads
- AC-electroluminescent Displays
- Microelectromechanical Systems Applications

General Description

The HV5622 is a low-voltage serial-to-high-voltage parallel converter with open drain outputs. This device has been designed as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple-output high-voltage current-sinking capabilities such as driving inkjet and electrostatic print heads, plasma panels, vacuum fluorescent and large matrix LCD displays.

The device consists of a 32-bit Shift register, 32 latches and control logic to perform the polarity select and blanking of the outputs. Data is shifted through the Shift register on the high-to-low transition of the clock. The HV5622 shifts in a clockwise direction when viewed from the top of the package. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the Shift register. The operation of the Shift register is not affected by the latch enable ($\overline{LE}$), blanking ($\overline{BL}$) and polarity ($\overline{POL}$) inputs. Transfer of data from the Shift register to the latch occurs when the $\overline{LE}$ input is high. The data in the latch is stored when $\overline{LE}$ is low.

Package Types

44-lead PQFP (Top view)
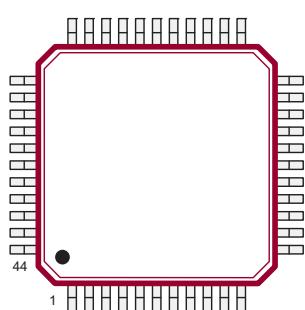
44-lead PLCC (Top view)
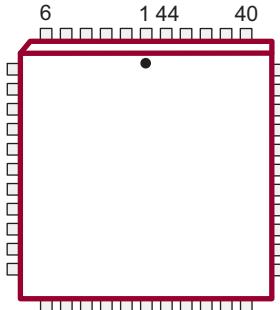
See Table 2-1 and Table 2-2 for pin information.

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Functional Block Diagram

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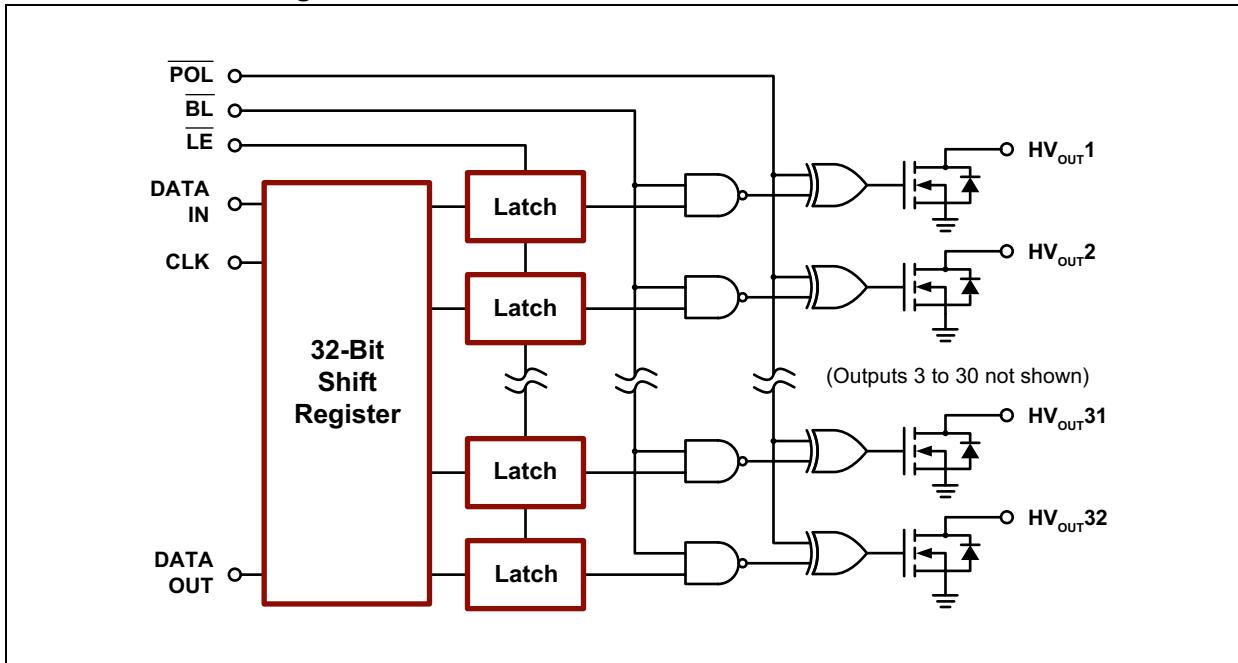
Typical Application Circuit
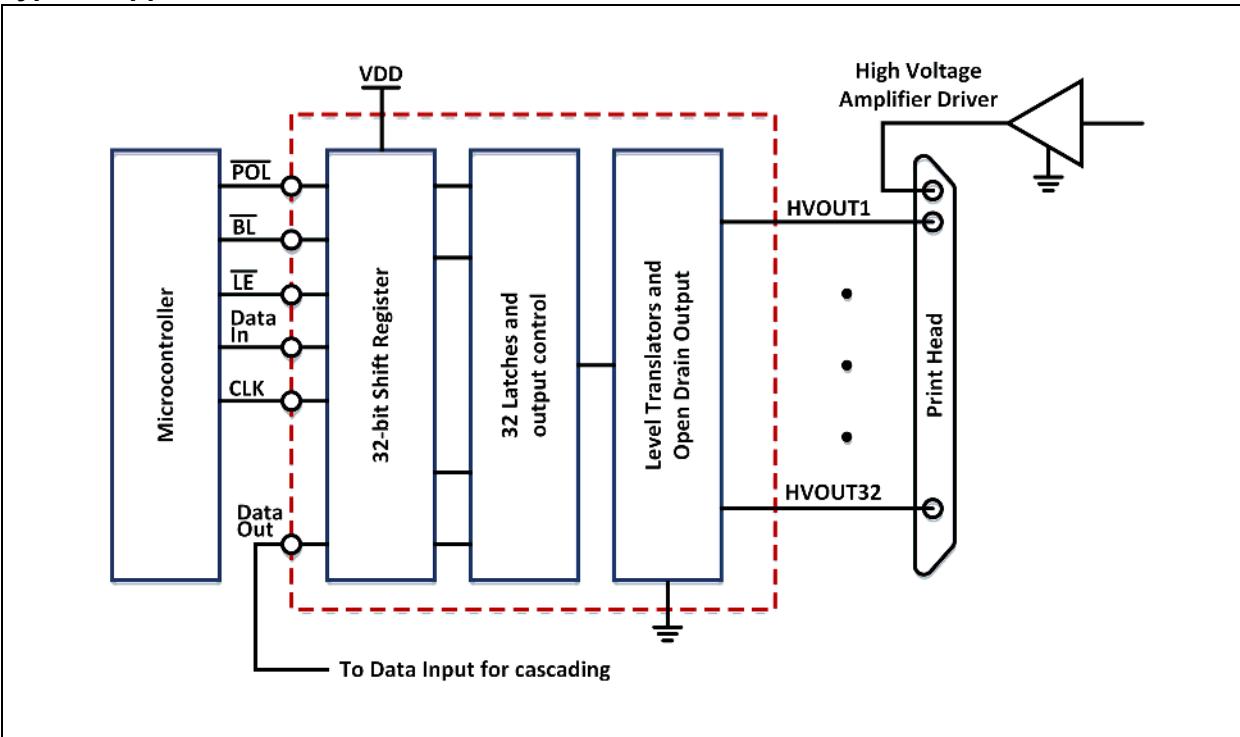
HV5622

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage, V_{DD} (**Note 1**) .... –0.5V to +15V
Output Voltage, V_{PP} (**Note 1**) .... –0.5V to +230V
Logic Input Levels (**Note 1**) .... –0.5V to V_{DD}+0.5V
Ground Current (**Note 2**) 1.5A
Operating Ambient Temperature, T_A .... –40°C to +85°C
Storage Temperature, T_S .... –65°C to +150°C
Continuous Total Power Dissipation:
    44-lead PQFP (**Note 3**) .... 1200 mW
    44-lead PLCC (**Note 3**) .... 1200 mW

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† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: All voltages are referenced to V_{SS}.
    2: Duty cycle is limited by the total power dissipated in the package.
    3: For operations above 25°C ambient, derate linearly to the maximum operating temperature at 20 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Logic Supply Voltage	V_{DD}	10.8	—	13.2	V	
High-voltage Output Voltage	HV_{OUT}	–0.3	—	+220	V	
High-level Input Voltage	V_{IH}	V_{DD}–2	—	V_{DD}	V	
Low-level Input Voltage	V_{IL}	0	—	2	V	
Clock Frequency	f_{CLK}	—	—	8	MHz	
Operating Ambient Temperature	T_A	–40	—	+85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over recommended operating conditions unless otherwise stated

Parameter		Sym.	Min.	Typ.	Max.	Unit	Conditions
V_{DD} Supply Current		I_{DD}	—	—	15	mA	f_{CLK} = 8 MHz, f_{DATA} = 4 MHz
Quiescent V_{DD} Supply Current		I_{DDQ}	—	—	100	µA	V_{IN} = 0V
Off State Output Current		$I_{O(OFF)}$	—	—	10	µA	All outputs high, all SWS parallel
High-level Logic Input Current		I_{IH}	—	—	1	µA	V_{IH} = V_{DD}
Low-level Logic Input Current		I_{IL}	—	—	–1	µA	V_{IL} = 0V
High-level Output Data Out		V_{OH}	V_{DD}–1V	—	—	V	I_{DOUT} = –100 µA
Low-level Output Voltage	HV_{OUT}	V_{OL}	—	—	15	V	I_{HVOUT} = 100 mA
	Data Out		—	—	1	V	I_{DOUT} = 100 µA
HV_{OUT} Clamp Voltage		V_{OC}	—	—	–1.5	V	I_{OL} = –100 mA

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: V_{DD} = 12V, T_A = 25°C

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	f_{CLK}	—	—	8	MHz	
Clock Width, High or Low	t_{WL}, t_{WH}	62	—	—	ns	
Data Set-up Time before CLK Falls	t_{SU}	25	—	—	ns	
Data Hold Time after CLK Falls	t_H	10	—	—	ns	
Turn-on Time, HV_{OUT} from Enable	t_{ON}	—	—	500	ns	R_L = 2 kΩ to V_{PP} maximum
Delay Time Clock to Data High to Low	t_{DHL}	—	—	100	ns	C_L = 15 pF
Delay Time Clock to Data Low to High	t_{DLH}	—	—	100	ns	C_L = 15 pF
Delay Time Clock to Latch Enable Low to High	t_{DLE}	50	—	—	ns	
Latch Enable Pulse Width	t_{WLE}	50	—	—	ns	
Latch Enable Setup Time before Clock Falls	t_{SLE}	50	—	—	ns	

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–40	—	+85	°C	
Storage Temperature	T_S	–65	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
44-lead PQFP	θ_{JA}	—	51	—	°C/W	
44-lead PLCC	θ_{JA}	—	37	—	°C/W	

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Timing Waveforms
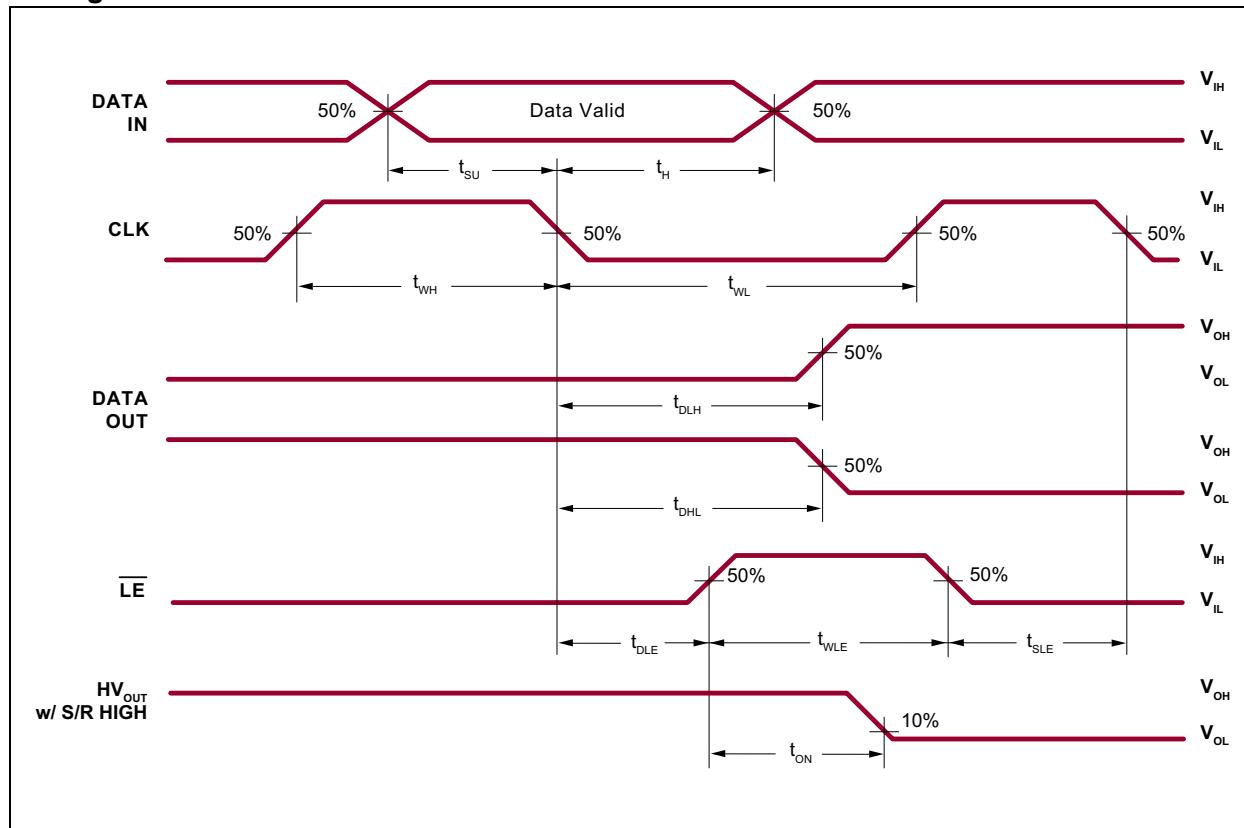
2.0   PIN DESCRIPTION

The details on the pins of HV5622 44-lead PQFP and
44-lead PLCC are in Table 2-1 and Table 2-2,
respectively. Refer to **Package Types** for the location
of pins.

TABLE 2-1:   44-LEAD PQFP PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT22	High-voltage output
2	HVOUT21	High-voltage output
3	HVOUT20	High-voltage output
4	HVOUT19	High-voltage output
5	HVOUT18	High-voltage output
6	HVOUT17	High-voltage output
7	HVOUT16	High-voltage output
8	HVOUT15	High-voltage output
9	HVOUT14	High-voltage output
10	HVOUT13	High-voltage output
11	HVOUT12	High-voltage output
12	HVOUT11	High-voltage output
13	HVOUT10	High-voltage output
14	HVOUT9	High-voltage output
15	HVOUT8	High-voltage output
16	HVOUT7	High-voltage output
17	HVOUT6	High-voltage output
18	HVOUT5	High-voltage output
19	HVOUT4	High-voltage output
20	HVOUT3	High-voltage output
21	HVOUT2	High-voltage output
22	HVOUT1	High-voltage output
23	DATA OUT	Data output pin
24	NC	No connection
25	NC	No connection
26	NC	No connection
27	$\overline{POL}$	Inverts the polarity of the HVOUT pins
28	CLK	Clock pin. Shift registers shift data on the falling edge of the input clock.
29	VSS	Reference voltage (usually ground)
30	VDD	Logic supply voltage
31	$\overline{LE}$	Latch enable pin. Data is shifted from the Shift register to the latches on logic input high.
32	DATA IN	Data input pin
33	$\overline{BL}$	This blanking pin sets all HVOUT pins low or high depending upon the state of polarity. See Table 3-2.
34	NC	No connection

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TABLE 2-1: 44-LEAD PQFP PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
35	HVOUT32	High-voltage output
36	HVOUT31	High-voltage output
37	HVOUT30	High-voltage output
38	HVOUT29	High-voltage output
39	HVOUT28	High-voltage output
40	HVOUT27	High-voltage output
41	HVOUT26	High-voltage output
42	HVOUT25	High-voltage output
43	HVOUT24	High-voltage output
44	HVOUT23	High-voltage output

TABLE 2-2: 44-LEAD PLCC PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	HVOUT17	High-voltage output
2	HVOUT16	High-voltage output
3	HVOUT15	High-voltage output
4	HVOUT14	High-voltage output
5	HVOUT13	High-voltage output
6	HVOUT12	High-voltage output
7	HVOUT11	High-voltage output
8	HVOUT10	High-voltage output
9	HVOUT9	High-voltage output
10	HVOUT8	High-voltage output
11	HVOUT7	High-voltage output
12	HVOUT6	High-voltage output
13	HVOUT5	High-voltage output
14	HVOUT4	High-voltage output
15	HVOUT3	High-voltage output
16	HVOUT2	High-voltage output
17	HVOUT1	High-voltage output
18	DATA OUT	Data output pin
19	NC	No connection
20	NC	No connection
21	NC	No connection
22	$\overline{POL}$	Inverts the polarity of the HVOUT pins
23	CLK	Clock pin. Shift registers shift data on the falling edge of the input clock.
24	VSS	Reference voltage (usually ground)
25	VDD	Logic supply voltage
26	$\overline{LE}$	Latch enable pin. Data is shifted from the Shift register to the latches on logic input high.

TABLE 2-2:   44-LEAD PLCC PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Description
27	DATA IN	Data input pin
28	$\overline{BL}$	This blanking pin sets all HVOUT pins low or high depending upon the state of polarity. See Table 3-2.
29	NC	No internal connection
30	HVOUT32	High-voltage output
31	HVOUT31	High-voltage output
32	HVOUT30	High-voltage output
33	HVOUT29	High-voltage output
34	HVOUT28	High-voltage output
35	HVOUT27	High-voltage output
36	HVOUT26	High-voltage output
37	HVOUT25	High-voltage output
38	HVOUT24	High-voltage output
39	HVOUT23	High-voltage output
40	HVOUT22	High-voltage output
41	HVOUT21	High-voltage output
42	HVOUT20	High-voltage output
43	HVOUT19	High-voltage output
44	HVOUT18	High-voltage output

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3.0   FUNCTIONAL DESCRIPTION

Follow the steps in Table 3-1 to power up and power down the HV5622.

TABLE 3-1:   POWER-UP AND POWER-DOWN SEQUENCE

Power-up		Power-down	
Step	Description	Step	Description
1	Connect ground.	1	Remove all inputs.
2	Apply V_{DD}.	2	Remove V_{DD}.
3	Set all inputs to a known state.	3	Disconnect ground.

TABLE 3-2:   TRUTH FUNCTION TABLE

Function	Inputs					Outputs								Data Out
						Shift Register				High-voltage Output				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	1	2	...	32	1	2	...	32	
All On	X	X	X	L	L	p1	p2	...	p32	On	On	...	On	d
All Off	X	X	X	L	H	p1	p2	...	p32	Off	Off	...	Off	d
Invert Mode	X	X	L	H	L	p1	p2	...	p32	$\overline{p1}$	$\overline{p2}$	...	$\overline{p32}$	d
Load S/R	H or L	↓	L	H	H	H or L	p1	...	p31	p1	p2	...	p32	p32
Load Latches	X	H or L	↑	H	H	p1	p2	...	p32	p1	p2	...	p32	d
	X	H or L	↑	H	L	p1	p2	...	p32	$\overline{p1}$	$\overline{p2}$	...	$\overline{p32}$	d
Transparent Latch Mode	L	↓	H	H	H	L	p1	...	p31	Off	p1	...	p31	p32
	H	↓	H	H	H	H	p1	...	p31	On	p1	...	p31	p32

Note: H = High-logic level
L = Low-logic level
X = Irrelevant
↓ = High-to-low transition
↑ = Low-to-high transition
d = Current state of the data output
pn = "p" represents the current state of the Shift register output, and
"n" represents the channel order.
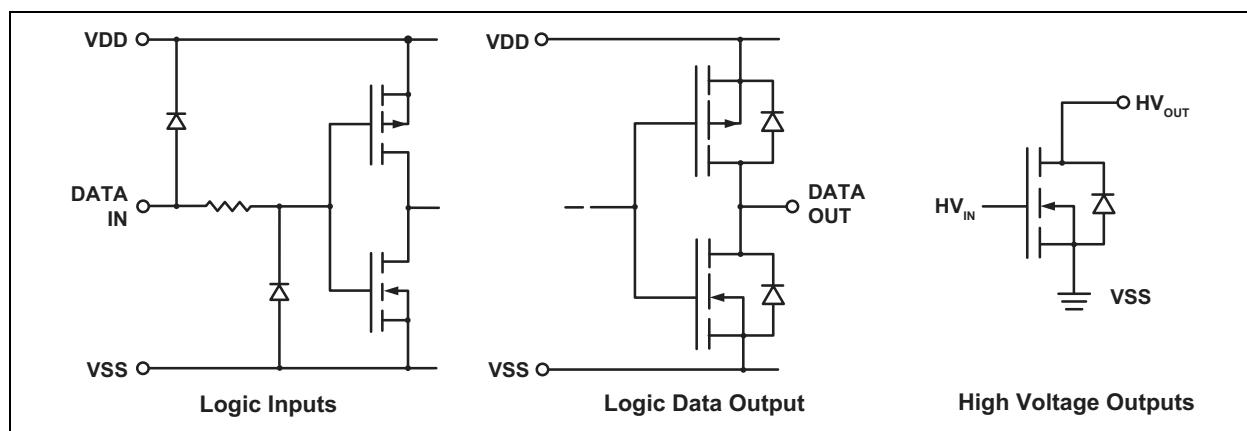
FIGURE 3-1:   *Input and Output Equivalent Circuits.*

4.0 PACKAGE MARKING INFORMATION

4.1 Packaging Information

44-lead PQFP

XXXXXXXXX
ⓔ3YYWWNNN

Example

HV5622PG
ⓔ31724198

44-lead PLCC

XXXXXXXXXXX
ⓔ3 YYWWNNN

Example

HV5622PJ
ⓔ31722741
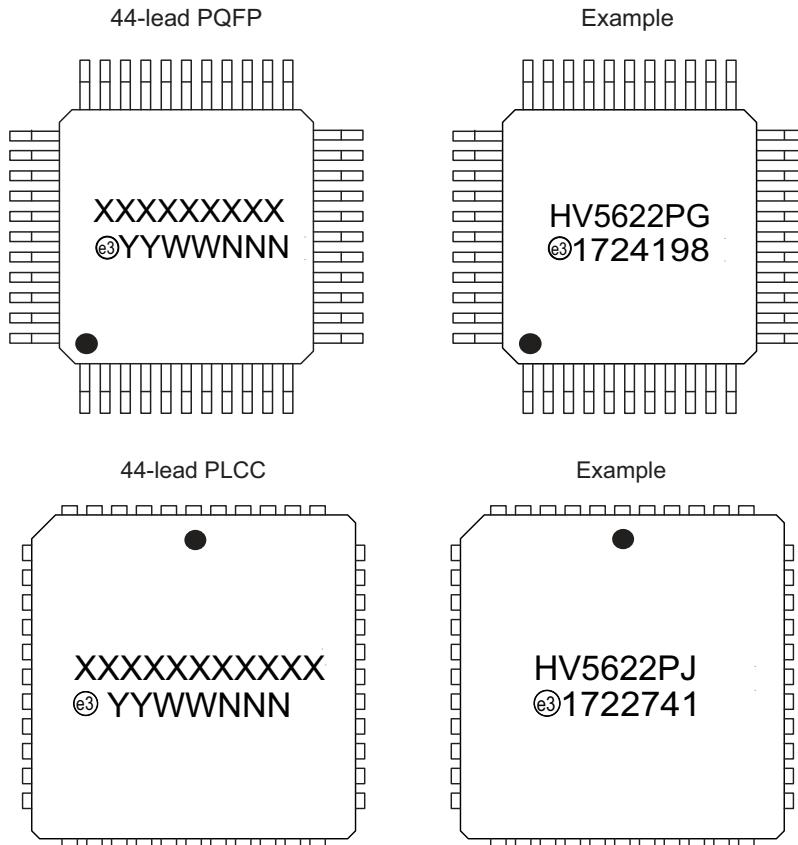
Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	ⓔ3	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

44-Lead PQFP Package Outline (PG)
10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch
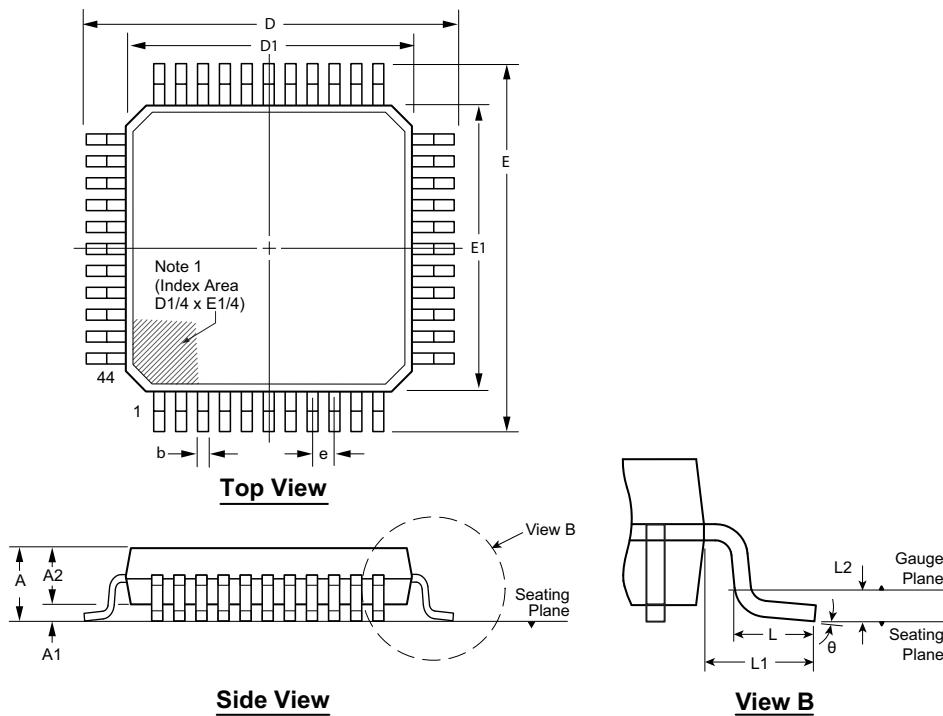
Top View

Side View

View B

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.95*	0.00	1.95	0.30	13.65*	9.80*	13.65*	9.80*	0.80 BSC	0.73	1.95 REF	0.25 BSC	0°
	NOM	-	-	2.00	-	13.90	10.00	13.90	10.00		0.88			3.5°
	MAX	2.35	0.25	2.10	0.45	14.15*	10.20*	14.15*	10.20*		1.03			7°

JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.
* This dimension is not specified in the JEDEC drawing.
Drawings not to scale.

44-Lead PLCC Package Outline (PJ)
.653x.653in body, .180in height (max), .050in pitch
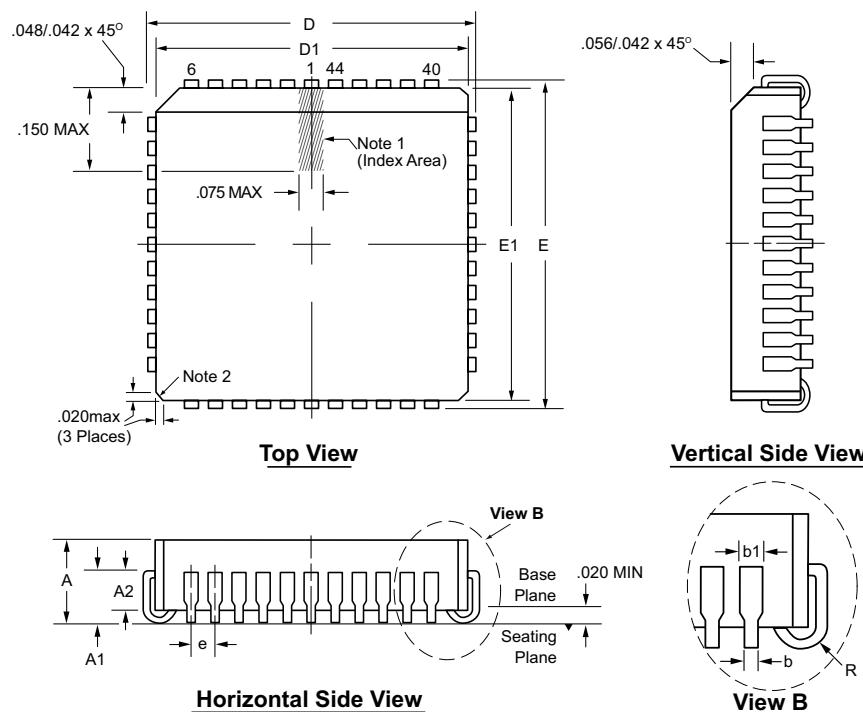
Top View

Vertical Side View

Horizontal Side View

View B

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e	R
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036†	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2017)

- Converted Supertex Doc # DSFP-HV5622 to Microchip DS20005854A
- Removed "Processed with HVCMOS$^{®}$ Technology" in the Features section
- Changed the package marking format
- Removed the 44-lead PQFP PG M919 and 44-lead PLCC PJ M903 media types
- Made minor changes throughout the document

HV5622

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device: HV5622 = 32-Channel Serial-to-Parallel Converter with Open Drain Outputs

Packages: PG = 44-lead PQFP
PJ = 44-lead PLCC

Environmental: G = Lead (Pb)-free/RoHS-compliant Package

Media Types: (blank) = 96/Tray for a PG Package
(blank) = 27/Tube for a PJ Package

Examples:

a) HV5622PG-G: 32-Channel Serial-to-Parallel Converter with Open Drain Outputs, 44-lead PQFP, 96/Tray

b) HV5622PJ-G: 32-Channel Serial-to-Parallel Converter with Open Drain Outputs, 44-lead PLCC, 27/Tube

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QUALITY MANAGEMENT SYSTEM

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Fax: 82-53-744-4302

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Fax: 82-2-558-5932 or
82-2-558-5934

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Fax: 886-3-5770-955

Taiwan - Kaohsiung
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Tel: 886-2-2508-8600
Fax: 886-2-2508-0102

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