Video / Audio Interfaces for TV and DVD Recorders

NTSC-PAL Audio I/O Interface for Recording

BD3823FV

●Description

BD3823FV is a low-noise (3.2μVrms), low distortion (0.0015%), 5ch selector, incorporating a resistor-ladder type volume.

Because of a wide power supply voltage range (7V to 14.5V), BD3823FV can meet a wide input voltage (to 4.5 Vms), and high S/N can be achieved. In addition, the built-in volume does not add any distortion ratio characteristics, even when the attenution is varied, and is applicable for high-quality audio systems.

●Features

1) A resistor-ladder type volume circuit is with a low distortion ratio (0.0015% with volume set to –6dB) and low noise (3.2 μVrms with volume set to -6dB).
2) By grouping sound input terminals with output terminals, the PCB layout is reduced.
3) Small package SSOP - B20 achieves good crosstalk characteristicss (-110 dB).
4) The use of Bi-CMOS process enables low current consumption and energy saving design.
Because of low current consumption, BD3823FV has the advantage in quality over the scaling down of the internal regulators and heat controls.

●Applications

DVD recorders

●Absolute maximum rating (T_a=25°C)

Parameter	Symbol	Limits	Unit
Applied Voltage	VCC	15.0	V
	SCL, SDA	7.0	
Input voltage	V_{IN}	VCC+0.3～GND-0.3	V
Power Dissipation	P_d	810 *1	mW
Operating Temperature	T_{opr}	-40～+85 *2	°C
Storage Temperature	T_{astg}	-55～+150	°C

*1 Reduced by 6.5 mW/°C at 25°C or higher.
Thermal resistance θja = 154 (°C/W), when Rohm standard board is mounted.
Rohm standard board: Size: 70×70×1.6 (mm^3)
Material: FR4 glass-epoxy substrate (copper foil area: not more than 3%).

*2 As long as voltage stays within operating voltage range, certain circuit operation is guaranteed in the operating temperature range.
Allowable power loss conditions are related to temperature, to which care must be taken.
In addition though the standard value of its electrical characteristics cannot be guaranteed under the conditions other than those specified, basic functions are maintained.

●Operating range (Basic operation at Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage *3	VCC	7.0	12.0	14.5	V

*3 As long as temperature and operating voltage meet specifications
In addition, though the standard value of its electrical characteristics cannot be guaranteed under the conditions other than those specified, basic functions are maintained.

●Electrical characteristics

Unless otherwise specified, Ta=25℃, VCC=12V, f=1kHz, Vin=1Vrms, Rg=600Ω, RL=10kΩ, Gain selector = 0dB, Volume = 0dB, Input terminal = Front 1, Output terminal = Out 1

	Parameter	Symbol	Limits			Unit	Conditions
			Min.	Typ.	Max.		
GENERAL	Circuit Current upon no signal	I_Q	-	2.5	10	mA	V_{IN}=0Vrms
	Voltage gain	G_V	-1.5	0	1.5	dB	$G_V=20\log(V_{OUT}/V_{IN})$
	Maximum output voltage	V_{OM}	3.0	3.6	-	Vrms	V_{OM} at THD(V_{OUT})=1% BW=400Hz-30KHz。
	Channel balance	CB	-1.5	0	1.5	dB	CB = G_{V1}-G_{V2} G_{V1}:ch1Gain, G_{V2}:ch2 Gain
	Total harmonic distortion	THD	-	0.0015	0.05	%	V_{IN}=2Vrms,Volume=-6dB BW=400Hz-30KHz
	Output noise voltage *	V_{NO}	-	3.2	16	μVrms	Volume=-6dB R_g = 0Ω, BW=IHF-A
	Residual output noise voltage *	V_{NOR}	-	2	10	μVrms	Volume = -∞dB R_g = 0Ω, BW=IHF-A
	Cross-talk between channels *	CTC	-	-110	-80	dB	R_g = 0Ω BW = IHF-A
	Input impedance	R_{IN}	77	110	143	kΩ	1pin-10pin terminal
	Maximum input voltage	V_{IM}	3.1	3.6[1)]	-	Vrms	V_{IM} at THD(V_{OUT})=1% BW=400Hz-30KHz 1pin-10pin terminal
	Cross-talk between selectors *	CTS	-	-110	-80	dB	R_g = 0Ω BW = IHF-A $CTS=20\log(V_{OUT}/V_{IN})$
VOLUME	Volume control range	V_V	-32.5	-30.5	-28.5	dB	$GV=20\log(V_{OUT}/V_{IN})$ BW = IHF-A
	Maximum attenuation *	$G_{V\,MIN}$	-	-106	-85	dB	Volume = -∞dB $GV=20\log(V_{OUT}/V_{IN})$ BW = IHF-A
	Step resolution	$G_{V\,STEP}$	-	0.5	-	dB	Volume=0～-30.5dB
	Attenuation set error	$G_{V\,ERR}$	-1.5	0	1.5	dB	Volume=0～-30.5dB
GAIN SELECTOR	Maximum gain	G_{MAX}	4.5	6	7.5	dB	Gain Selector=6dB V_{IN}=500mVrms $G=20\log(V_{OUT}/V_{IN})$
	Step resolution	G_{STEP}	-	2	-	dB	From 2dB to 4dB
	Gain set error	G_{ERR}	-1.5	0	1.5	dB	

＊VP-9690A (average value detection, effective value display) filter by Matsushita Communication is used for * measurement.

＊Phase between input/output is the same.

＊This IC is not designed to be radiation-resistant.

1)V_{IM}=2.5Vrms(TYP) at VCC=9V、THD(V_{OUT})=1%

V_{IN}=4.2Vrms(TYP) at VCC=14V、THD(V_{OUT})=1%

●Timing chart

Electrical specifications and timing of bus lines and I/O stages

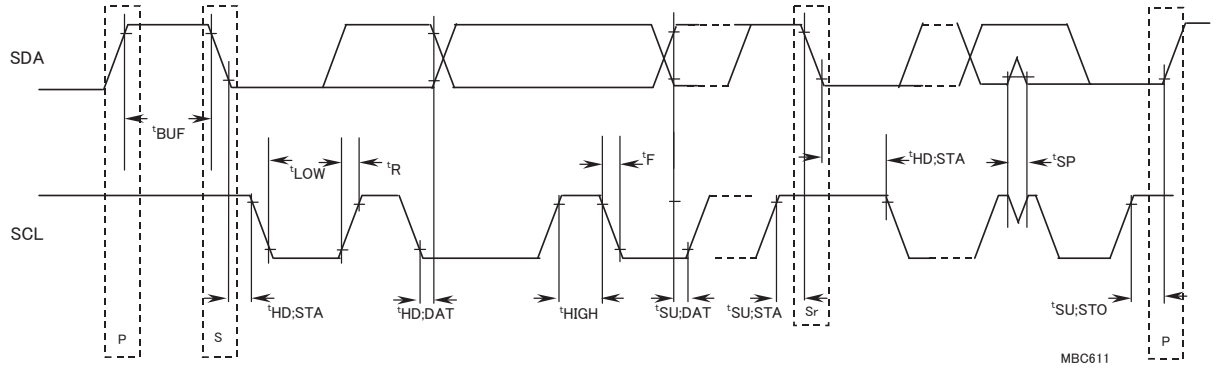


Fig.1 Timing Definition on I^2C BUS

Table 1 . Characteristics of the SDA and SCL BUS lines for I^2C BUS devices

	Parameter	Symbol	High speed mode I^2C BUS		Unit
			Min.	Max.	
1	SCL clock frequency	f_{SCL}	0	400	kHz
2	Bus free time between a STOP and START condition	t_{BUF}	1.3	-	μs
3	Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	-	μs
4	LOW period of the SCL clock	t_{LOW}	1.3	-	μs
5	HIGH period of the SCL clock	t_{HIGH}	0.6	-	μs
6	Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	μs
7	Data hold time	$t_{HD;DAT}$	0*	-	μs
8	Data set-up time	$t_{SU;DAT}$	100	-	ns
9	Rise time of both SDA and SCL signals	t_R	20+Cb	300	ns
10	Fall time of both SDA and SCL signals	t_F	20+Cb	300	ns
11	Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	μs
12	Capacitive load for each bus line	C_b	-	400	pF

The above numerical values all correspond to $V_{IH\ min}$ and $V_{IL\ max}$ levels (see Table 2).

*The input signals must internally provide at least 300 ns hold-time for SDA signals (at $V_{IH\ min}$ of SCL signals) in order to cross over undefined region at the fall-end of SCL.

Table 2. Characteristics of the SDA and SCL I/O stages for I^2C BUS devices

	Parameter	Symbol	High speed mode I2C BUS		Unit
			Min.	Max.	
13	Low-level input voltage : fixed input levels	V_{IL}	-0.5	1.0	V
14	Low-level input voltage : fixed input levels	V_{IH}	2.3	-	μs
15	Hysteresis of Schmitt trigger inputs: fixed input levels	V_{hys}	n/a	n/a	V
16	Pulse width of spikes which must be suppressed by the input filter.	t_{SP}	0	50	ns
17	Low-level output voltage (open drain): at 3mA sink current	V_{OL1}	0	0.4	V
18	Output fall time from VIHmin. to VIHmax. with a bus capacitance from 10 pF to 400pF: with up to 3mA sink current at VOL1	t_{OF}	20+0.1Cb	250	ns
19	Input current each I/O pin with an input voltage between 0.4V and 0.9 VCCmax.	I_i	-10	10	μA
20	Capacitance for each I/O pin	C_i	-	10	pF

n/a = not applicable

I²C BUS FORMAT

MSB		LSB	MSB		LSB	MSB		LSB		
S	Slave Address		A	Select Address		A	Data		A	P
1bit	8bit	1bit		8bit	1bit		8bit		1bit	1bit

S = Start condition (Recognition of start bit)

Slave Address = Recognition of slave address. 7 bits in upper order are voluntary.
Least significant bit is “L” for writing.

A = ACKNOWLEDGE bit (Recognition of acknowledgement)

Select Address =Selection of volume, etc.

Data =Data such as volume, etc.

P = Stop condition (Recognition of stop bit)

I²C BUS Interface Protocol

1) Basic form

S	Slave Address	A	Select Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2) Automatic increment (Select Address increases (+1) according to the number of data.)

S	Slave Address	A	Select Address	A	Data1	A	Data2	A	····	DataN	A	P
	MSB LSB		MSB LSB	MSB	LSB	MSB	LSB	MSB	LSB			

(例) [1] Data 1 shall be set as data of address specified by Select Address.

[2] Data 2 shall be set as data of address specified by Select Address +1.

[3] Data N shall be set as data of address specified by Select Address +N-1.

Slave Address

Because the slave address can be changed by the SELECT setting, it is possible to use two chips simultaneously on a single control BUS .

	MSB							LSB
SELECTvoltage condition	A6	A5	A4	A3	A2	A1	A0	R/W
GND ～ 0.2×VCC	1	0	0	0	0	0	0	0
0.8×VCC ～ VCC	1	0	0	0	0	1	0	0

Set the SELECT voltage within the condition defined.

Data format

Items to be set	Select Address (HEX)	MSB Data LSB							
		D7	D6	D5	D4	D3	D2	D1	D0
Input Selector	00	*	*	*	*	*	Input Selector		
Volume ch1	01	*	*	Volume attenuation ch1					
Volume ch2	02	*	*	Volume attenuation ch2					
Gain Selector	03	*	*	*	*	*	*	Gain Selector	

*Don’t care

●Application circuit diagram

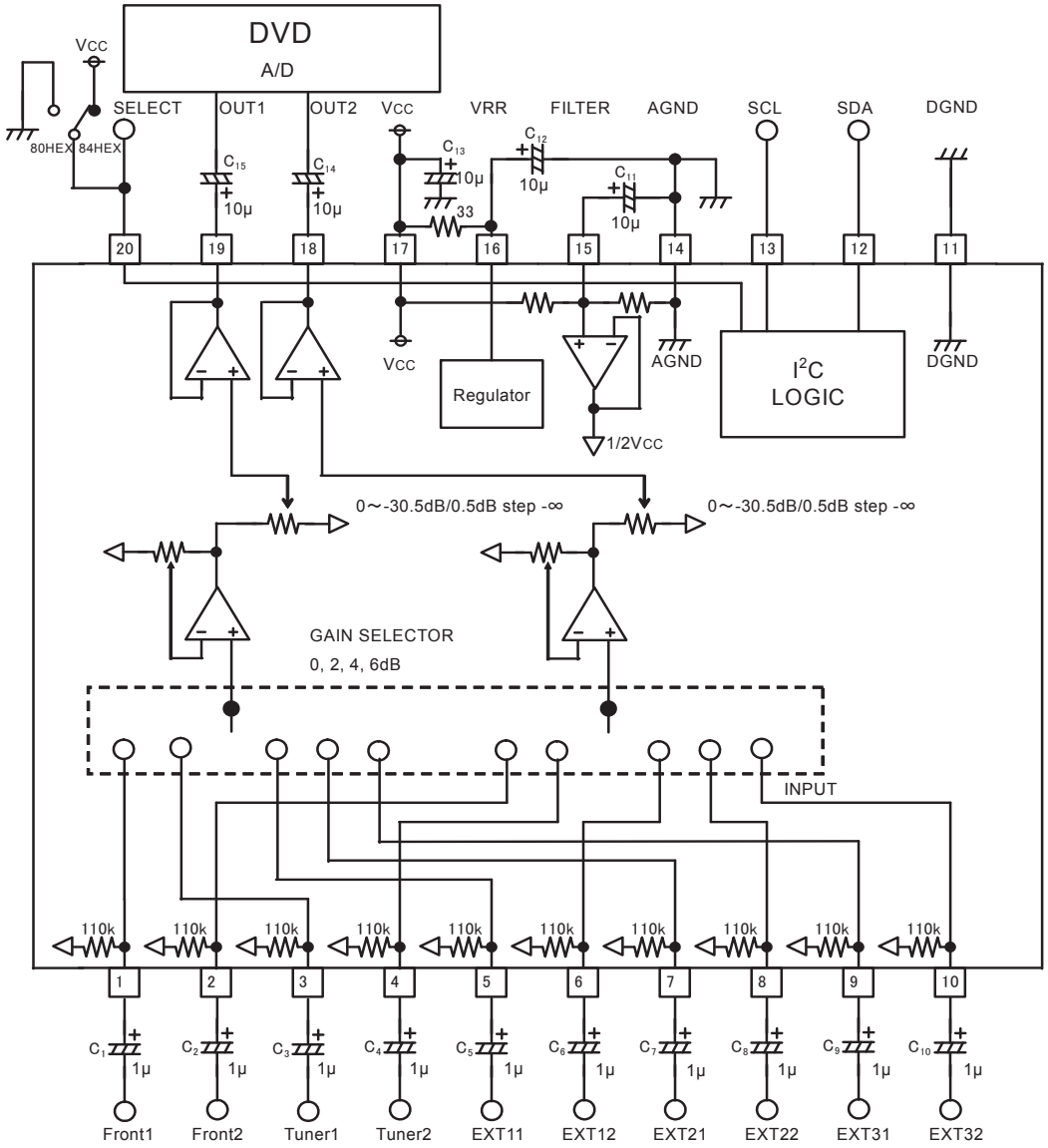


Fig.2 Application Circuit Diagram

Pin No.	Pin Name	Pin Description	Pin No.	Pin Name	Pin Description
1	Front1	Front 1ch input terminal	11	DGND	Ground ternial
2	Front2	Front 2ch input terminal	12	SDA	I^2C communication data terminal
3	Tuner1	Tuner 1 ch input	13	SCL	I^2C communication clock terminal
4	Tuner2	Tuner 2 ch input	14	AGND	Ground terminal
5	EXT11	External 1 1ch input terminal	15	FILTER	1/2Vcc terminal
6	EXT12	External 1 2ch input terminal	16	VRR	Ripple filter terminal
7	EXT21	External 2 1ch input terminal	17	Vcc	Power supply terminal
8	EXT22	External 2 2ch input terminal	18	OUT2	Volume 2ch output terminal
9	EXT31	External 3 1ch input terminal	19	OUT1	Volume 1ch output terminal
10	EXT32	External 3 2ch input terminal	20	SELECT	Slave address selection terminal

●**Reference data**

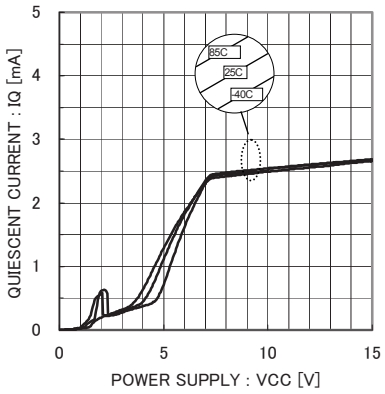


Fig.3 Quiescent Current vs. Power Supply

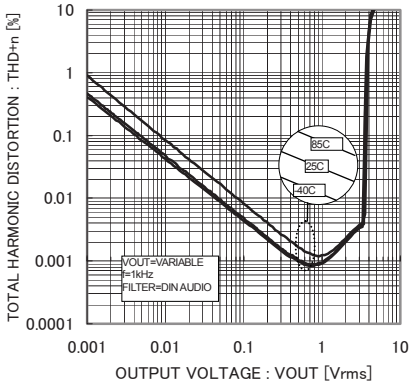


Fig.4 Total harmonic distortion vs. Output Voltage

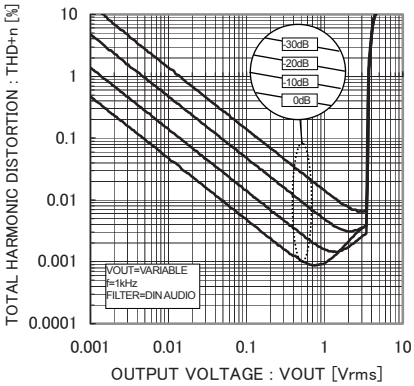


Fig.5 Total harmonic distortion vs. Output voltage

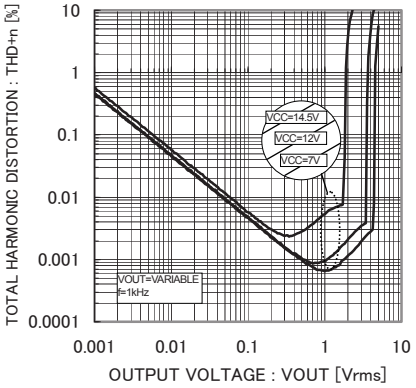


Fig.6 Total harmonic distortion vs. Output voltage

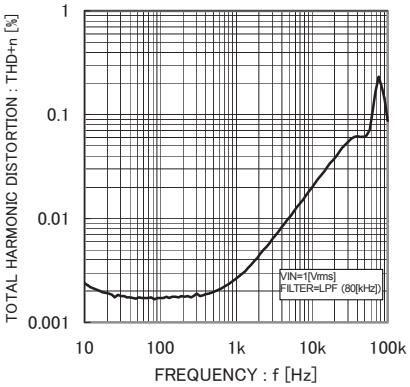


Fig.7 Total harmonic distortion vs. Frequency

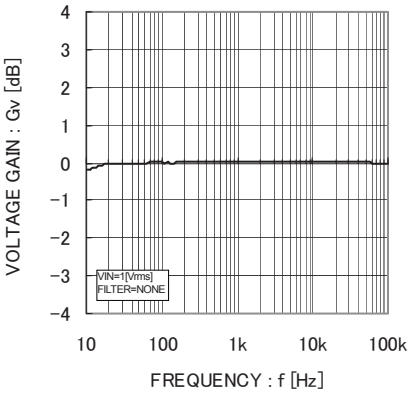


Fig.8 Voltage gain vs. Frequency

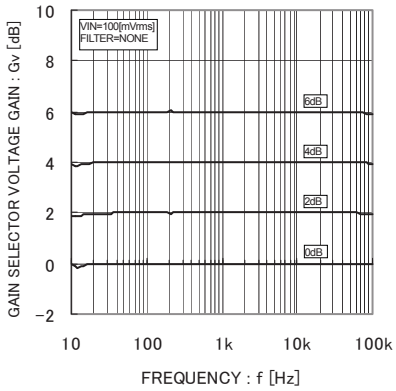


Fig.9 Gain selector voltage gain vs. Frequency

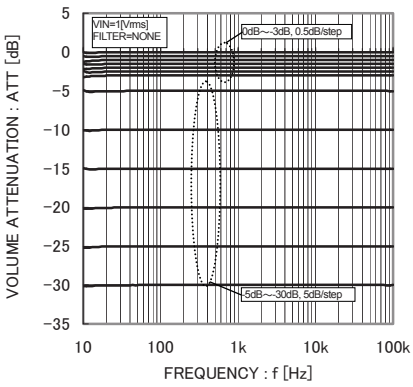


Fig.10 Volume attenuation vs. Frequency

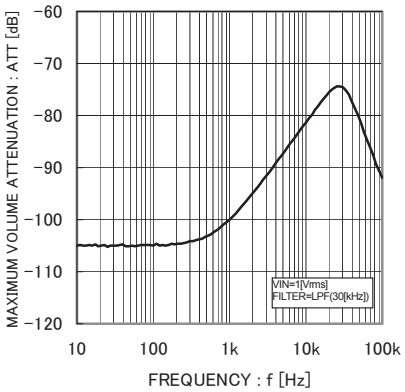


Fig.11 Maximum volume attenuation vs. Frequency

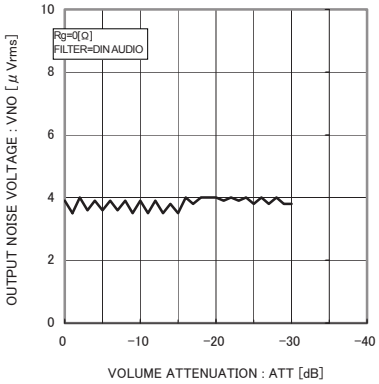


Fig.12 Volume attenuation vs. voltage attenuation

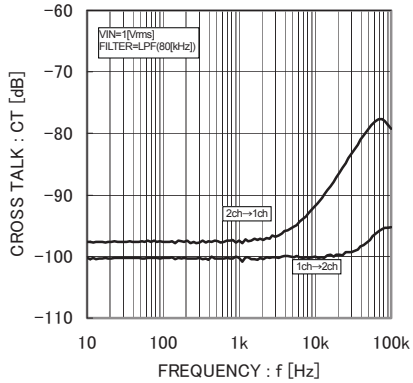


Fig.13 Cross Talk vs. Frequency

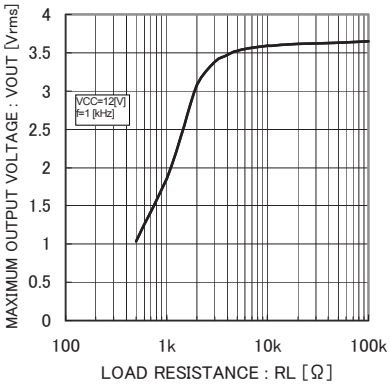


Fig.14 Maximum output voltage vs. Load resistance

●How to select application parts

Initial condition when power supply (17 pin) is turned ON

A circuit that carries out initialization in IC, when power supply (17 pin) is turned ON is incorporated. Settings are as shown in the following table. However, it is recommended to transmit the data to all the addresses as initial data when power is turned ON, and to apply mute while the initial data is input

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
VCC rise time	Trise	20	-	-	μS	VCC rise time from 0V to 3V
VCC voltage when power on reset is released.	Vpor	-	2.6	-	V	

Function	Initial Condition
Input Selector	Input MUTE
Volume	-∞dB
Gain SERECTOR	0dB

Signal input section

1) Setting for input coupling capacitor

In the signal input terminal, set the constant for the input coupling capacitor C(F), taking the input impedance R_{IN} (Ω) inside into account. This makes up the primary HPF characteristics of the RC.

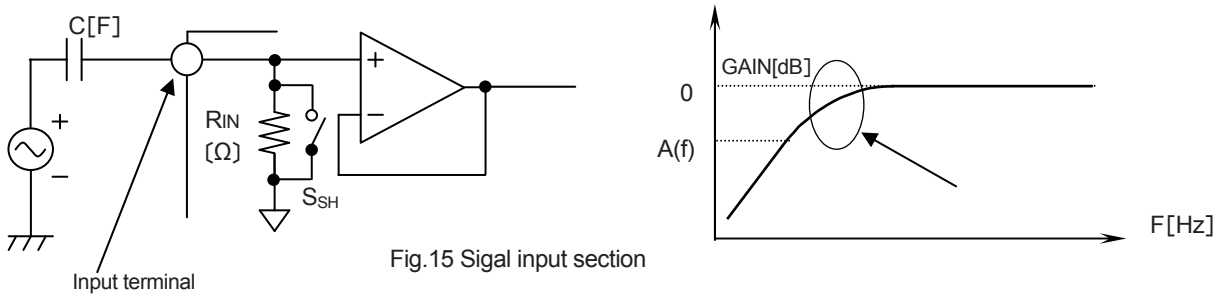


Fig.15 Sigal input section

2) SHORT mode of input

SHORT mode is a command to reduce resistance by setting impedance R_{IN} to switch S_{SH}=ON. When SHORT command is not chosen, switch S_{SH} is turned OFF. By using this command, it is possible to stop charging externally mounted coupling capacitor C. Use SHORT mode when there is no signal since the SHORT mode turns ON the S_{SH} switch in order to achieve low impedance.

● Operation Notes

1. Numbers and data in entries are representative design values and are not guaranteed values of the items.
2. Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.
3. Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.
4. GND potential
   Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.
5. Thermal design
   Perform thermal design, in which there are adequate margins, by taking into account the permissible dissipation (Pd) in actual states of use.
6. Short circuit between terminals and erroneous mounting
   Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.
7. Operation in strong electromagnetic field
   Using the ICs in a strong electromagnetic field can cause operation malfunction.

●**Selection of order type**

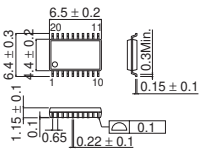
B	D	3	8	2	3	F	V	—	E	2

Part No.
BD3823FV

Tape and Reel information

SSOP-B20

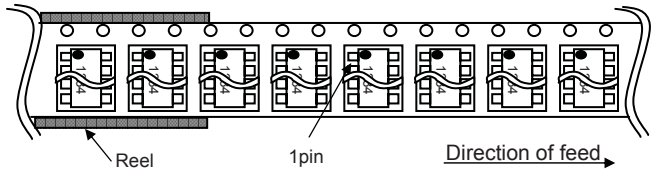
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (Correct direction: 1pin of product should be at the upper left when you hold reel on the left hand, and you pull out the tape on the right hand)



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It is our top priority to supply products with the utmost quality and reliability. However, there is always a chance of failure due to unexpected factors. Therefore, please take into account the derating characteristics and allow for sufficient safety features, such as extra margin, anti-flammability, and fail-safe measures when designing in order to prevent possible accidents that may result in bodily harm or fire caused by component failure. ROHM cannot be held responsible for any damages arising from the use of the products under conditions out of the range of the specifications or due to non-compliance with the NOTES specified in this catalog.

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact your nearest sales office.

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