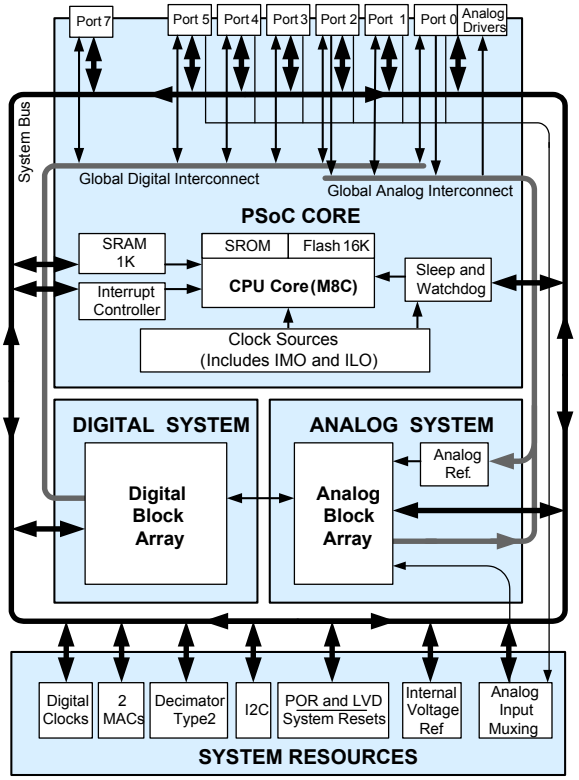
CY8CTMA120

Automotive TrueTouch™ Multi-Touch All-Point Touchscreen Controller

Features

- TrueTouch™ Capacitive Touchscreen Controller
  - Supports Multi-Touch All-Point Touchscreen Applications
  - Supports up to 37 X/Y Sensor Inputs
  - Supports Screen Sizes 7.3 inch and Below (Typical)
  - Fast Scan Rates: Typical 120 us per X/Y Crossing
  - High Resolution: Typical 480 x 360 for 3.5-inch Screen
  - Available in 56-Pin QFN Package
  - AEC Qualified
- Multi-Touch All-Point Addressable Detection
  - Capable of Tracking up to 10 Independent Fingers
  - Allows Development of Customized Multi-Finger Gestures
- Lowest Noise TrueTouch Device
- Highly Configurable Sensing Circuitry
  - Enables Maximum Design Flexibility
  - Enables Trade-Off Between Scan Time and Noise Performance
- Powerful Harvard Architecture Processor
  - M8C Processor Speeds to 24 MHz
  - Two 8x8 Multiply, 32-Bit Accumulate
  - Low Power at High Speed
  - 3V to 5.25V Operating Voltage
  - Automotive Temperature Range: –40°C to +85°C
- Flexible On-Chip Memory
  - 16K Flash Program Storage, 1000 Erase/Write Cycles
  - 1K SRAM Data Storage
  - In-System Serial Programming (ISSP)
  - Partial Flash Updates
  - Flexible Protection Modes
  - EEPROM Emulation in Flash
- Precision, Programmable Clocking
  - Internal ±4% 24 and 48 MHz Oscillator
  - Internal Oscillator for Watchdog and Sleep
- Additional System Resources
  - I2C Slave, Master, and Multi-Master to 400 kHz
  - Watchdog and Sleep Timers
  - User-Configurable Low Voltage Detection
  - Integrated Supervisory Circuit
  - On-Chip Precision Voltage Reference
- Complete Development Tools
  - Free Development Software (PSoC Designer™)
  - TrueTouch Touchscreen Tuner
  - Full-Featured, In-Circuit Emulator and Programmer
  - Full Speed Emulation
  - Complex Breakpoint Structure
  - 128K Bytes Trace Memory
- Programmable Pin Configurations
  - 25 mA Sink, 10 mA Drive on All GPIO
  - Pull Up, Pull Down, High Z, Strong, or Open Drain Drive Modes on All GPIO

Logic Block Diagram



TrueTouch Functional Overview

The TrueTouch family provides the fastest and most efficient way to develop and tune a capacitive touchscreen application. A TrueTouch device includes the configurable TrueTouch block, configurable analog and digital logic, programmable interconnect, and an 8-bit CPU to run custom firmware. This architecture enables the user to create flexible, customized touchscreen configurations to match the requirements of each individual touchscreen application. Various configurations of Flash program memory, SRAM data memory, and configurable IO are included in a range of convenient pinouts.

The TrueTouch architecture is comprised of four main areas: the Core, Digital System, the TrueTouch Analog System, and System Resources. Configurable global busing allows all the device resources to be combined into a complete custom touchscreen system. The CY8CTMA120 device can have up to seven IO ports that connect to the global digital and analog interconnects, providing access to four digital blocks and six analog blocks. Implementation of touchscreen application allows additional digital and analog resources to be used, depending on the touchscreen design. The CY8CTMA120 is offered in a 56-pin QFN package with up to 48 general purpose IO (GPIO), and support of up to 37 X/Y sensors.

When designing touchscreen applications, refer to the UM data sheet for performance requirements to meet and detailed design process explanation.

The TrueTouch Core

The core includes a CPU, memory, clocks, and configurable GPIO (General Purpose IO).

The M8C CPU core is a powerful processor with speeds up to 24 MHz, providing a four MIPS 8-bit Harvard architecture microprocessor. The CPU uses an interrupt controller with up to 20 vectors, to simplify programming of real time embedded events. Program execution is timed and protected using the included Sleep and Watch Dog Timers (WDT).

Memory encompasses 16K of Flash for program storage, 1K of SRAM for data storage, and up to 2K of EEPROM emulated using the Flash. Program Flash uses four protection levels on blocks of 64 bytes, allowing customized software IP protection.

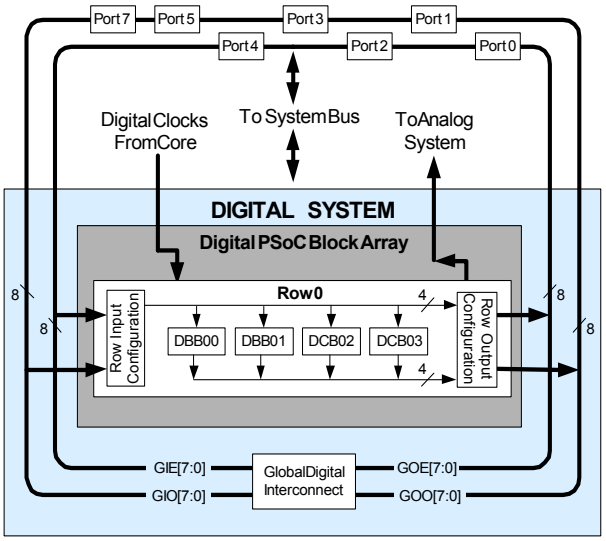
The TrueTouch device incorporates flexible internal clock generators, including a 24 MHz IMO (Internal Main Oscillator) accurate to 8 percent over temperature and voltage. The 24 MHz IMO can also be doubled to 48 MHz for use by the digital system. A low power 32 kHz ILO (Internal Low speed Oscillator) is provided for the sleep timer and WDT. The clocks, together with programmable clock dividers (as a System Resource), provide the flexibility to integrate almost any timing requirement into the TrueTouch device.

The GPIOs provide connection to the CPU, digital and analog resources of the device. Each pin's drive mode may be selected from eight options, allowing great flexibility in external interfacing. Every pin is also capable of generating a system interrupt on high level, low level, and change from last read.

The Digital System

The Digital System comprises four digital resources. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user module references.

Figure 1. Digital System Block Diagram



Digital peripheral configurations include those listed below.

- PWMs (8 to 32 bit)
- PWMs with dead band (8 to 24 bit)
- Counters (8 to 32 bit)
- Timers (8 to 32 bit)
- UART 8 bit with selectable parity
- SPI master and slave
- I2C slave and multi-master
- Pseudo Random Sequence Generators (8 to 32 bit)

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow signal multiplexing and performing logic operations. This configurability frees the designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by TrueTouch device family. This allows optimum choice of system resources for your application. Family characteristics are shown in Table 1 on page 4.

The Analog System

The Analog System is composed of six configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Implementation of touchscreen application allows additional analog resources to be used, depending on the touchscreen design. Analog peripherals are very flexible and are customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are listed below.

- Analog-to-digital converters (up to 2, with 6 to 14-bit resolution, selectable as Incremental, Delta Sigma, and SAR)
- Filters (2 and 4 pole band-pass, low-pass, and notch)
- Amplifiers (up to 2, with selectable gain to 48x)
- Instrumentation amplifiers (1 with selectable gain to 93x)
- Comparators (up to 2, with 16 selectable thresholds)
- DACs (up to 2, with 6- to 9-bit resolution)
- Multiplying DACs (up to 2, with 6- to 9-bit resolution)
- High current output drivers (two with 30 mA drive as a PSoC Core Resource)
- 1.3V reference (as a System Resource)
- Modulators
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are arranged in a column of three, which includes one CT (Continuous Time) and two SC (Switched Capacitor) blocks, as shown in Figure 2.

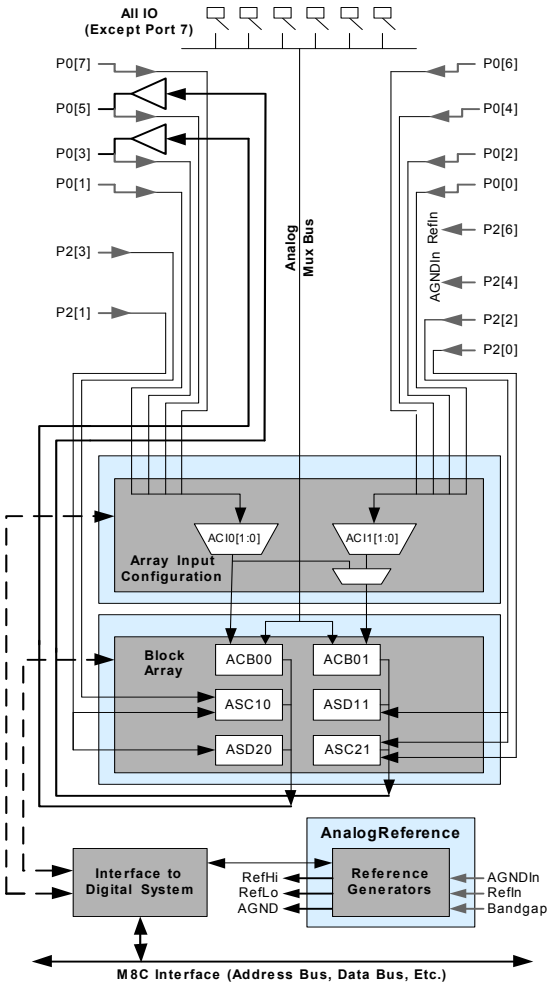
The Analog Multiplexer System

The Analog Mux Bus connects to every GPIO pin in ports 0-5. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for capacitive sensing with the TrueTouch block comparator. It is split into two sections for simultaneous dual-channel processing. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch control logic enables selected pins to switch dynamically under hardware control. This enables capacitive measurement for the touchscreen applications. Other multiplexer applications include:

- Chip-wide mux that allows analog input from up to 48 I/O pins.
- Electrical connection between any IO pin combinations.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, provide additional capability useful to complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each resource follow.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks are routed to both the digital and analog systems. Additional clocks are generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multipliers with 32-bit accumulate, to assist in both general math and digital filters.
- Decimator provides a custom hardware filter for digital signal processing applications, including creation of Delta Sigma ADCs.

- The I2C module provides 100 and 400 kHz communication over two wires. Slave, master, multi-master are supported.
- Low Voltage Detection (LVD) interrupts signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3V reference provides an absolute reference for the analog system, including ADCs and DACs.
- Versatile analog multiplexer system.

Getting Started

The quickest way to understand TrueTouch device is to read this data sheet and then use the PSoC Designer Integrated Development Environment (IDE). This data sheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the PSoC® Programmable System-on-Chip Technical Reference Manual for CY8C28xxx PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device data sheets on the web at www.cypress.com/psoc.

TrueTouch Device Characteristics

Depending on the TrueTouch device selected for a touchscreen application, characteristics and capabilities of each device change. Table 1 lists the touchscreen sensing capabilities available for specific TrueTouch devices. The TrueTouch device covered by this data sheet is highlighted in this table.

Table 1. TrueTouch Device Characteristics

TrueTouch Part Number	Sensor Inputs	Max Screen Size (Inches)	Single-Touch	Multi-Touch Gesture	Multi-Touch All-Point	Scan Speed (ms)[1]	Current Consumption[2]	Flash Size	SRAM Size
CY8CTMG120	up to 44	8.4	Y	Y	N	0.5	16	16K	1K
CY8CTMA120	up to 37	7.3”	Y	Y	Y	0.12	16	16K	1K

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They are located here: www.cypress.com/psoc. Select Application Notes under the Documentation tab.

Development Kits

PSoC Development Kits are available online from Cypress at www.cypress.com/shop and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at www.cypress.com/training. The training covers a wide variety of topics and skill levels to assist you in your designs.

Cypros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to www.cypress.com/cypros.

Solutions Library

Visit our growing library of solution focused designs at www.cypress.com/solutions. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at www.cypress.com/support. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Notes
1. Per sensor typical. Depends on touchscreen panel. For MA120 per X/Y crossing Vcc = 3.3V.
2. Average mA supply current. Based on 8 ms report rate, except for MA120.

Development Tools

PSoC Designer is a Microsoft® Windows-based, integrated development environment for the Programmable System-on-Chip (PSoC) devices. The PSoC Designer IDE runs on Windows XP or Windows Vista.

This system provides design database management by project, an integrated debugger with In-Circuit Emulator, in-system programming support, and built-in support for third-party assemblers and C compilers.

PSoC Designer also supports C language compilers developed specifically for the devices in the PSoC family.

PSoC Designer Software Subsystems

System-Level View

A drag-and-drop visual embedded system design environment based on PSoC Express. In the system level view you create a model of your system inputs, outputs, and communication interfaces. You define when and how an output device changes state based upon any or all other system devices. Based upon the design, PSoC Designer automatically selects one or more PSoC Mixed-Signal Controllers that match your system requirements.

PSoC Designer generates all embedded code, then compiles and links it into a programming file for a specific PSoC device.

Chip-Level View

The chip-level view is a more traditional integrated development environment (IDE) based on PSoC Designer 4.4. Choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The device editor also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic configuration allows for changing configurations at run time.

Hybrid Designs

You can begin in the system-level view, allow it to choose and configure your user modules, routing, and generate code, then switch to the chip-level view to gain complete control over on-chip resources. All views of the project share a common code editor, builder, and common debug, emulation, and programming tools.

Code Generation Tools

PSoC Designer supports multiple third party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to merge seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices.

The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

The PSoC Designer Debugger subsystem provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write IO registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help for the user. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer in getting started.

Hardware Tools

In-Circuit Emulator

A low cost, high functionality ICE (In-Circuit Emulator) is available for development support. This hardware has the capability to program single devices.

The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24 MHz) operation.

TrueTouch Touchscreen Tuner

The TrueTouch tuner is a Microsoft® Windows based graphical user interface allowing developers to set critical parameters and observe changes to the touchscreen application in real time. Optimal configuration from the tuner are immediately applied to the TrueTouch user module settings.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select components
2. Configure components
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

Both the system-level and chip-level views provide a library of prebuilt, pretested hardware peripheral components. In the system-level view, these components are called “drivers” and correspond to inputs (a thermistor, for example), outputs (a brushless DC fan, for example), communication interfaces (I^2C-bus, for example), and the logic to control how they interact with one another (called valuators).

In the chip-level view, the components are called “user modules”. User modules make selecting and implementing peripheral devices simple, and come in analog, digital, and mixed signal varieties.

Configure Components

Each of the components you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a Pulse Width Modulator (PWM) User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus.

Both the system-level drivers and chip-level user modules are documented in data sheets that are viewed directly in the PSoC Designer. These data sheets explain the internal operation of the component and provide performance specifications. Each data sheet describes the use of each user module parameter or driver property, and other information you may need to successfully implement your design.

Organize and Connect

You can build signal chains at the chip level by interconnecting user modules to each other and the IO pins, or connect system level inputs, outputs, and communication interfaces to each other with valuator functions.

In the system-level view, selecting a potentiometer driver to control a variable speed fan driver and setting up the valuators to control the fan speed based on input from the pot selects, places, routes, and configures a programmable gain amplifier (PGA) to buffer the input from the potentiometer, an analog to digital converter (ADC) to convert the potentiometer’s output to a digital signal, and a PWM to control the fan.

In the chip-level view, perform the selection, configuration, and routing so that you have complete control over the use of all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Application” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system.

Both system-level and chip-level designs generate software based on your design. The chip-level design provides application programming interfaces (APIs) with high level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed. The system-level design also generates a C main() program that completely controls the chosen application and contains placeholders for custom code at strategic positions allowing you to further refine the software without disrupting the generated code.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside the PSoC Designer’s Debugger subsystem. The Debugger downloads the HEX image to the ICE where it runs at full speed. Debugger capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint and watch-variable features, the Debugger provides a large trace buffer and allows you define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Document Conventions

Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CPU	central processing unit
CT	continuous time
DAC	digital-to-analog converter
DC	direct current
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
FSR	full scale range
GPIO	general purpose IO
GUI	graphical user interface
HBM	human body model
ICE	in-circuit emulator
ILO	internal low speed oscillator
IMO	internal main oscillator
IO	input/output
IPOR	imprecise power on reset
LSb	least-significant bit
LVD	low voltage detect
MSb	most-significant bit
PC	program counter
PLL	phase-locked loop
POR	power on reset
PPOR	precision power on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse width modulator
SC	switched capacitor
SRAM	static random access memory

Units of Measure

A units of measure table is located in the Electrical Specifications section. Table 3 on page 9 lists all the abbreviations used to measure the PSoC devices.

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers are also represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘0x’, or ‘b’ are decimal.

Pinouts

This section describes, lists, and illustrates the CY8CTMA120 TrueTouch family pins and pinout configuration. The CY8CTMA120 TrueTouch device is available in the following packages, all of which are shown on the following pages. Every port pin (labeled “P”) is capable of Digital IO. However, Vss, Vdd, and XRES are not capable of Digital IO.

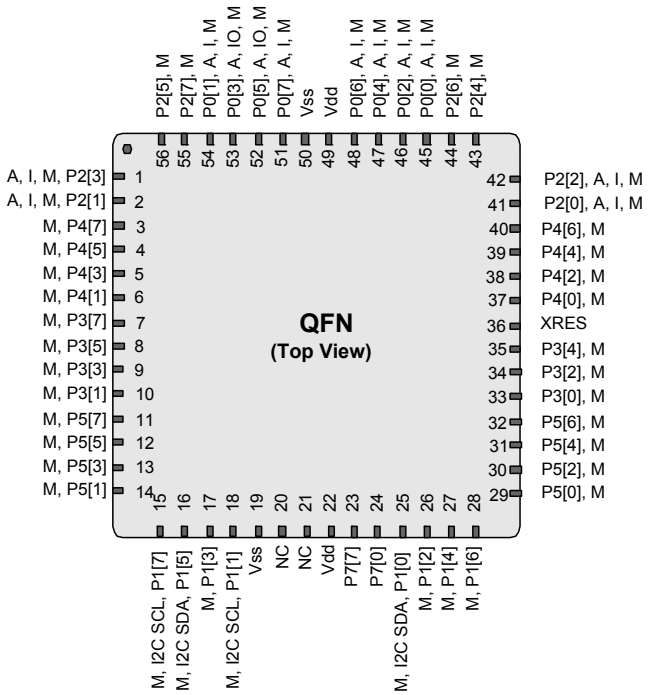
56-Pin Part Pinout

Table 2. 56-Pin Part Pinout (QFN)

Pin No.	Type		Name	Description
	Digital	Analog		
1	IO	I, M	P2[3]	VREF
2	IO	I, M	P2[1]	SNS_OUT(Output of external OP-AMP)
3	IO	M	P4[7]	
4	IO	M	P4[5]	
5	IO	M	P4[3]	
6	IO	M	P4[1]	
7	IO	M	P3[7]	
8	IO	M	P3[5]	
9	IO	M	P3[3]	
10	IO	M	P3[1]	
11	IO	M	P5[7]	
12	IO	M	P5[5]	
13	IO	M	P5[3]	
14	IO	M	P5[1]	
15	IO	M	P1[7]	phi2 (Control for high precision switches)
16	IO	M	P1[5]	phi1 (Control for high precision switches).
17	IO	M	P1[3]	
18	IO	M	P1[1]	I2C Serial Data (SDA), ISSP DATA[3].
19	Power		Vss	Ground. Connect to circuit ground.
20	NC			
21	NC			
22	Power		Vdd	Supply voltage. Bypass to ground with 0.1 uF capacitor.
23	IO		P7[7]	
24	IO		P7[0]	SHDN
25	IO	M	P1[0]	I2C Serial IRQ (Interrupt), ISSP CLK[3].
26	IO	M	P1[2]	
27	IO	M	P1[4]	
28	IO	M	P1[6]	
29	IO	M	P5[0]	
30	IO	M	P5[2]	
31	IO	M	P5[4]	
32	IO	M	P5[6]	
33	IO	M	P3[0]	
34	IO	M	P3[2]	
35	IO	M	P3[4]	
36	Input		XRES	Active high external reset with internal pull down.
37	IO	M	P4[0]	
38	IO	M	P4[2]	
39	IO	M	P4[4]	
40	IO	M	P4[6]	
41	IO	I, M	P2[0]	Direct switched capacitor block input.
42	IO	I, M	P2[2]	Direct switched capacitor block input.
43	IO	M	P2[4]	VREF.
44	IO	M	P2[6]	VREF.
45	IO	I, M	P0[0]	Analog column mux input.
46	IO	I, M	P0[2]	Analog column mux input.
47	IO	I, M	P0[4]	Analog column mux input.
48	IO	I, M	P0[6]	Analog column mux input.
49	Power		Vdd	Supply voltage. Bypass to ground with 0.1 uF capacitor.
50	Power		Vss	Ground. Connect to circuit ground.
51	IO	I, M	P0[7]	Rx.
52	IO	IO, M	P0[5]	Tx.
53	IO	IO, M	P0[3]	Analog column mux input and column output.
54	IO	I, M	P0[1]	Analog column mux input.
55	IO	M	P2[7]	
56	IO	M	P2[5]	
EP	Power		Vss	Exposed pad is internally connected to ground. Connect to circuit ground.

LEGEND A = Analog, I = Input, O = Output, and M = Analog Mux Input.

Figure 3. CY8CTMA120 56-Pin PSoC Device



Note
3. These are the ISSP pins, which are not High Z at POR

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8CTMA120 TrueTouch device family. For the most up to date electrical specifications, confirm that you have the most recent data sheet by going to the web at http://www.cypress.com/psoc.

Specifications are valid for -40°C ≤ T_A ≤ 85°C and T_J ≤ 100°C, except where noted.

Figure 4. Voltage versus CPU Frequency

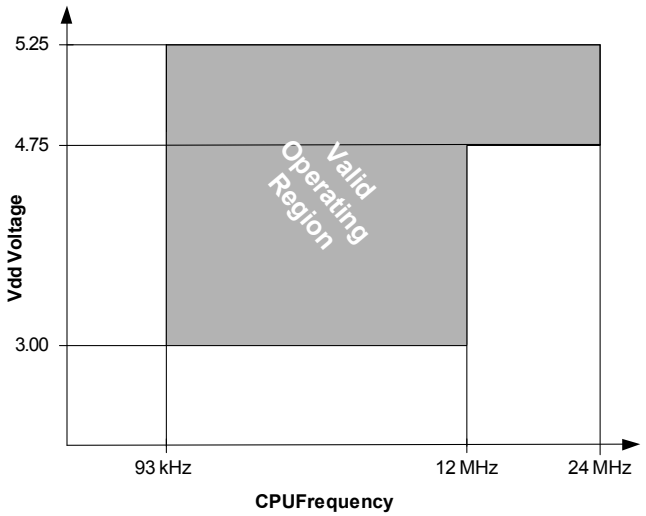


Table 3 lists the units of measure that are used in this section.

Table 3. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µW	microwatts
dB	decibels	mA	milli-ampere
fF	femto farad	ms	milli-second
Hz	hertz	mV	milli-volts
KB	1024 bytes	nA	nanoampere
Kbit	1024 bits	ns	nanosecond
kHz	kilohertz	nV	nanovolts
kΩ	kilohm	W	ohm
MHz	megahertz	pA	picoampere
MΩ	megaohm	pF	picofarad
µA	microampere	pp	peak-to-peak
µF	microfarad	ppm	parts per million
µH	microhenry	ps	picosecond
µs	microsecond	sps	samples per second
µV	microvolts	s	sigma: one standard deviation
µVrms	microvolts root-mean-square	V	volts

Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage Temperature	-55	25	+100	°C	Higher storage temperatures reduces data retention time. Recommended storage temperature is +25°C ± 25°C. Extended duration storage temperatures above 65°C degrades reliability.
T_A	Ambient Temperature with Power Applied	-40	–	+85	°C	
Vdd	Supply Voltage on Vdd Relative to Vss	-0.5	–	+6.0	V	
V_{IO}	DC Input Voltage	Vss - 0.5	–	Vdd + 0.5	V	
V_{IO2}	DC Voltage Applied to Tri-state	Vss - 0.5	–	Vdd + 0.5	V	
I_{MIO}	Maximum Current into any Port Pin	-25	–	+50	mA	
I_{MAIO}	Maximum Current into any Port Pin Configured as Analog Driver	-50	–	+50	mA	
ESD	Electro Static Discharge Voltage[4]	2000	–	–	V	Human Body Model ESD.
LU	Latch Up Current	–	–	200	mA	

Operating Temperature

Table 5. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient Temperature[5]	-40	–	+85	°C	
T_J	Junction Temperature	-40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 30 on page 26. The user must limit the power consumption to comply with this requirement.

Notes
4. See the user module data sheet for touchscreen application related ESD testing.
5. See the user module data sheet for touchscreen application related temperature testing.

DC Electrical Characteristics

The following electrical characteristics are for proper CPU core and IO operation. For capacitive touchscreen electrical characteristics, refer to the touchscreen user module data sheet.

DC Chip Level Specifications

Table 6 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 6. DC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	3.0	–	5.25	V	See DC POR and LVD specifications, Table 17 on page 17.
I_{DD5}	Supply Current, IMO = 24 MHz (5V)	–	14	27	mA	Conditions are Vdd = 5.0V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 93.75 kHz, analog power = off.
I_{DD3}	Supply Current, IMO = 24 MHz (3.3V)	–	8	14	mA	Conditions are Vdd = 3.3V, T_A = 25 °C, CPU = 3 MHz, SYSCLK doubler disabled, VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.367 kHz, analog power = off.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[6]	–	3	6.5	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, -40 °C ≤ T_A ≤ 55 °C, analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature.[6]	–	4	25	µA	Conditions are with internal slow speed oscillator, Vdd = 3.3V, 55 °C < T_A ≤ 85 °C, analog power = off.

DC General Purpose IO Specifications

Table 7 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 7. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull Up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull Down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	Vdd - 1.0	–	–	V	IOH = 10 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined IOH budget.
V_{OL}	Low Output Level	–	–	0.75	V	IOL = 25 mA, Vdd = 4.75 to 5.25V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 200 mA maximum combined IOL budget.
V_{IL}	Input Low Level	–	–	0.8	V	Vdd = 3.0 to 5.25.
V_{IH}	Input High Level	2.1	–		V	Vdd = 3.0 to 5.25.
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 µA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25°C.

Note
6. Standby current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

DC Operational Amplifier Specifications

Table 8 and Table 9 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

The Operational Amplifier is a component of both the Analog Continuous Time PSoC blocks and the Analog Switched Capacitor PSoC blocks. The guaranteed specifications are measured in the Analog Continuous Time PSoC block.

Table 8. 5V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	–	 1.6 1.3 1.2	 10 8 7.5	 mV mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range Common Mode Voltage Range (high power or high opamp bias)	0.0 0.5	– –	Vdd Vdd - 0.5	V	The common mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 60 60 80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.5	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 0.2 0.2 0.5	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	65	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

Table 9. 3.3V DC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input Offset Voltage (absolute value) Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = High High Power is 5V Only	 – –	 1.65 1.32	 10 8	 mV mV	
TCV_{OSOA}	Average Input Offset Voltage Drift	–	7.0	35.0	µV/°C	
I_{EBOA}	Input Leakage Current (Port 0 Analog Pins)	–	20	–	pA	Gross tested to 1 µA.
C_{INOA}	Input Capacitance (Port 0 Analog Pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25°C.
V_{CMOA}	Common Mode Voltage Range	0.2	–	Vdd - 0.2	V	The common mode input voltage range is measured through an analog output buffer. The specification includes the limitations imposed by the characteristics of the analog output buffer.
G_{OLOA}	Open Loop Gain Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	 60 60 80	–	–	dB	
$V_{OHIGHOA}$	High Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High is 5V only	 Vdd - 0.2 Vdd - 0.2 Vdd - 0.2	 – – –	 – – –	 V V V	
V_{OLOWOA}	Low Output Voltage Swing (internal signals) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = Low Power = High, Opamp Bias = Low	 – – –	 – – –	 0.2 0.2 0.2	 V V V	
I_{SOA}	Supply Current (including associated AGND buffer) Power = Low, Opamp Bias = Low Power = Low, Opamp Bias = High Power = Medium, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = Low Power = High, Opamp Bias = High	 – – – – – –	 400 500 800 1200 2400 4600	 800 900 1000 1600 3200 6400	 µA µA µA µA µA µA	
$PSRR_{OA}$	Supply Voltage Rejection Ratio	65	80	–	dB	Vss ≤ VIN ≤ (Vdd - 2.25) or (Vdd - 1.25V) ≤ VIN ≤ Vdd.

DC Low Power Comparator Specifications

Table 10 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 10. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low Power Comparator (LPC) Reference Voltage range	0.2	–	Vdd - 1	V	
I_{SLPC}	LPC Supply Current	–	10	40	µA	
V_{OSLPC}	LPC Voltage Offset	–	2.5	30	mV	

DC IDAC Resolution

Table 11 lists IDAC typical resolution. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 11. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DAC}	Current output of 1 LSB (1x Setting)	-	75	-	nA	

DC Analog Output Buffer Specifications

Table 12 and Table 13 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 12. 5V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common Mode Input Voltage Range	0.5	–	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 0.6 0.6	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.1 0.5 x Vdd + 1.1	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32 ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.3 0.5 x Vdd - 1.3	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	53	64	–	dB	(0.5 x Vdd - 1.3) ≤ V_{OUT} ≤ (Vdd - 2.3).

Table 13. 3.3V DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	12	mV	
TCV_{OSOB}	Average Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common Mode Input Voltage Range	0.5	-	Vdd - 1.0	V	
R_{OUTOB}	Output Resistance Power = Low Power = High	 – –	 1 1	 – –	 Ω Ω	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 0.5 x Vdd + 1.0 0.5 x Vdd + 1.0	 – –	 – –	 V V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 1K ohms to Vdd/2) Power = Low Power = High	 – –	 – –	 0.5 x Vdd - 1.0 0.5 x Vdd - 1.0	 V V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 –	 0.8 2.0	 2.0 4.3	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	34	64	–	dB	$(0.5 \times Vdd - 1.0) \leq V_{OUT} \leq (0.5 \times Vdd + 0.9)$.

DC Analog Reference Specifications

Table 14 and Table 15 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

The guaranteed specifications are measured through the Analog Continuous Time PSoC blocks. The power levels for AGND refer to the power of the Analog Continuous Time PSoC block. The power levels for RefHi and RefLo refer to the Analog Reference Control register. The limits stated for AGND include the offset error of the AGND buffer local to the Analog Continuous Time PSoC block. Reference control power is high.

Table 14. 5V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[7]	Vdd/2 - 0.04	Vdd/2 - 0.01	Vdd/2 + 0.007	V
–	AGND = 2 x BandGap[7]	2 x BG - 0.048	2 x BG - 0.030	2 x BG + 0.024	V
–	AGND = P2[4] (P2[4] = Vdd/2)[7]	P2[4] - 0.011	P2[4]	P2[4] + 0.011	V
–	AGND = BandGap[7]	BG - 0.009	BG + 0.008	BG + 0.016	V
–	AGND = 1.6 x BandGap[7]	1.6 x BG - 0.022	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Block to Block Variation (AGND = Vdd/2)[7]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Vdd/2 + BG - 0.10	Vdd/2 + BG	Vdd/2 + BG + 0.10	V
–	RefHi = 3 x BandGap	3 x BG - 0.06	3 x BG	3 x BG + 0.06	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3V)	2 x BG + P2[6] - 0.113	2 x BG + P2[6] - 0.018	2 x BG + P2[6] + 0.077	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	P2[4] + BG - 0.130	P2[4] + BG - 0.016	P2[4] + BG + 0.098	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] + P2[6] - 0.133	P2[4] + P2[6] - 0.016	P2[4] + P2[6]+ 0.100	V
–	RefHi = 3.2 x BandGap	3.2 x BG - 0.112	3.2 x BG	3.2 x BG + 0.076	V
–	RefLo = Vdd/2 – BandGap	Vdd/2 - BG - 0.04	Vdd/2 - BG + 0.024	Vdd/2 - BG + 0.04	V

Note
7. AGND tolerance includes the offsets of the local buffer in the PSoC block. Bandgap voltage is 1.3V ± 0.02V.

Table 14. 5V DC Analog Reference Specifications *(continued)*

Symbol	Description	Min	Typ	Max	Units
–	RefLo = BandGap	BG - 0.06	BG	BG + 0.06	V
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 1.3V)	2 x BG - P2[6] - 0.084	2 x BG - P2[6] + 0.025	2 x BG - P2[6] + 0.134	V
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	P2[4] - BG - 0.056	P2[4] - BG + 0.026	P2[4] - BG + 0.107	V
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 1.3V)	P2[4] - P2[6] - 0.057	P2[4] - P2[6] + 0.026	P2[4] - P2[6] + 0.110	V

Table 15. 3.3V DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
BG	Bandgap Voltage Reference	1.28	1.30	1.32	V
–	AGND = Vdd/2[7]	Vdd/2 - 0.03	Vdd/2 - 0.01	Vdd/2 + 0.005	V
–	AGND = 2 x BandGap[7]	Not Allowed			
–	AGND = P2[4] (P2[4] = Vdd/2)	P2[4] - 0.008	P2[4] + 0.001	P2[4] + 0.009	V
–	AGND = BandGap[7]	BG - 0.009	BG + 0.005	BG + 0.015	V
–	AGND = 1.6 x BandGap[7]	1.6 x BG - 0.027	1.6 x BG - 0.010	1.6 x BG + 0.018	V
–	AGND Column to Column Variation (AGND = Vdd/2)[7]	-0.034	0.000	0.034	V
–	RefHi = Vdd/2 + BandGap	Not Allowed			
–	RefHi = 3 x BandGap	Not Allowed			
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] + P2[6] - 0.075	P2[4] + P2[6] - 0.009	P2[4] + P2[6] + 0.057	V
–	RefHi = 3.2 x BandGap	Not Allowed			
–	RefLo = Vdd/2 - BandGap	Not Allowed			
–	RefLo = BandGap	Not Allowed			
–	RefLo = 2 x BandGap - P2[6] (P2[6] = 0.5V)	Not Allowed			
–	RefLo = P2[4] – BandGap (P2[4] = Vdd/2)	Not Allowed			
–	RefLo = P2[4]-P2[6] (P2[4] = Vdd/2, P2[6] = 0.5V)	P2[4] - P2[6] - 0.048	P2[4]- P2[6] + 0.022	P2[4] - P2[6] + 0.092	V

DC Analog PSoC Block Specifications

Table 16 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 16. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.2	–	kΩ	
C_{SC}	Capacitor Unit Value (Switched Capacitor)	–	80	–	fF	

DC POR and LVD Specifications

Table 17 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V or 3.3V at 25°C. These are for design guidance only.

Note The bits PORLEV and VM in the table below refer to bits in the VLT_CR register.

Table 17. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	Vdd Value for PPOR Trip (positive ramp)					
V_{PPOR0R}	PORLEV[1:0] = 00b		2.91		V	
V_{PPOR1R}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2R}	PORLEV[1:0] = 10b		4.55		V	
	Vdd Value for PPOR Trip (negative ramp)					
V_{PPOR0}	PORLEV[1:0] = 00b		2.82		V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	4.39	–	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55		V	
	PPOR Hysteresis					
V_{PH0}	PORLEV[1:0] = 00b	–	92	–	mV	
V_{PH1}	PORLEV[1:0] = 01b	–	0	–	mV	
V_{PH2}	PORLEV[1:0] = 10b	–	0	–	mV	
	Vdd Value for LVD Trip					
V_{LVD0}	VM[2:0] = 000b	2.86	2.92	2.98[8]	V	
V_{LVD1}	VM[2:0] = 001b	2.96	3.02	3.08	V	
V_{LVD2}	VM[2:0] = 010b	3.07	3.13	3.20	V	
V_{LVD3}	VM[2:0] = 011b	3.92	4.00	4.08	V	
V_{LVD4}	VM[2:0] = 100b	4.39	4.48	4.57	V	
V_{LVD5}	VM[2:0] = 101b	4.55	4.64	4.74[9]	V	
V_{LVD6}	VM[2:0] = 110b	4.63	4.73	4.82	V	
V_{LVD7}	VM[2:0] = 111b	4.72	4.81	4.91	V	

Notes
8. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
9. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.

DC Programming Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C and are for design guidance only.

Table 18. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
I_{DDP}	Supply Current During Programming or Verify	–	15	30	mA	
V_{ILP}	Input Low Voltage During Programming or Verify	–	–	0.8	V	
V_{IHP}	Input High Voltage During Programming or Verify	2.1	–	–	V	
I_{ILP}	Input Current when Applying Vilp to P1[0] or P1[1] During Programming or Verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input Current when Applying Vihp to P1[0] or P1[1] During Programming or Verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output Low Voltage During Programming or Verify	–	–	Vss + 0.75	V	
V_{OHV}	Output High Voltage During Programming or Verify	Vdd - 1.0	–	Vdd	V	
$Flash_{ENPB}$	Flash Endurance (per block)	1000	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash Endurance (total)[10]	36,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash Data Retention	10	–	–	Years	

Note

10. A maximum of 36 x 1000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 1000 maximum cycles each, 36x2 blocks of 500 maximum cycles each, or 36x4 blocks of 250 maximum cycles each (to limit the total number of cycles to 36x1000 and that no single block ever sees more than 1000 cycles).
For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.

AC Electrical Characteristics

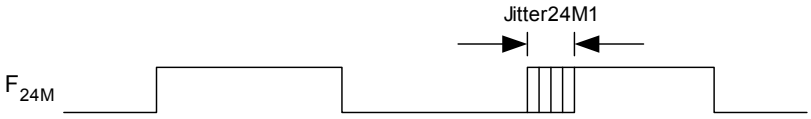
AC Chip Level Specifications

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 19. AC Chip Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{IMO245V}$	Internal Main Oscillator Frequency for 24 MHz (5V)	23.04	24	24.96[11,12]	MHz	Trimmed for 5V operation using factory trim values.
$F_{IMO243V}$	Internal Main Oscillator Frequency for 24 MHz (3.3V)	22.08	24	25.92[12,13]	MHz	Trimmed for 3.3V operation using factory trim values.
F_{CPU1}	CPU Frequency (5V Nominal)	0.93	24	24.96[11,12]	MHz	
F_{CPU2}	CPU Frequency (3.3V Nominal)	0.93	12	12.96[12,13]	MHz	
F_{BLK5}	Digital PSoC Block Frequency (5V Nominal)	0	48	49.92[11,12,14]	MHz	Refer to the AC Digital Block Specifications.
F_{BLK3}	Digital PSoC Block Frequency (3.3V Nominal)	0	24	25.92[12, 14]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	Trimmed. During power up, ILO is untrimmed and minimum is 5 kHz
Jitter32k	32 kHz Period Jitter	–	100		ns	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Fout48M	48 MHz Output Frequency	46.08	48.0	49.92[11,13]	MHz	Trimmed. Utilizing factory trim values.
Jitter24M1	24 MHz Period Jitter (IMO) Peak-to-Peak	–	300		ps	
F_{MAX}	Maximum Frequency of signal on row input or row output.	–	–	12.96	MHz	
T_{RAMP}	Supply Ramp Time	20	–	–	µs	

Figure 5. 24 MHz Period Jitter (IMO) Timing Diagram



Notes
11. 4.75V < Vdd < 5.25V.
12. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
13. 3.0V < Vdd < 3.6V. See Application Note AN2012 “Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation” for information on trimming for operation at 3.3V.
14. See the individual user module data sheets for information on maximum frequencies for user modules.

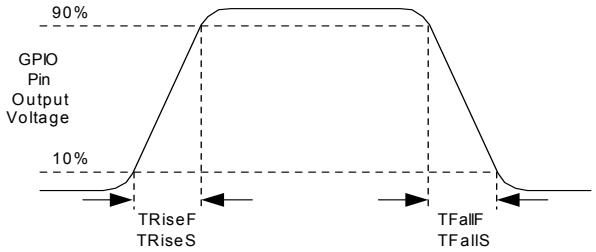
AC General Purpose IO Specifications

Table 20 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 20. AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO Operating Frequency	0	–	12	MHz	Normal Strong Mode
TRiseF	Rise Time, Normal Strong Mode, Cload = 50 pF	3	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TFallF	Fall Time, Normal Strong Mode, Cload = 50 pF	2	–	18	ns	Vdd = 4.5 to 5.25V, 10% - 90%
TRiseS	Rise Time, Slow Strong Mode, Cload = 50 pF	10	27	–	ns	Vdd = 3 to 5.25V, 10% - 90%
TFallS	Fall Time, Slow Strong Mode, Cload = 50 pF	10	22	–	ns	Vdd = 3 to 5.25V, 10% - 90%

Figure 6. GPIO Timing Diagram



AC Operational Amplifier Specifications

Table 21 and Table 22 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Power = High and Opamp Bias = High is not supported at 3.3V.

Table 21. 5V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 3.9 0.72 0.62	 µs µs µs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 – – –	 – – –	 5.9 0.92 0.72	 µs µs µs
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.15 1.7 6.5	 – – –	 – – –	 V/µs V/µs V/µs
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.01 0.5 4.0	 – – –	 – – –	 V/µs V/µs V/µs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High Power = High, Opamp Bias = High	 0.75 3.1 5.4	 – – –	 – – –	 MHz MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

Table 22. 3.3V AC Operational Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROA}	Rising Settling Time from 80% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 3.92 0.72	 µs µs
T_{SOA}	Falling Settling Time from 20% of ΔV to 0.1% of ΔV (10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 – –	 – –	 5.41 0.72	 µs µs
SR_{ROA}	Rising Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.31 2.7	 – –	 – –	 V/µs V/µs
SR_{FOA}	Falling Slew Rate (20% to 80%)(10 pF load, Unity Gain) Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.24 1.8	 – –	 – –	 V/µs V/µs
BW_{OA}	Gain Bandwidth Product Power = Low, Opamp Bias = Low Power = Medium, Opamp Bias = High	 0.67 2.8	 – –	 – –	 MHz MHz
E_{NOA}	Noise at 1 kHz (Power = Medium, Opamp Bias = High)	–	100	–	nV/rt-Hz

AC Low Power Comparator Specifications

Table 23 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, or 2.4V to 3.0V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V at 25°C. These are for design guidance only.

Table 23. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC Response Time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

AC Digital Block Specifications

Table 24 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 24. AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
Timer	Capture Pulse Width	50[15]	–	–	ns	
	Maximum Frequency, No Capture	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, With Capture	–	–	25.92	MHz	
Counter	Enable Pulse Width	50[15]	–	–	ns	
	Maximum Frequency, No Enable Input	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
	Maximum Frequency, Enable Input	–	–	25.92	MHz	
Dead Band	Kill Pulse Width:					
	Asynchronous Restart Mode	20	–	–	ns	
	Synchronous Restart Mode	50[15]	–	–	ns	
	Disable Mode	50[15]	–	–	ns	
	Maximum Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (PRS Mode)	Maximum Input Clock Frequency	–	–	49.92	MHz	4.75V < Vdd < 5.25V.
CRCPRS (CRC Mode)	Maximum Input Clock Frequency	–	–	24.6	MHz	
SPIM	Maximum Input Clock Frequency	–	–	8.2	MHz	Maximum data rate at 4.1 MHz due to 2 x over clocking.
SPIS	Maximum Input Clock Frequency	–	–	4.1	MHz	
	Width of SS_ Negated Between Transmissions	50[15]	–	–	ns	
Transmitter	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.
Receiver	Maximum Input Clock Frequency	–	–	24.6	MHz	Maximum data rate at 3.08 MHz due to 8 x over clocking.

Note
15. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC External Clock Specifications

Table 25 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 25. AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units
F_{OSCEXT}	Frequency	0	–	24.24	MHz
–	High Period	20.6	–	–	ns
–	Low Period	20.6	–	–	ns
–	Power up to IMO Switch	150	–	–	µs

AC Analog Output Buffer Specifications

Table 26 and Table 27 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 26. 5V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	 – –	 – –	 2.5 2.5	 µs µs
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	 – –	 – –	 2.2 2.2	 µs µs
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/µs V/µs
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load Power = Low Power = High	 0.65 0.65	 – –	 – –	 V/µs V/µs
BW_{OBSS}	Small Signal Bandwidth, 20mV_{pp}, 3dB BW, 100pF Load Power = Low Power = High	 0.8 0.8	 – –	 – –	 MHz MHz
BW_{OBLS}	Large Signal Bandwidth, 1V_{pp}, 3dB BW, 100pF Load Power = Low Power = High	 300 300	 – –	 – –	 kHz kHz

Table 27. 3.3V AC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{ROB}	Rising Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	 – –	 – –	 3.8 3.8	 µs µs	
T_{SOB}	Falling Settling Time to 0.1%, 1V Step, 100pF Load Power = Low Power = High	 – –	 – –	 2.6 2.6	 µs µs	
SR_{ROB}	Rising Slew Rate (20% to 80%), 1V Step, 100pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs	
SR_{FOB}	Falling Slew Rate (80% to 20%), 1V Step, 100pF Load Power = Low Power = High	 0.5 0.5	 – –	 – –	 V/µs V/µs	
BW_{OBSS}	Small Signal Bandwidth, 20mV$_{pp}$, 3dB BW, 100pF Load Power = Low Power = High	 0.7 0.7	 – –	 – –	 MHz MHz	
BW_{OBLS}	Large Signal Bandwidth, 1V$_{pp}$, 3dB BW, 100pF Load Power = Low Power = High	 200 200	 – –	 – –	 kHz kHz	

AC Programming Specifications

Table 28 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 28. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise Time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall Time of SCLK	1	–	20	ns	
T_{SSCLK}	Data Setup Time to Falling Edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data Hold Time from Falling Edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash Erase Time (Block)	–	10	–	ms	
T_{WRITE}	Flash Block Write Time	–	30	–	ms	
T_{DSCLK}	Data Out Delay from Falling Edge of SCLK	–	–	45	ns	Vdd > 3.6
T_{DSCLK3}	Data Out Delay from Falling Edge of SCLK	–	–	50	ns	3.0 ≤ Vdd ≤ 3.6

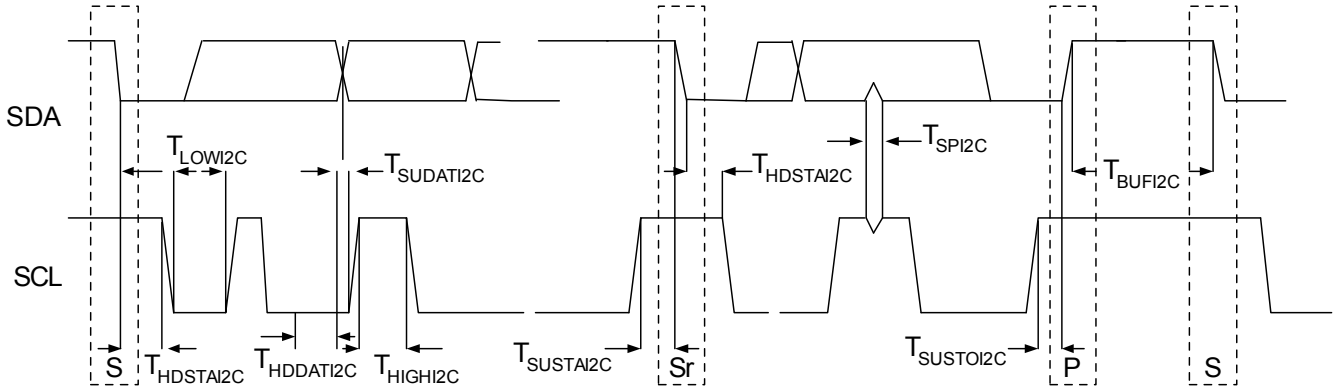
AC I²C Specifications

Table 29 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75V to 5.25V and -40°C ≤ T_A ≤ 85°C, or 3.0V to 3.6V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters apply to 5V and 3.3V at 25°C. These are for design guidance only.

Table 29. AC Characteristics of the I2C SDA and SCL Pins for Vdd

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold Time (Repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Setup Time	250	–	100[16]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of Spikes are Suppressed by the Input Filter.	–	–	0	50	ns	

Figure 7. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

16. A fast-mode I2C-bus device is used in a standard mode I2C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the standard-mode I2C-bus specification) before the SCL line is released.

Package Dimensions

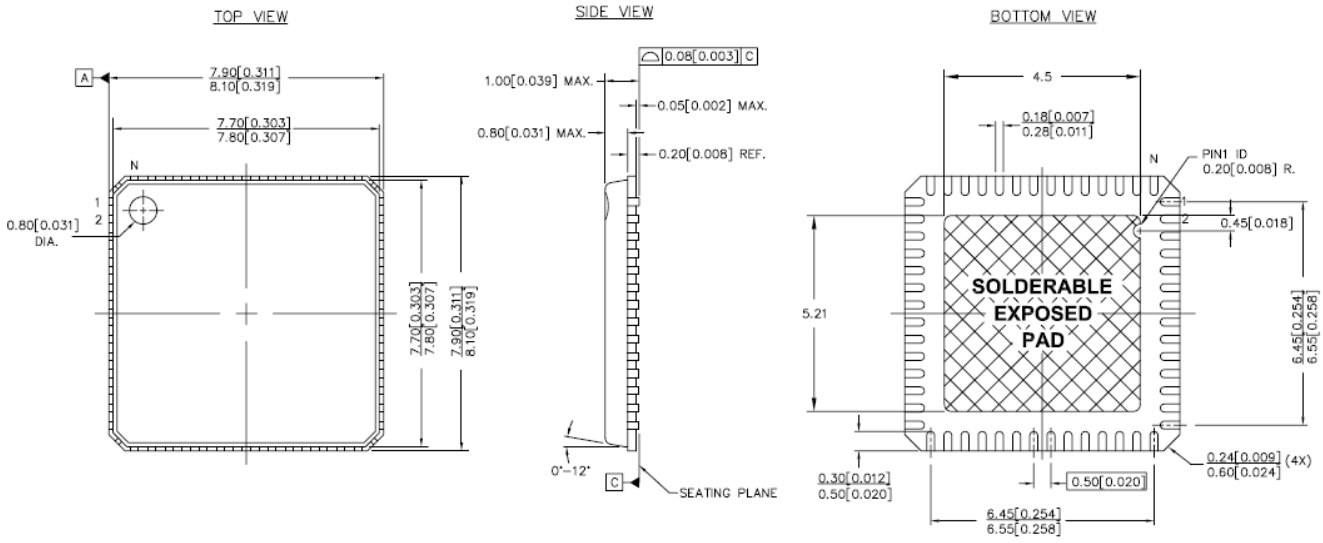
This section illustrates the package specification for the CY8CTMA120 TrueTouch devices along with the thermal impedance for the package and solder reflow peak temperatures.

It is important to note that emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at http://www.cypress.com/design/MR10161.

For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.

Note Pinned vias for thermal conduction are not required for the low power PSoC device.

Figure 8. 56-Pin (8x8 mm) QFN



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.162g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF56A	STANDARD
LY56A	PB-FREE

001-12921 **

Table 30. Thermal Impedance for the Package

Package	Typical θ_{JA} [17]
56 QFN[18]	12.93 °C/W

Table 31. Solder Reflow Peak Temperature

Package	Minimum Peak Temperature[19]	Maximum Peak Temperature
56 QFN	240°C	260°C

Notes

17. $T_J = T_A$ + Power x θ_{JA}.
18. To achieve the thermal impedance specified for the ** package, the center thermal pad is soldered to the PCB ground plane.
19. Higher temperatures is required based on the solder melting point. Typical temperatures for solder are 220 ± 5oC with Sn-Pb or 245 ± 5oC with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications

Development Tool Selection

This section presents the development tools available for all current PSoC device families including CY8CTMA120 family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Used by thousands of PSoC developers, this software has been facilitating PSoC designs for the last five years. PSoC Designer is available free of charge at http://www.cypress.com under Design Resources >> Software and Drivers.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works as a standalone programming application and can operate directly from PSoC Designer or PSoC Express. PSoC Programmer software is compatible both with PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

Development Kits

All development kits can be purchased by contacting tsbusdev@cypress.com.

CY3290-TMA120

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3216 Modular Programmer

The CY3216 Modular Programmer kit features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- 3 Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production-programming environment.

Note: CY3207ISSP needs special software and is not compatible with PSoC Programmer.

The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Build a PSoC Emulator into your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note “Debugging - Build a PSoC Emulator into Your Board - AN2323” at http://www.cypress.com/AN2323.

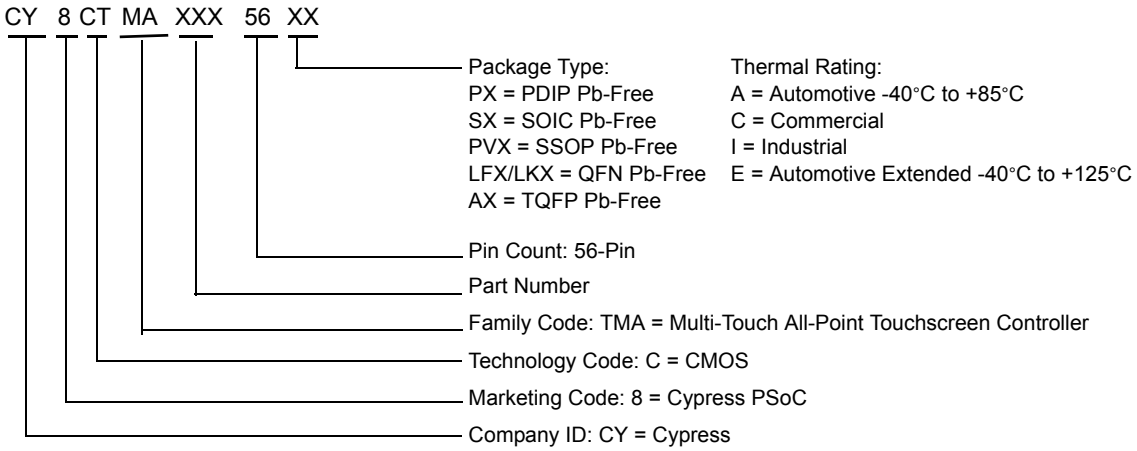
Specific details for each of these tools is found at

http://www.cypress.com under Design Resources > Evaluation Boards.

Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Temperature Range	Single-Touch Enabled	Multi-Touch Gesture Enabled	Multi-Touch All-Point Enabled	X/Y Sensor Inputs
56-Pin (8x8 mm) QFN	CY8CTMA120-56LFXA	16K	1K	-40C to +85C	Y	Y	Y	Up to 37
56-Pin (8x8 mm) QFN (Tape and Reel)	CY8CTMA120-56LFXAT	16K	1K	-40C to +85C	Y	Y	Y	Up to 37

Ordering Code Definitions



Document History Page

Document Title: CY8CTMA120 Automotive TrueTouch™ Multi-Touch All-Point Touchscreen Controller Document Number: 001-53860				
Revision	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2732561	MASJ/AESA	06/09/2009	New data sheet

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at cypress.com/sales.

Products

PSoC	psoc.cypress.com
Clocks & Buffers	clocks.cypress.com
Wireless	wireless.cypress.com
Memories	memory.cypress.com
Image Sensors	image.cypress.com