

### 25-Bit Configurable Registered Buffer for DDR2

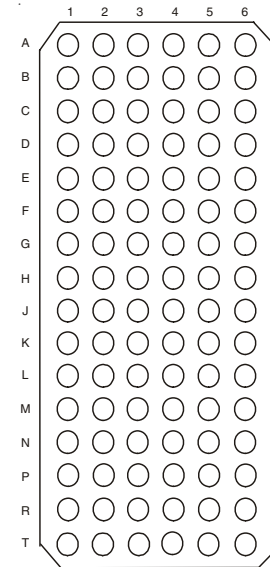
#### Recommended Application:

- DDR2 Memory Modules
- Provides complete DDR DIMM solution with ICS97ULP877, 98ULPA877A
- Ideal for DDR2 400,533, and 667

#### Product Features:

- 25-bit 1:1 or 14-bit 1:2 configurable registered buffer with parity check functionality
- Supports SSTL\_18 JEDEC specification on data inputs and outputs
- Supports LVCMOS switching levels on  $\overline{\text{CSR}}$  and  $\overline{\text{RESET}}$  inputs
- Low voltage operation  
 $V_{DD} = 1.7V$  to  $1.9V$
- Available in 96 BGA package
- Drop-in replacement for ICSSSTUA32864
- Green packages available

#### Pin Configuration



**96 Ball BGA  
(Top View)**

#### Functionality Truth Table

Inputs						Outputs,			
$\overline{\text{RST}}$	$\overline{\text{DCS}}$	$\overline{\text{CSR}}$	CK	$\overline{\text{CK}}$	Dn, DODT, DCKE	Qn	$\overline{\text{QCS}}$	QODT, QCKE	
H	L	L	↑	↓	L	L	L	L	
H	L	L	↑	↓	H	H	L	H	
H	L	L	L or H	L or H	X	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	
H	L	H	↑	↓	L	L	L	L	
H	L	H	↑	↓	H	H	L	H	
H	L	H	L or H	L or H	X	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	
H	H	L	↑	↓	L	L	H	L	
H	H	L	↑	↓	H	H	H	H	
H	H	L	L or H	L or H	X	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	
H	H	H	↑	↓	L	Q <sub>0</sub>	H	L	
H	H	H	↑	↓	H	Q <sub>0</sub>	H	H	
H	H	H	L or H	L or H	X	Q <sub>0</sub>	Q <sub>0</sub>	Q <sub>0</sub>	
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	L	L	

# Ball Assignments

## 25 bit 1:1 Register

A	DCKE	PPO	VREF	VDD	QCKE	NC
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	VDD	VDD	Q3	Q16
D	DODT	$\overline{QERR}$	GND	GND	QODT	NC
E	D5	D17	VDD	VDD	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	PAR_IN	$\overline{RST}$	VDD	VDD	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCS}$	NC
J	$\overline{CK}$	$\overline{CSR}$	VDD	VDD	ZOH	ZOL
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	VDD	VDD	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	VDD	VDD	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	VDD	VDD	Q13	Q24
T	D14	D25	VREF	VDD	Q14	Q25
	1	2	3	4	5	6

**C0 = 0, C1 = 0**

## 14 bit 1:2 Registers

A	DCKE	PPO	VREF	VDD	QCKEA	QCKEB
B	D2	NC	GND	GND	Q2A	Q2B
C	D3	NC	VDD	VDD	Q3A	Q3B
D	DODT	$\overline{QERR}$	GND	GND	QODTA	QODTB
E	D5	NC	VDD	VDD	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RST}$	VDD	VDD	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCSA}$	$\overline{QCSB}$
J	$\overline{CK}$	$\overline{CSR}$	VDD	VDD	ZOH	ZOL
K	D8	NC	GND	GND	Q8A	Q8B
L	D9	NC	VDD	VDD	Q9A	Q9B
M	D10	NC	GND	GND	Q10A	Q10B
N	D11	NC	VDD	VDD	Q11A	Q11B
P	D12	NC	GND	GND	Q12A	Q12B
R	D13	NC	VDD	VDD	Q13A	Q13B
T	D14	NC	VREF	VDD	Q14A	Q14B
	1	2	3	4	5	6

**Register A (C0 = 0, C1 = 1)**

A	D1	PPO	VREF	VDD	Q1A	Q1B
B	D2	NC	GND	GND	Q2A	Q2B
C	D3	NC	VDD	VDD	Q3A	Q3B
D	D4	$\overline{QERR}$	GND	GND	Q4A	Q4B
E	D5	NC	VDD	VDD	Q5A	Q5B
F	D6	NC	GND	GND	Q6A	Q6B
G	PAR_IN	$\overline{RST}$	VDD	VDD	C1	C0
H	CK	$\overline{DCS}$	GND	GND	$\overline{QCSA}$	$\overline{QCSB}$
J	$\overline{CK}$	$\overline{CSR}$	VDD	VDD	ZOH	ZOL
K	D8	NC	GND	GND	Q8A	Q8B
L	D9	NC	VDD	VDD	Q9A	Q9B
M	D10	NC	GND	GND	Q10A	Q10B
N	DODT	NC	VDD	VDD	QODTA	QODTB
P	D12	NC	GND	GND	Q12A	Q12B
R	D13	NC	VDD	VDD	Q13A	Q13B
T	DCKE	NC	VREF	VDD	QCKEA	QCKEB
	1	2	3	4	5	6

**Register B (C0 = 1, C1 = 1)**

## General Description

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V VDD operation.

All clock and data inputs are compatible with the JEDEC standard for SSTL\_18. The control inputs are LVCMOS. All outputs are 1.8-V CMOS drivers that have been optimized to drive the DDR-II DIMM load. **ICSSSTUB32866B** operates from a differential clock (CK and  $\overline{CK}$ ). Data are registered at the crossing of CK going high, and  $\overline{CK}$  going low.

The C0 input controls the pinout configuration of the 1:2 pinout from A configuration (when low) to B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high).

### A - Pair Configuration (CO<sub>1</sub> = 0, CI<sub>1</sub> = 1 and CO<sub>2</sub> = 0, CI<sub>2</sub> = 1)

Parity that arrives one cycle after the data input to which it applies is checked on the PAR\_IN of the first register. The second register produces PPO and QERR signals. The QERR of the first register is left floating. The valid error information is latched on the QERR output of the second register. If an error occurs QERR is latched low for two cycles or until Reset is low.

### B - Single Configuration (CO = 0, C1 = 0)

The device supports low-power standby operation. When the reset input ( $\overline{RST}$ ) is low, the differential input receivers are disabled, and undriven (floating) data, clock and reference voltage (VREF) inputs are allowed. In addition, when  $\overline{RST}$  is low all registers are reset, and all outputs are forced low. The LVCMOS  $\overline{RST}$  and Cn inputs must always be held at a valid logic high or low level. To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{RST}$  must be held in the low state during power up.

In the DDR-II RDIMM application,  $\overline{RST}$  is specified to be completely asynchronous with respect to CK and  $\overline{CK}$ . Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of  $\overline{RST}$  until the input receivers are fully enabled, the design of the **ICSSSTUB32866B** must ensure that the outputs will remain low, thus ensuring no glitches on the output.

The device monitors both  $\overline{DCS}$  and  $\overline{CSR}$  inputs and will gate the Qn outputs from changing states when both  $\overline{DCS}$  and  $\overline{CSR}$  inputs are high. If either  $\overline{DCS}$  or  $\overline{CSR}$  input is low, the Qn outputs will function normally. The  $\overline{RST}$  input has priority over the  $\overline{DCS}$  and  $\overline{CSR}$  control and will force the outputs low. If the  $\overline{DCS}$ -control functionality is not desired, then the  $\overline{CSR}$  input can be hardwired to ground, in which case, the setup-time requirement for  $\overline{DCS}$  would be the same as for the other D data inputs. Package options include 96-ball LFBGA (MO-205CC).

### Parity and Standby Functionality Truth Table

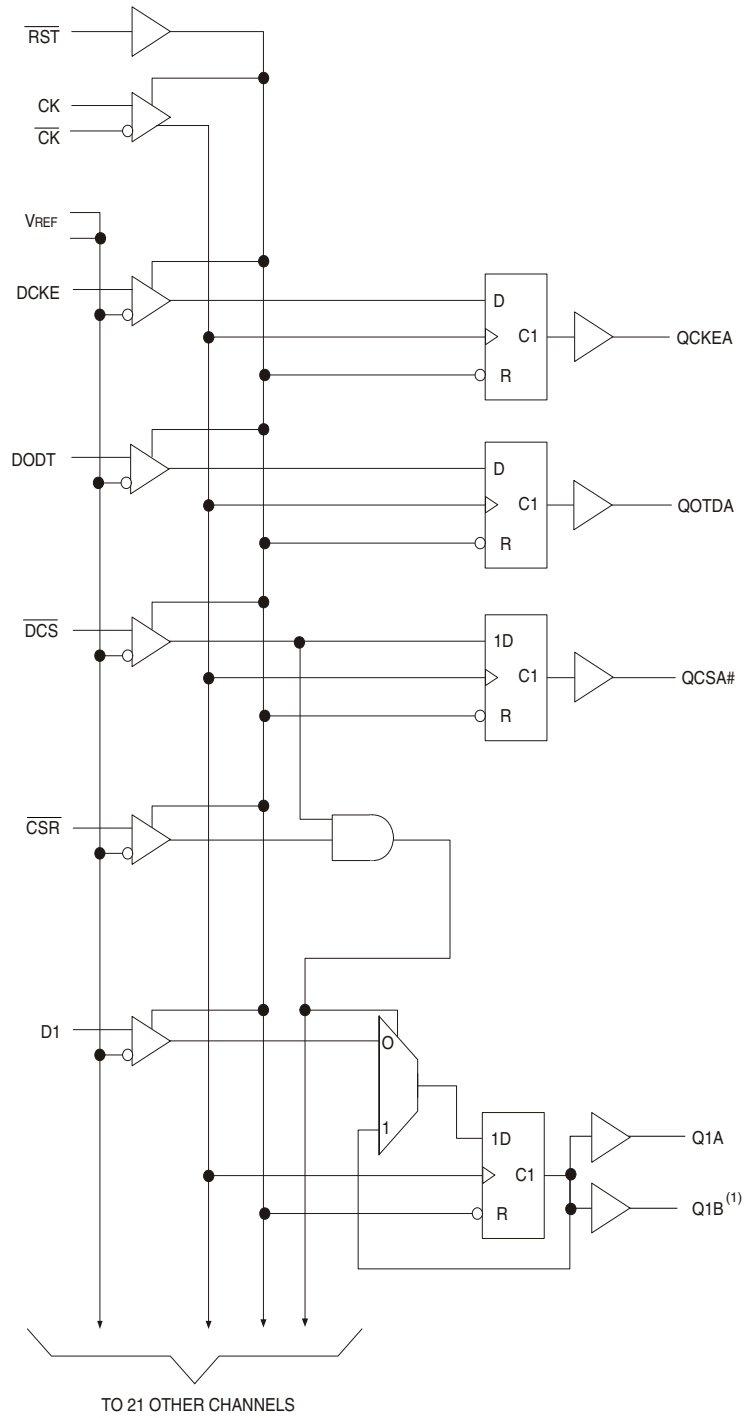
Inputs							Outputs	
Rst	DCS	CSR	CK	$\overline{CK}$	Sum of Inputs = H (D1 - D25)	PAR_IN	PPO	QERR
H	L	X	↑	↓	Even	L	L	H
H	L	X	↑	↓	Odd	L	H	L
H	L	X	↑	↓	Even	H	H	L
H	L	X	↑	↓	Odd	H	L	H
H	H	L	↑	↓	Even	L	L	H
H	H	L	↑	↓	Odd	H	H	L
H	H	H	↑	↓	X	X	PPO <sub>0</sub>	QERR <sub>0</sub>
H	X	X	L or H	L or H	X	X	PPO <sub>0</sub>	QERR <sub>0</sub>
L	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	X or Floating	L	H

- CO = 0 and CI = 0, Data inputs are D2, D3, D5, D6, D8 - D25.  
CO = 0 and CI = 1, Data inputs are D2, D3, D5, D6, D8 - D14  
CO = 1 and CI = 1, Data inputs are D1 - D6, D8 - D10, D12, D13
- PAR\_IN arrives one clock cycle after the data to which it applies when CO = 0.
- PAR\_IN arrives two clock cycles after the data to which it applies when CO = 1.
- Assume QERR is high at the CK↑ and  $\overline{CK}$ ↓ crossing. If QERR is low it stays latched low for two clock cycles on until Rst is low.

## Ball Assignment

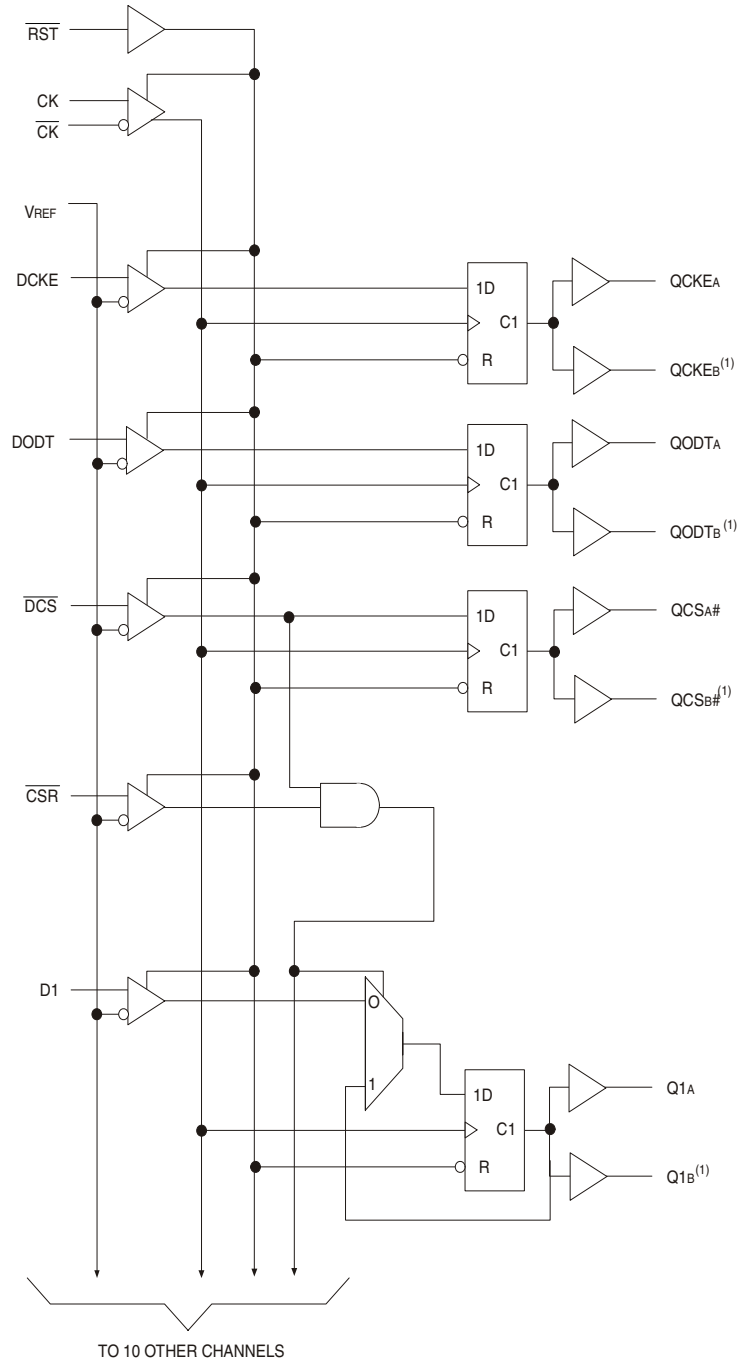
Terminal Name	Description	Electrical Characteristics
GND	Ground	Ground input
V <sub>DD</sub>	Power supply voltage	1.8V nominal
V <sub>REF</sub>	Input reference voltage	0.9V nominal
Z <sub>OH</sub>	Reserved for future use	Input
Z <sub>OL</sub>	Reserved for future use	Input
CK	Positive master clock input	Differential input
$\overline{CK}$	Negative master clock input	Differential input
C0, C1	Configuration control inputs	LVC MOS inputs
$\overline{RST}$	Asynchronous reset input - resets registers and disables V <sub>REF</sub> data and clock differential-input receivers	LVC MOS input
$\overline{CSR}$ , $\overline{DCS}$	Chip select inputs - disables D1 - D24 outputs switching when both inputs are high	SSTL <sub>18</sub> input
D1 - D25	Data input - clock in on the crossing of the rising edge of CK and the falling edge of $\overline{CK}$	SSTL <sub>18</sub> input
DODT	The outputs of this register bit will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	SSTL <sub>18</sub> input
DCKE	The outputs of this register bit will now be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	SSTL <sub>18</sub> input
Q1 - Q25	Data outputs that are suspended by the DCS and CSR control	1.8V CMOS
$\overline{QCS}$	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8V CMOS
QODT	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8V CMOS
QCKE	Data output that will not be suspended by the $\overline{DCS}$ and $\overline{CSR}$ control	1.8V CMOS
PPO	Partial parity out indicates off parity of inputs D1 - D25.	1.8V CMOS
PAR_IN	Parity input arrives one clock cycle after the corresponding data input	SSTL <sub>18</sub> input
$\overline{QERR}$	Output error bit-generated one clock cycle after the corresponding data output	Open drain output

Block Diagram for 1:1 mode (positive logic)



NOTE:  
1. Disabled in 1:1 configuration.

Block Diagram for 1:2 mode (positive logic)



NOTE:  
1. Disabled in 1:1 configuration.

2. Device standard (cont'd)

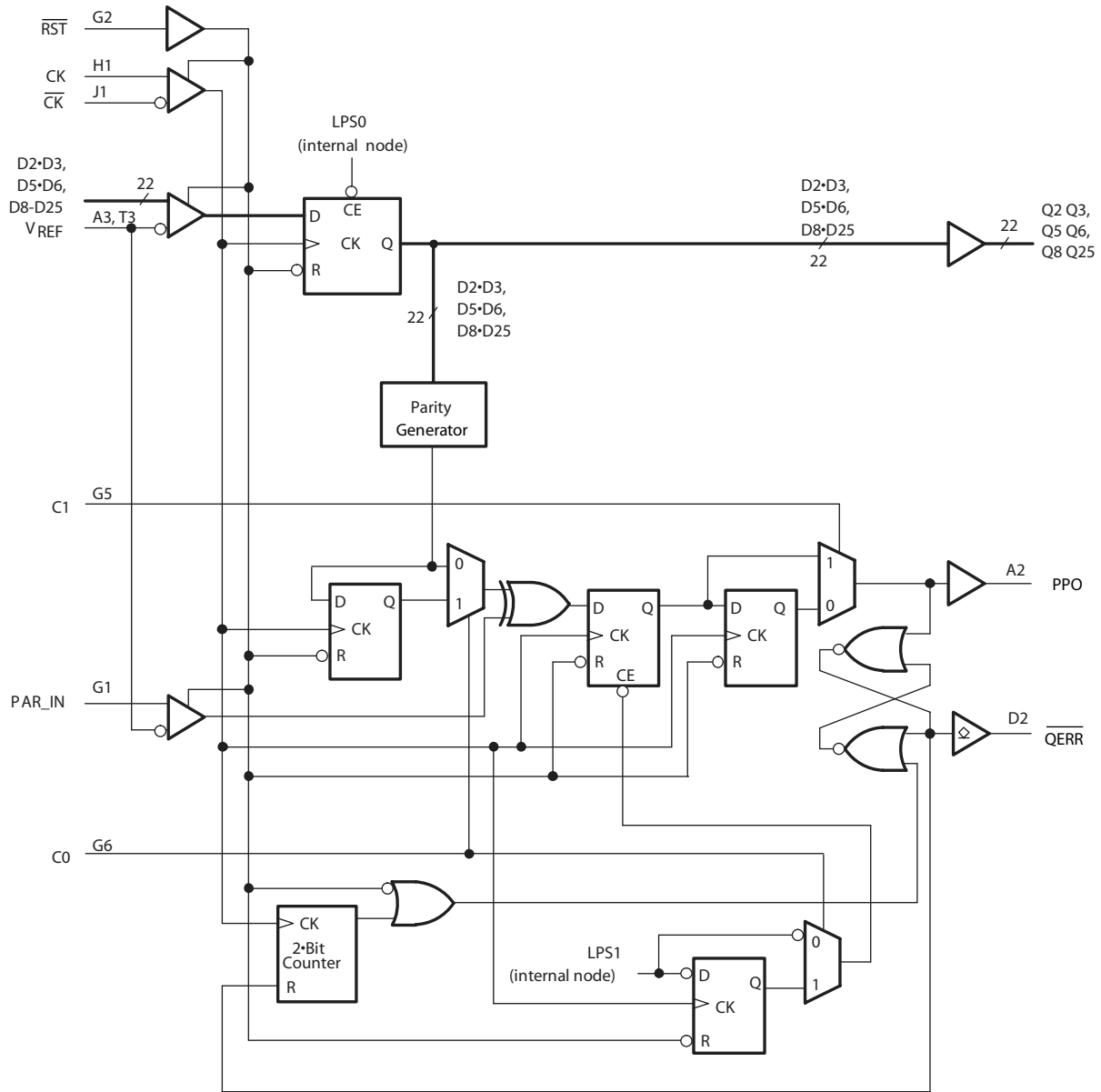


Figure 6 — Parity logic diagram for 1:1 register configuration (positive logic): C0=0, C1=0

2. Device standard (cont'd)

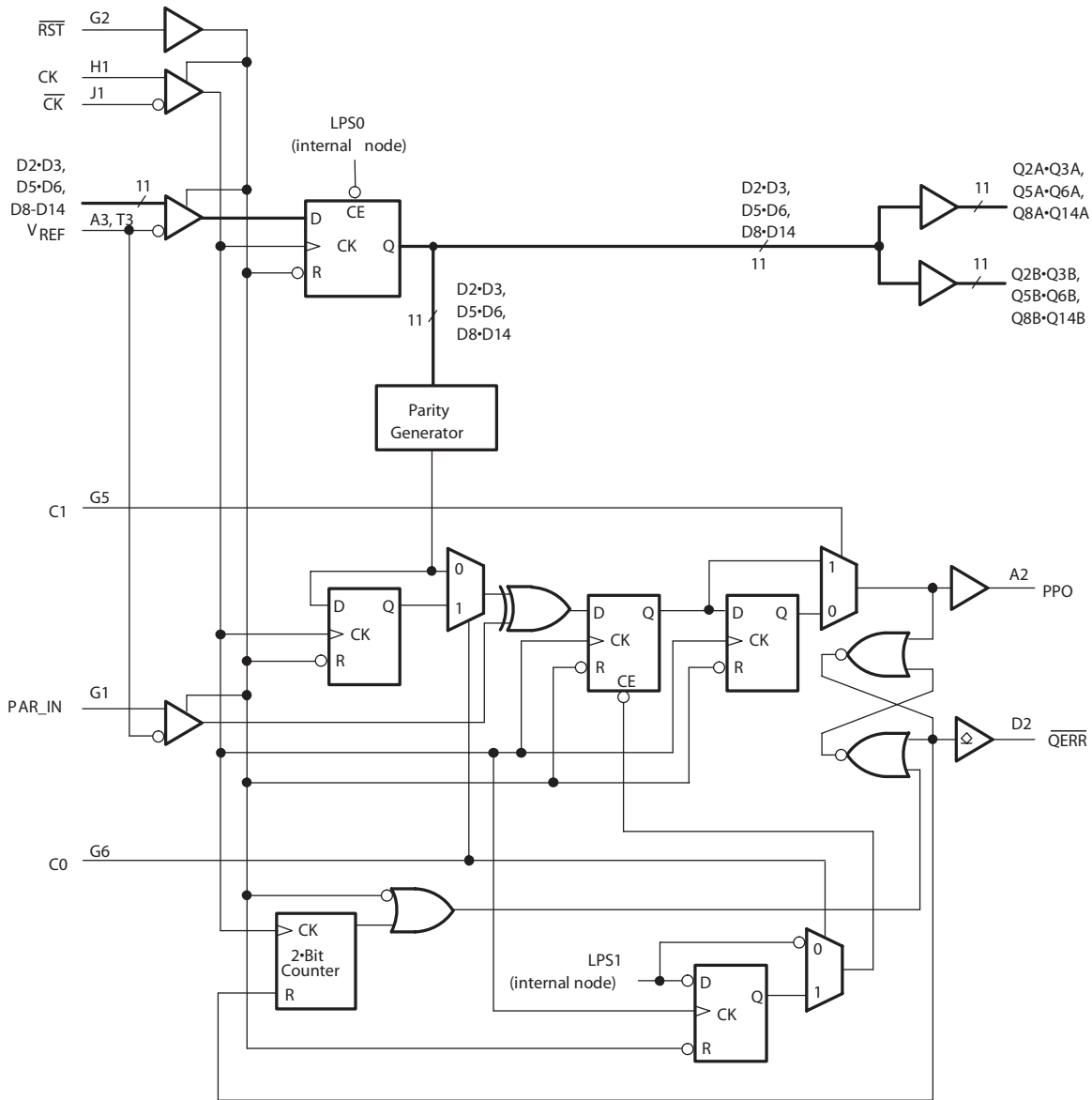


Figure 7 — Parity logic diagram for 1:2 register-A configuration (positive logic); C0=0, C1=1



2. Device standard (cont'd)

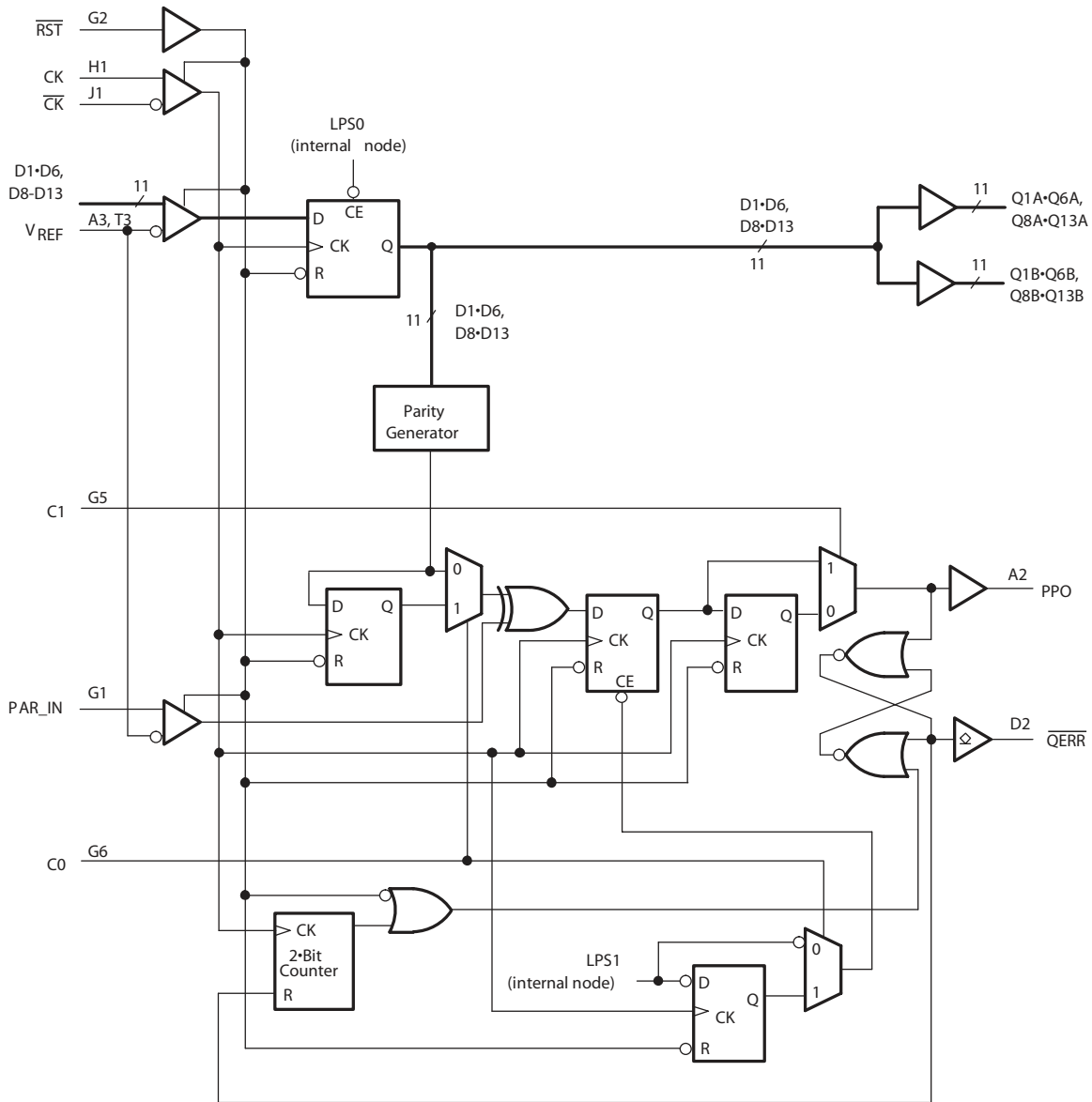


Figure 8 — Parity logic diagram for 1:2 register-B configuration (positive logic); CO=1, C1=1

2. Device standard (cont'd)

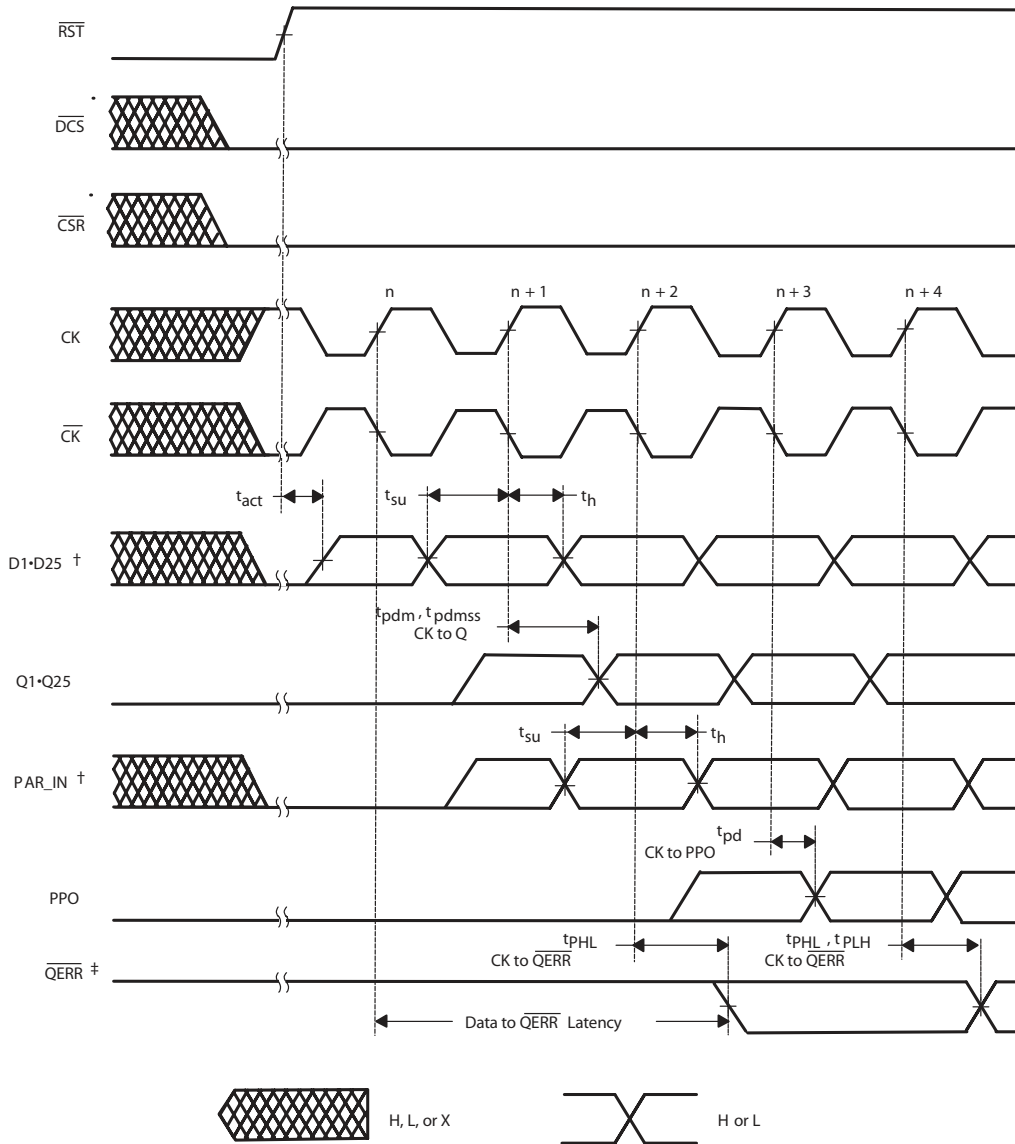
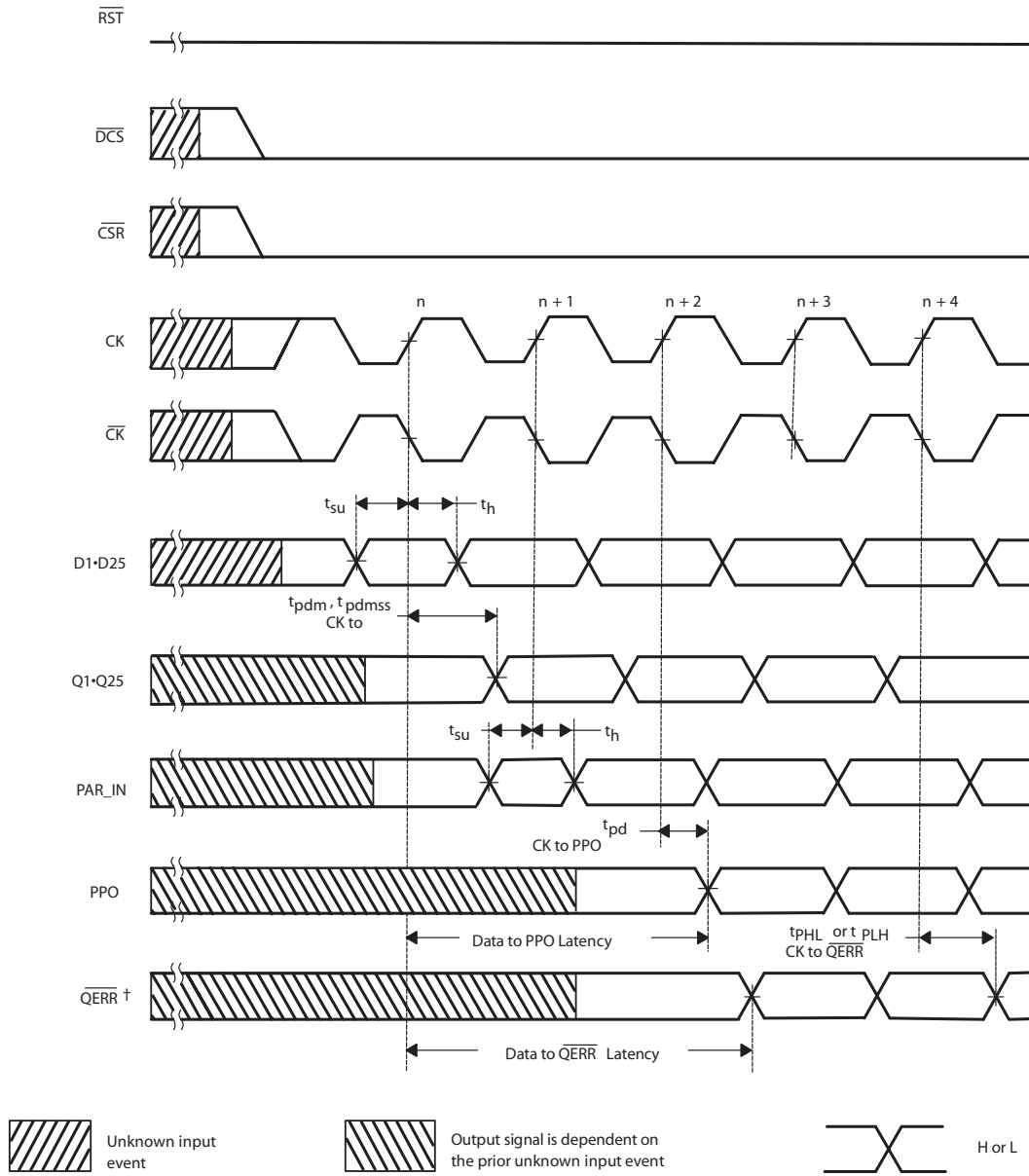


Figure 9 — Timing diagram for SSTU32866 used as a single device; C0=0, C1=0;  $\overline{RST}$  Switches from L to H

† After  $\overline{RST}$  is switched from low to high, all data and PAR\_IN inputs signals must be set and held low for a minimum time of  $t_{ACT}$  max, to avoid false error.

‡ If the data is clocked in on the n clock pulse, the  $\overline{QERR}$  output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse.

2. Device standard (cont'd)



**Figure 10 — Timing diagram for SSTU32866 used as a single device; C0=0, C1=0;  $\overline{RST}$  being held high**

<sup>†</sup> If the data is clocked in on the n clock pulse, the  $\overline{QERR}$  output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse. If an error occurs and the  $\overline{QERR}$  output is driven low, it stays latched low for a minimum of two clock cycles or until  $\overline{RST}$  is driven low.

2. Device standard (cont'd)

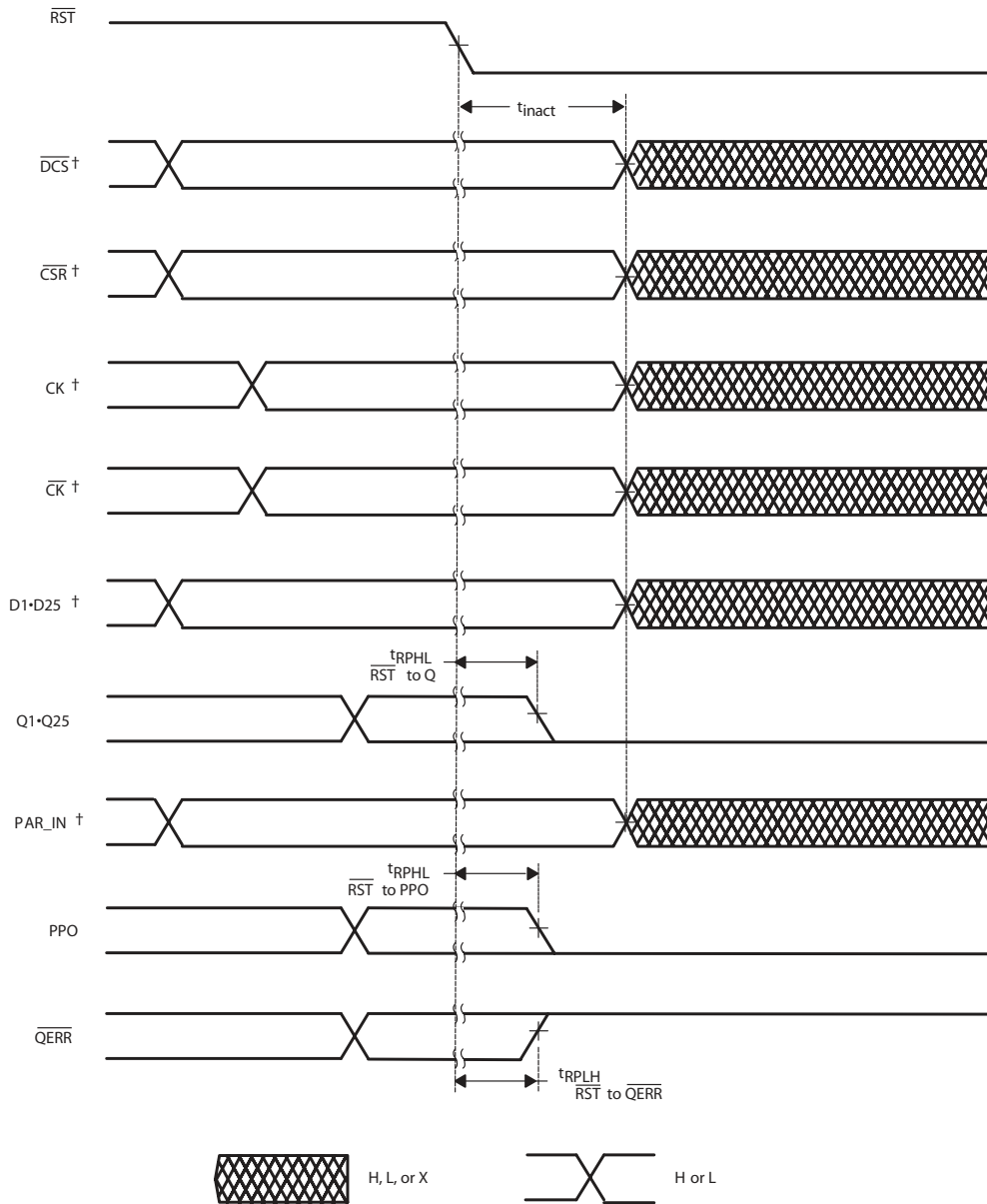


Figure 11 — Timing diagram for SSTU32866 used as a single device; C0=0, C1=0;  $\overline{\text{RST}}$  switches from H to L

† After  $\overline{\text{RST}}$  is switched from high to low, all data and clock unouts signals must be set and held at valid logic levels (not floating) for a minimum time of  $t_{\text{INACT max}}$ .

2. Device standard (cont'd)

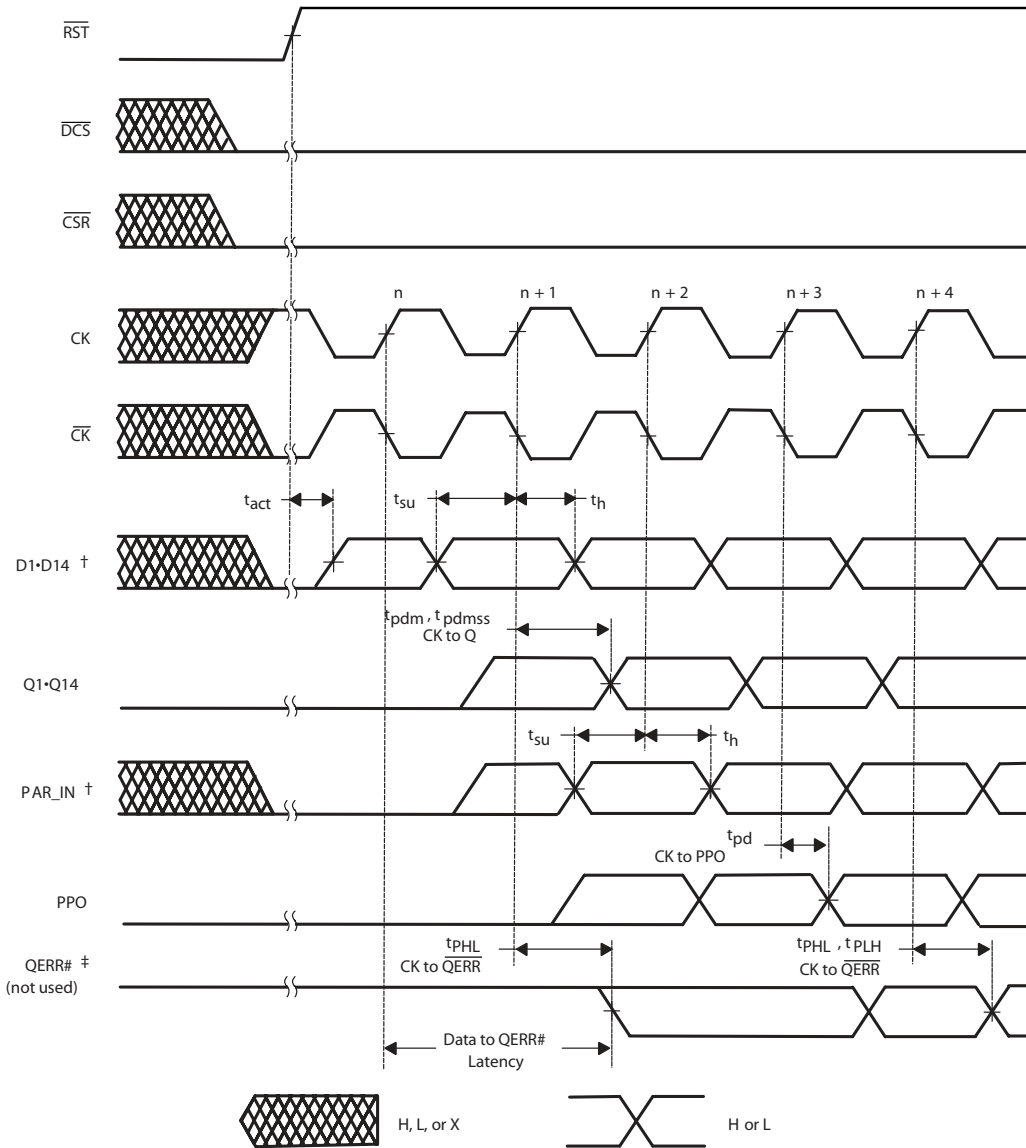


Figure 12 — Timing diagram for the first SSTU32866 (1:2 register-A configuration) device used in pair;  $C0=0, C1=1$ ;  $\overline{RST}$  switches from L to H

† After  $\overline{RST}$  is switched from low to high, all data and  $PAR\_IN$  inputs signals must be set and held low for a minimum time of  $t_{ACT}$  max, to avoid false error

‡ If the data is clocked in on the  $n$  clock pulse, the  $\overline{QERR}$  output signal will be generated on the  $n+1$  clock pulse, and it will be valid on the  $n+2$  clock pulse.

2. Device standard (cont'd)

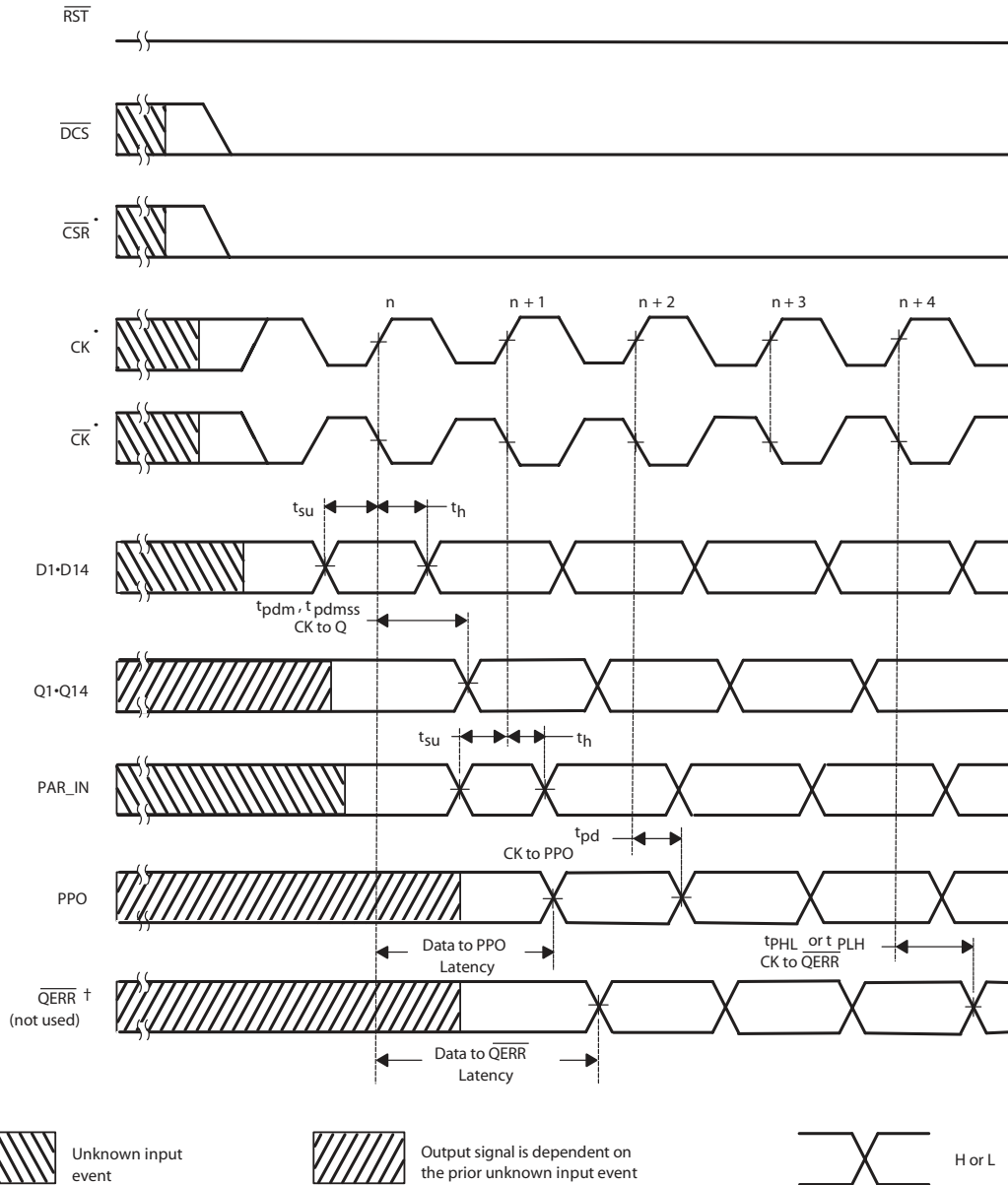


Figure 13 — Timing diagram for the first SSTU32866 (1:2 register-A configuration) device used in pair; C0=0, C1=1;  $\overline{RST}$  being held high

†

If the data is clocked in on the clock pulse, the  $\overline{QERR}$  output signal will be generated on the n+1 clock pulse, and it will be valid on the n+2 clock pulse. If an error occurs and the  $\overline{QERR}$  output is driven low, it stays latched low for a minimum of two clock cycles or until  $\overline{RST}$  is driven low.

2. Device standard (cont'd)

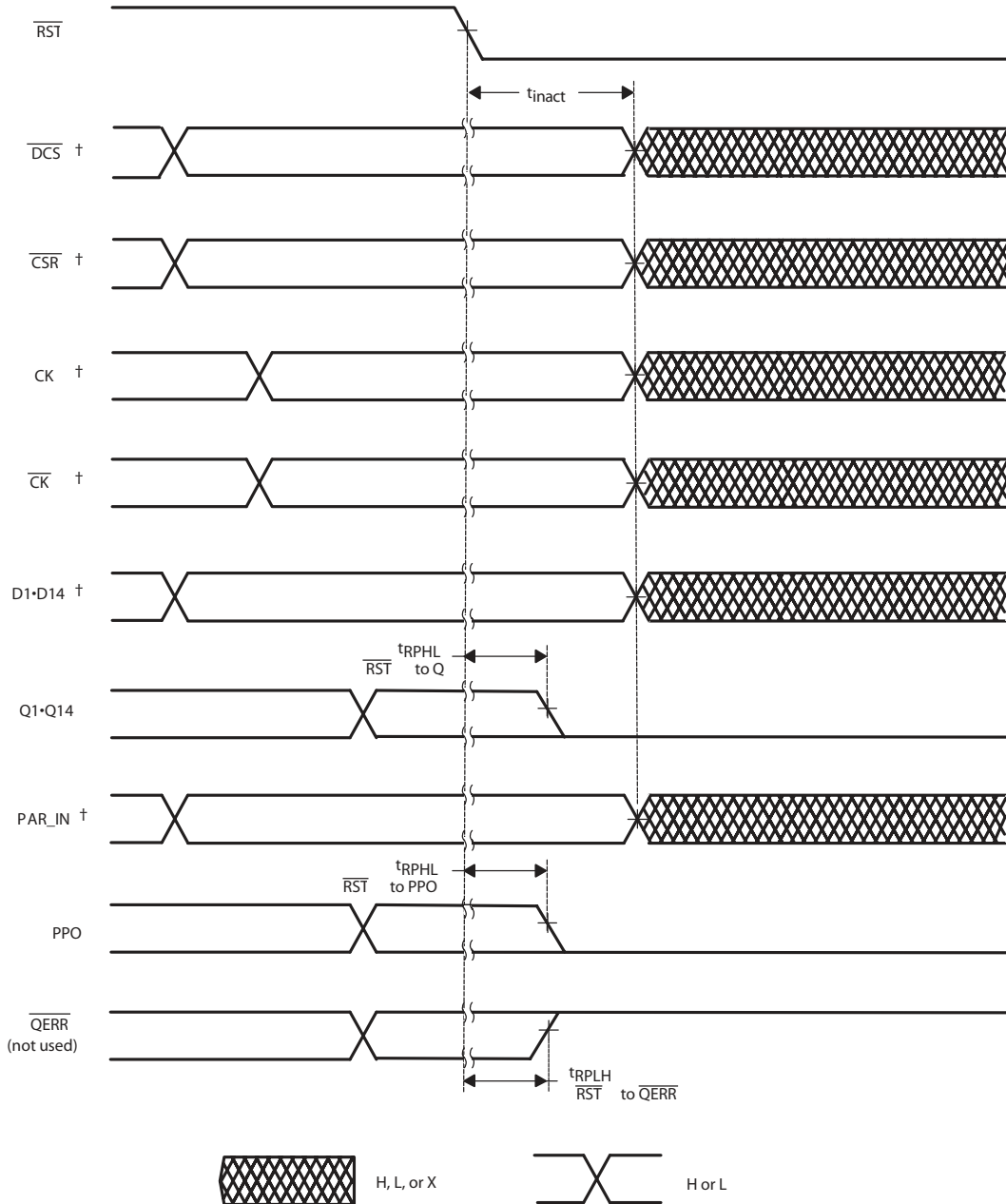
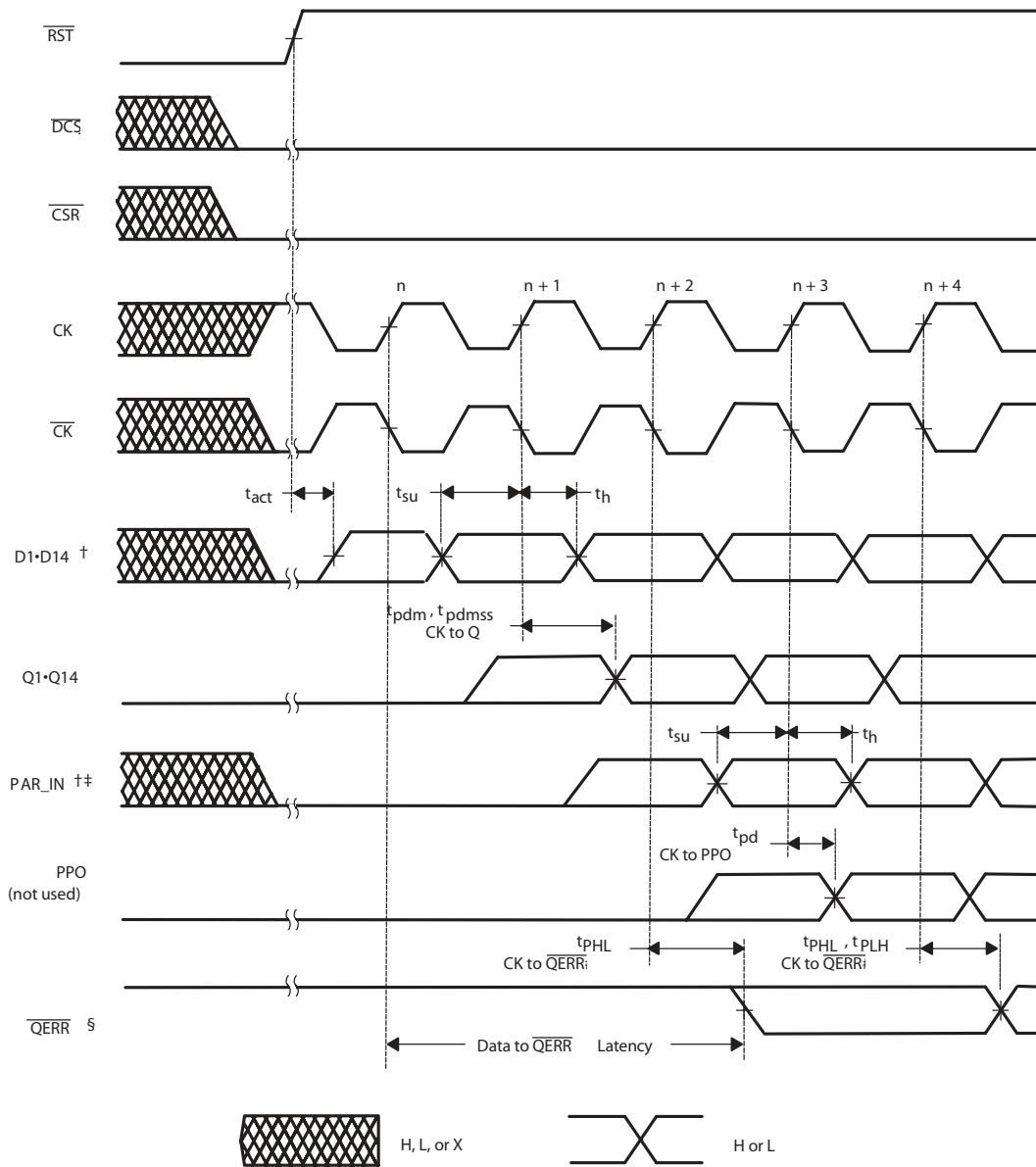


Figure 14 — Timing diagram for the first SSTU32866 (1:2 register-A configuration) device used in pair; C0=0, C1=1;  $\overline{RST}$  switches from H to L

† After  $\overline{RST}$  is switched from high to low, all data and clock inputs signals must be held at valid logic levels (not floating) for a minimum time of  $t_{INACT} \text{ max}$

2. Device standard (cont'd)



**Figure 15 — Timing diagram for the second SSTU32866 (1:2 register-B configuration) device used in pair; C0=1, C1=1; RST switches from L to H**

- † After  $\overline{\text{RST}}$  switched from low to high, all data and PAR\_IN inputs signals must be set and held low for a minimum time of  $t_{\text{ACT max}}$ , to avoid false error.
- ‡ PAR\_IN is driven from PPO of the first SSTU32866 device.
- § If the data is clocked in on the n clock pulse, the  $\overline{\text{QERR}}$  output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse.



2. Device standard (cont'd)

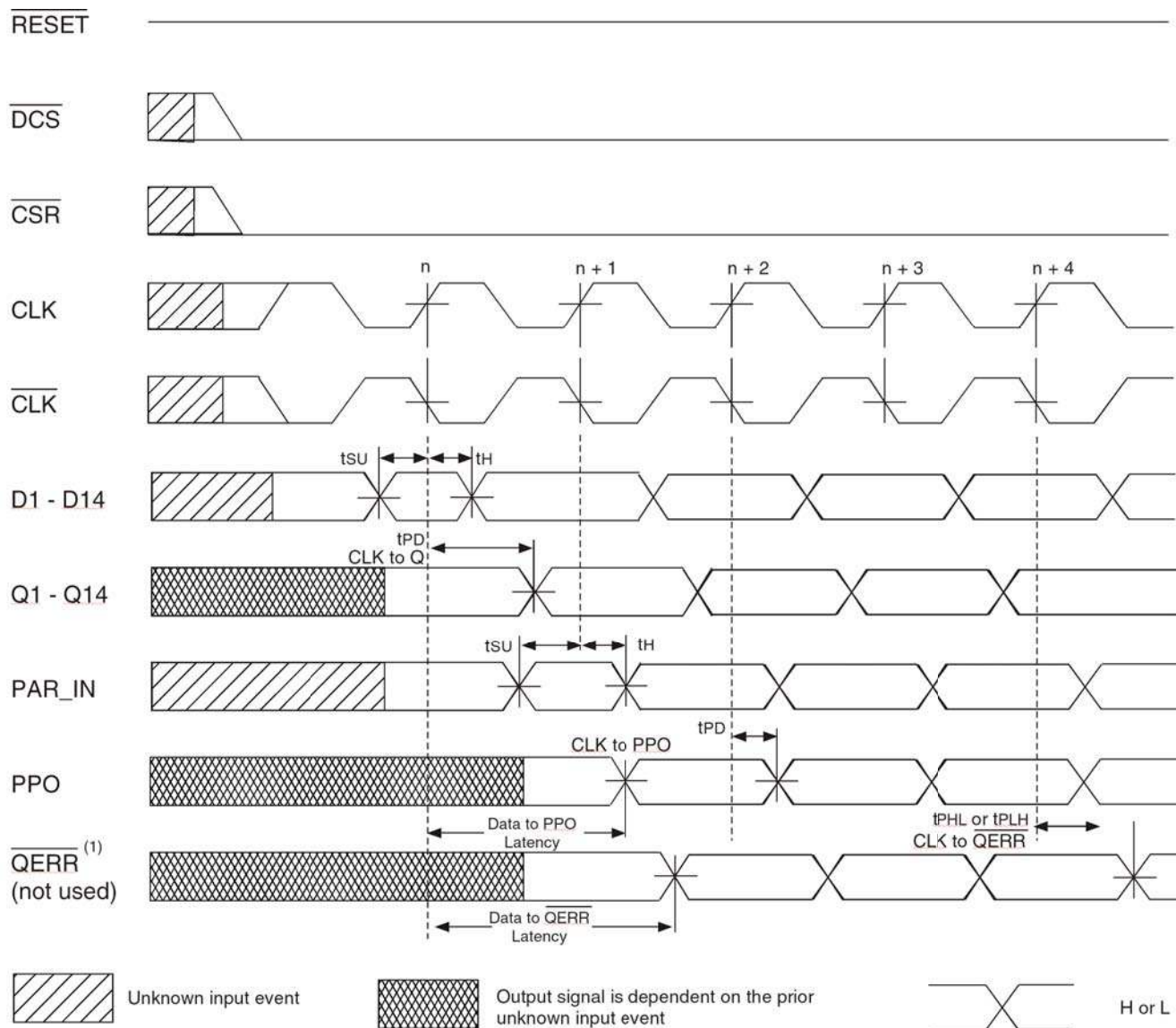


Figure 16 Timing diagram for the second SSTU32866 (1:2 register-B configuration) device used in pair: C0 = 1, C1=1;  $\overline{\text{RESET}}$  being held HIGH

NOTE 1: PAR\_IN is driven from PPO of the first SSTU32866 device. If the data is clocked in on the n clock pulse, the  $\overline{\text{QERR}}$  output signal will be generated on the n+2 clock pulse, and it will be valid on the n+3 clock pulse. If an error occurs and the  $\overline{\text{QERR}}$  signal is driven LOW, it stays latched LOW for a minimum of two clock cycles or until  $\overline{\text{RESET}}$  is driven LOW.

2. Device standard (cont'd)

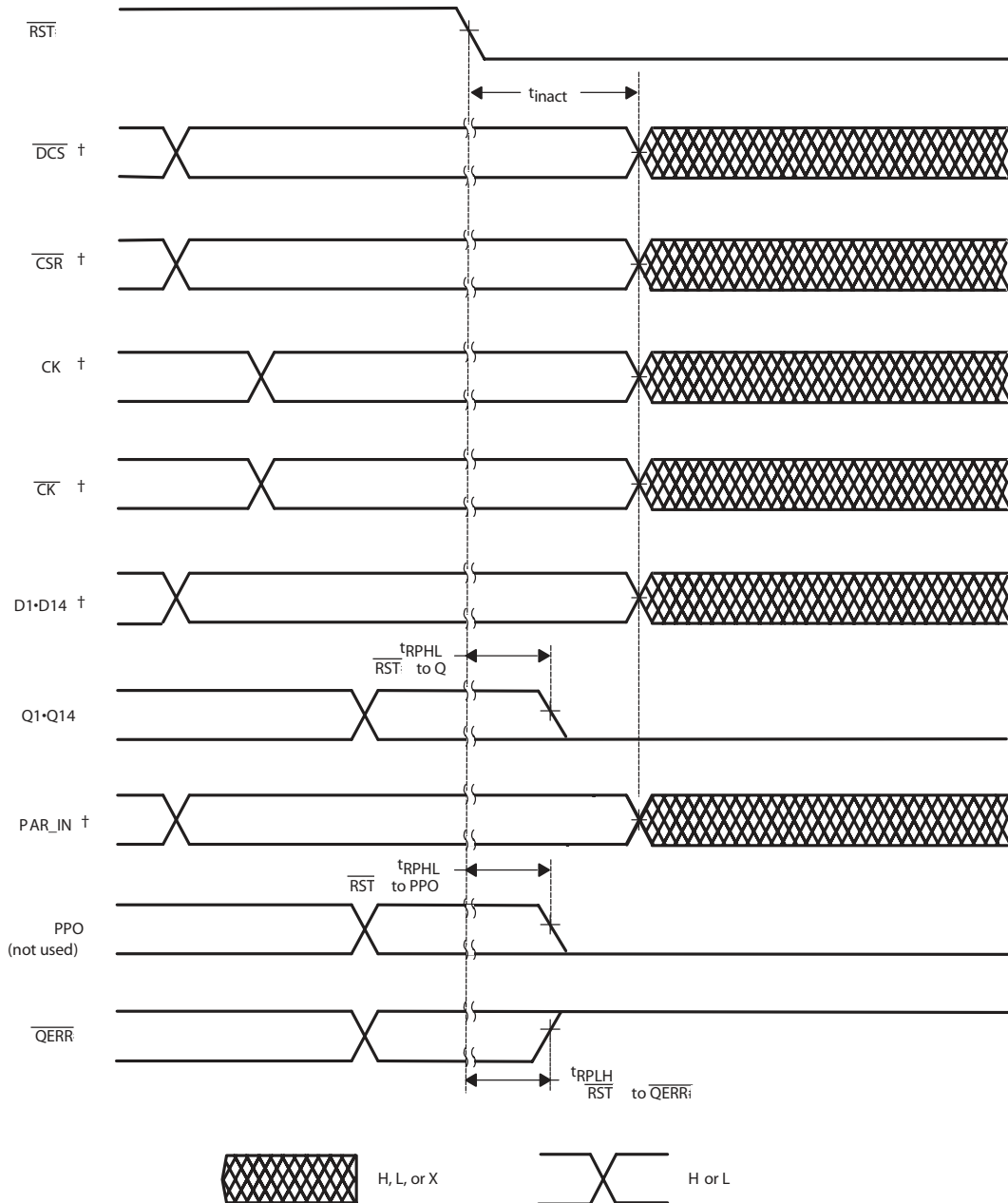


Figure 17 — Timing diagram for the second SSTU32866 (1:2 register-B configuration) device used in pair; C0=1, C1=1;  $\overline{RST}$  switches from H to L

† After  $\overline{RST}$  is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of  $t_{INACT \text{ max}}$ .

**\* Register Configurations**

DATA INPUT:	DATA OUTPUT:	CO	CI
D2, D3, D5, D6, D8 - D25	D2, D3, D5, D6, D8 - D25	0	0
D2, D3, D5, D6, D8 - D14	D2, D3, D5, D6, D8 - D14	0	1
D1 - D6, D8 - D10, D12, D13	D1 - D6, D8 - D10, D12, D13	1	1

## Absolute Maximum Ratings

Storage Temperature	-65°C to +150°C
Supply Voltage	-0.5V to 2.5V
Input Voltage <sup>1,2</sup>	-0.5V to +2.5V
Output Voltage <sup>1,2</sup>	-0.5V to VDD + 0.5V
Input Clamp Current	±50 mA
Output Clamp Current	±50mA
Continuous Output Current	±50mA
VDD or GND Current/Pin	±100mA
Package Thermal Impedance <sup>3</sup>	36°C

### Notes:

1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This value is limited to 2.5V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V <sub>DDQ</sub>	I/O Supply Voltage		1.7	1.8	1.9	V
V <sub>REF</sub>	Reference Voltage		0.49 x V <sub>DD</sub>	0.5 x V <sub>DD</sub>	0.51 x V <sub>DD</sub>	
V <sub>TT</sub>	Termination Voltage		V <sub>REF</sub> - 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
V <sub>I</sub>	Input Voltage		0		V <sub>DDQ</sub>	
V <sub>IH (DC)</sub>	DC Input High Voltage	Data Inputs	V <sub>REF</sub> + 0.125			
V <sub>IH (AC)</sub>	AC Input High Voltage		V <sub>REF</sub> + 0.250			
V <sub>IL (DC)</sub>	DC Input Low Voltage				V <sub>REF</sub> - 0.125	
V <sub>IL (AC)</sub>	AC Input Low Voltage				V <sub>REF</sub> - 0.250	
V <sub>IH</sub>	Input High Voltage Level	RST, C0, C1	0.65 x V <sub>DDQ</sub>			
V <sub>IL</sub>	Input Low Voltage Level				0.35 x V <sub>DDQ</sub>	
V <sub>ICR</sub>	Common mode Input Range	CK, CK	0.675		1.125	
V <sub>ID</sub>	Differential Input Voltage		0.600			
I <sub>OH</sub>	High-Level Output Current				-8	mA
I <sub>OL</sub>	Low-Level Output Current				8	
T <sub>A</sub>	Operating Free-Air Temperature		0		70	°C

<sup>1</sup>Guaranteed by design, not 100% tested in production.

Note: RST and Cn inputs must be held at valid logic levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless RST is low.

## Electrical Characteristics - DC

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 1.8 \pm 0.1\text{V}$  (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS	$V_{DD}$	MIN	TYP	MAX	UNITS
$V_{IK}$		$I_I = -18\text{mA}$				-1.2	V
$V_{OH}$		$I_{OH} = -6\text{mA}$	1.7V	1.2			
$V_{OL}$		$I_{OL} = 6\text{mA}$	1.7V			0.5	
$I_I$	All Inputs <sup>(2)</sup>	$V_I = V_{DD}$ or GND	1.9V	-5		5	$\mu\text{A}$
$I_{DD}$	Standby (Static)	$\overline{\text{RESET}} = \text{GND}$	1.9V			100	$\mu\text{A}$
	Operating (Static) <sup>(3)</sup>	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , $\overline{\text{RESET}} = V_{DD}$				40	mA
$I_{DDD}$	Dynamic operating (clock only)	$\text{RESET} = V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , CLK and $\overline{\text{CLK}}$ switching 50% duty cycle.	$I_o = 0$ 1.8V		39		$\mu\text{A}/\text{clock}$ MHz
	Dynamic Operating (per each data input) 1:1 mode	$\overline{\text{RESET}} = V_{DD}$ , $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$ , CLK and $\overline{\text{CLK}}$ switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle.			19		$\mu\text{A}/\text{clock}$ MHz/data
	Dynamic Operating (per each data input) 1:2 mode				35		
$C_i$	Data Inputs	$V_I = V_{REF} \pm 350\text{mV}$		2.5		3.5	pF
	CLK and $\overline{\text{CLK}}$	$V_{ICR} = 1.25\text{V}$ , $V_{I(PP)} = 360\text{mV}$		2		3	
	$\overline{\text{RESET}}$	$V_I = V_{DD}$ or GND			2.5		

Notes:

- 1 - Guaranteed by design, not 100% tested in production.
- 2 - PAR\_IN leakage current is  $\pm 17\mu\text{A}$  due to weak pull-down resistor. Allows this device to be used as replacement for SSTUB32864B (has no parity).
- 3 - Static operating current will be greater than 40mA if both CLK and  $\overline{\text{CLK}}$  are pulled HIGH or LOW.

## Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range (See figure 7)

PARAMETER	$V_{DD} = 1.8\text{V} \pm 0.1\text{V}$		UNIT
	MIN	MAX	
$dV/dt_r$	1	4	V/ns
$dV/dt_f$	1	4	V/ns
$dV/dt_{\Delta}^1$		1	V/ns

1. Difference between  $dV/dt_r$  (rising edge rate) and  $dV/dt_f$  (falling edge rate)

## Timing Requirements

(over recommended operating free-air temperature range, unless otherwise noted)

SYMBOL	PARAMETERS	$V_{DD} = 1.8V \pm 0.1V$		UNITS
		MIN	MAX	
$f_{clock}$	Clock frequency		410	MHz
$t_W$	Pulse duration, CK, $\overline{CK}$ HIGH or LOW	1		ns
$t_{ACT}$	Differential inputs active time (See Notes 1 and 2)		10	ns
$t_{INACT}$	Differential inputs inactive time (See Notes 1 and 3)		15	ns
$t_{su}$	Setup time	DCS before CK $\uparrow$ , $\overline{CK}$ $\downarrow$ , CSR high; CSR before CK $\uparrow$ , CK $\downarrow$ , $\overline{DCS}$ high		ns
$t_{su}$	Setup time	DCS before CK $\uparrow$ , $\overline{CK}$ $\downarrow$ , CSR low		ns
$t_{su}$	Setup time	DODT, DCKE and data before CK $\uparrow$ , $\overline{CK}$ $\downarrow$		ns
$t_{su}$	Setup time	PAR_IN before CK $\uparrow$ , $\overline{CK}$ $\downarrow$		ns
$t_H$	Hold time	DCS, DODT, DCKE and Q after CK $\uparrow$ , $\overline{CK}$ $\downarrow$		ns
	Hold time	PAR_IN after CK $\uparrow$ , $\overline{CK}$ $\downarrow$		ns

- Notes:**
- 1 - Guaranteed by design, not 100% tested in production.
  - 2 - For data signal input slew rate of 1V/ns.
  - 3 - For data signal input slew rate of 0.5V/ns and < 1V/ns.
  - 4 - CLK/ $\overline{CLK}$  signal input slew rate of 1V/ns.

## Switching Characteristics

(over recommended operating free-air temperature range, unless otherwise noted)

Symbol	Parameter	Measurement Conditions	MIN	MAX	Units
$f_{max}$	Max input clock frequency		410		MHz
$t_{PDM}$	Propagation delay, single bit switching	CK $\uparrow$ to $\overline{CK}$ $\downarrow$ QN	1.1	1.9	ns
$t_{PD}$	Propagation delay	CK $\uparrow$ to $\overline{CK}$ $\downarrow$ to PPO	0.5	1.8	ns
$t_{LH}$	Low to High propagation delay	CK $\uparrow$ to $\overline{CK}$ $\downarrow$ to $\overline{QERR}$	1.2	3	ns
$t_{HL}$	High to low propagation delay		1	2.4	ns
$t_{PDMSS}$	Propagation delay simultaneous switching	CK $\uparrow$ to $\overline{CK}$ $\downarrow$ QN	-	2	ns
$t_{PHL}$	High to low propagation delay	$\overline{RESET}$ $\downarrow$ to QN $\downarrow$		3	ns
$t_{PHL}$	High to low propagation delay	$\overline{RESET}$ $\downarrow$ to PPO $\downarrow$		3	ns
$t_{PLH}$	Low to High propagation delay	$\overline{RESET}$ $\downarrow$ to $\overline{QERR}$ $\uparrow$		3	ns

2. Guaranteed by design, not 100% tested in production.

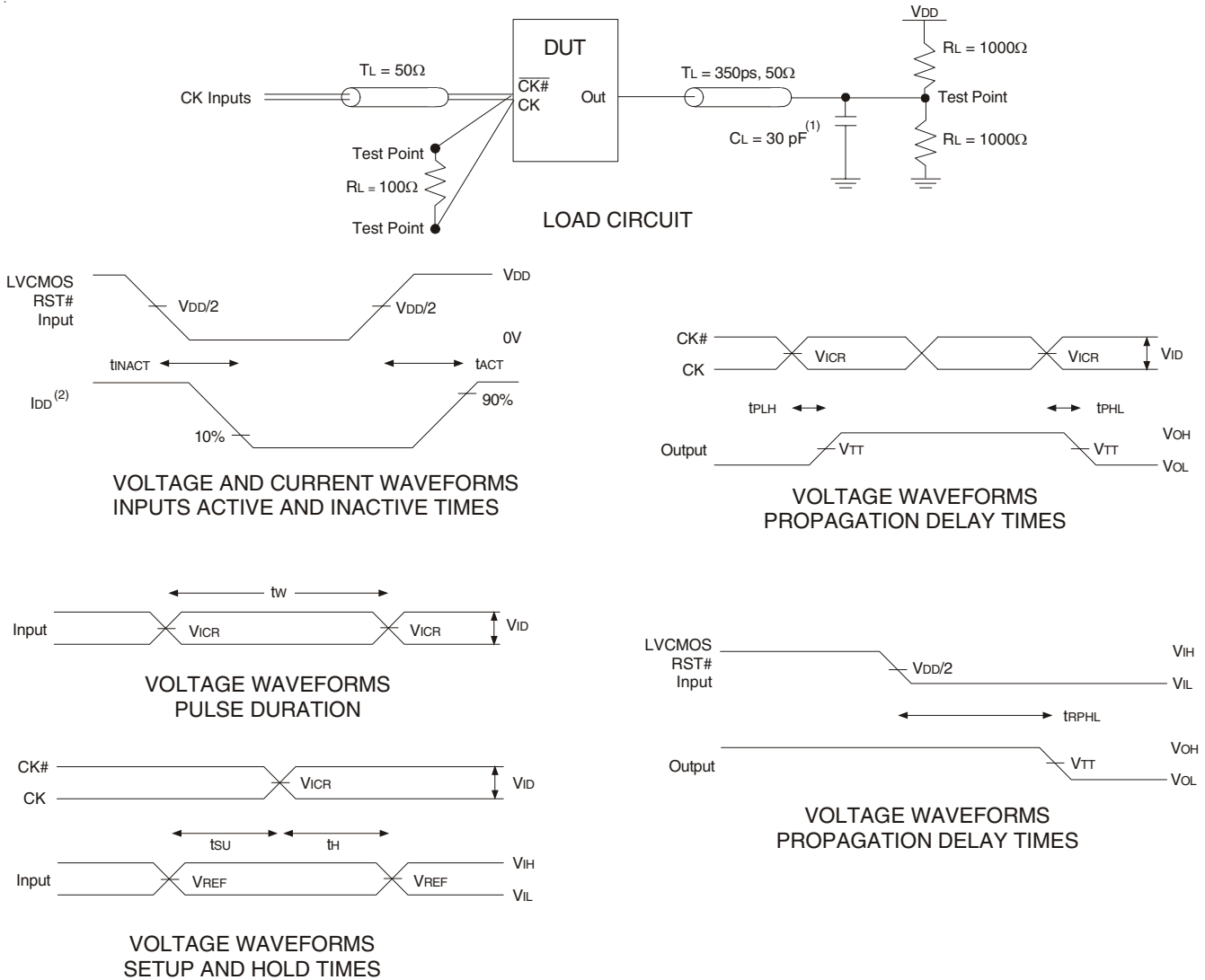
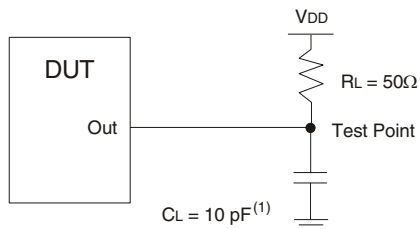
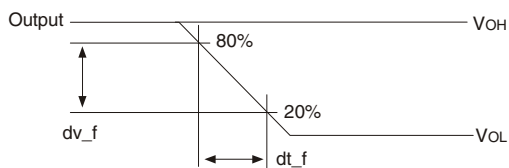


Figure 6 — Parameter Measurement Information ( $V_{DD} = 1.8V \pm 0.1V$ )

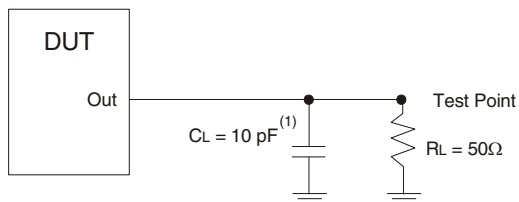
- Notes:
1.  $C_L$  includes probe and jig capacitance.
  2.  $I_{DD}$  tested with clock and data inputs held at  $V_{DD}$  or GND, and  $I_o = 0mA$ .
  3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_o = 50\Omega$ , input slew rate =  $1$  V/ns  $\pm 20\%$  (unless otherwise specified).
  4. The outputs are measured one at a time with one transition per measurement.
  5.  $V_{REF} = V_{DD}/2$
  6.  $V_{IH} = V_{REF} + 250$  mV (ac voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVC MOS input.
  7.  $V_{IL} = V_{REF} - 250$  mV (ac voltage levels) for differential inputs.  $V_{IL} = GND$  for LVC MOS input.
  8.  $V_{ID} = 600$  mV
  9.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PDM}$ .



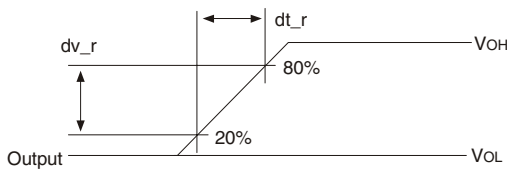
LOAD CIRCUIT - HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS  
HIGH-TO-LOW SLEW-RATE MEASUREMENT



LOAD CIRCUIT - LOW-TO-HIGH SLEW-RATE MEASUREMENT



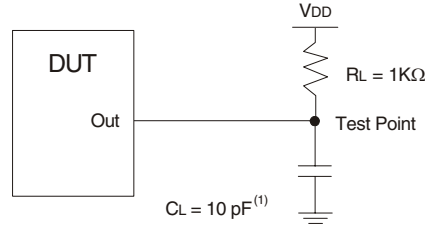
VOLTAGE WAVEFORMS  
LOW-TO-HIGH SLEW-RATE MEASUREMENT

Figure 7 — Output Slew-Rate Measurement Information ( $V_{DD} = 1.8V \pm 0.1V$ )

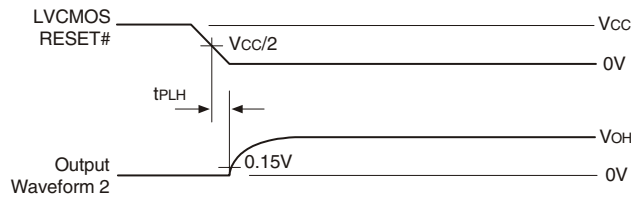
Notes: 1.  $C_L$  includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10MHz$ ,  $Z_O = 50\Omega$ , input slew rate =  $1 V/ns \pm 20\%$  (unless otherwise specified).

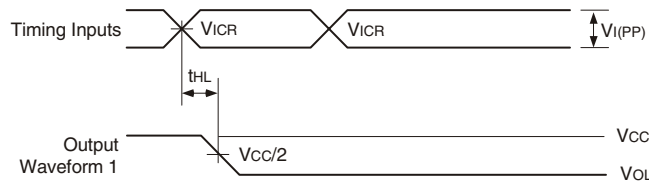




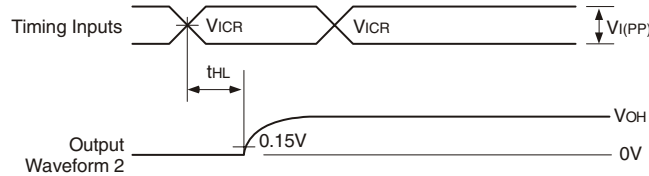
Load Circuit, error output measurements



Voltage Waveforms, open-drain output LOW-to-HIGH with respect to RESET# input



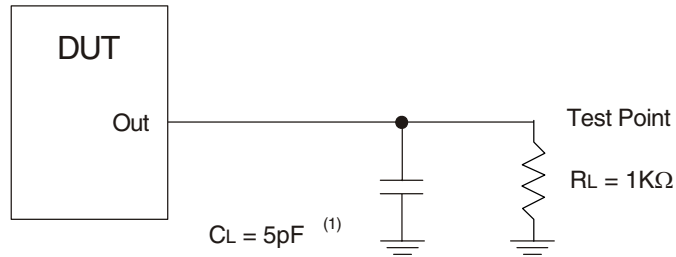
Voltage Waveforms, open-drain output HIGH-to-LOW with respect to clock inputs



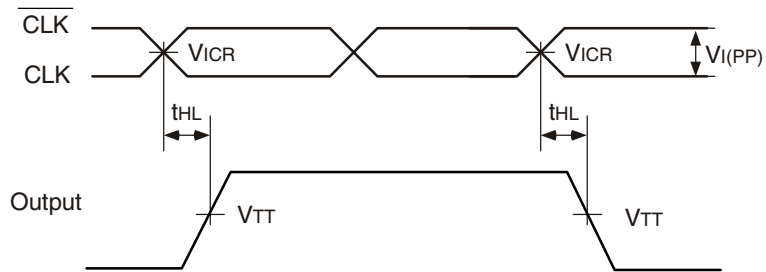
Voltage Waveforms, open-drain output LOW-to-HIGH with respect to clock inputs

Notes: 1.  $C_L$  includes probe and jig capacitance.

2. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{MHz}$ ,  $Z_O = 50\Omega$ , input slew rate =  $1\text{ V/ns} \pm 20\%$  (unless otherwise specified).

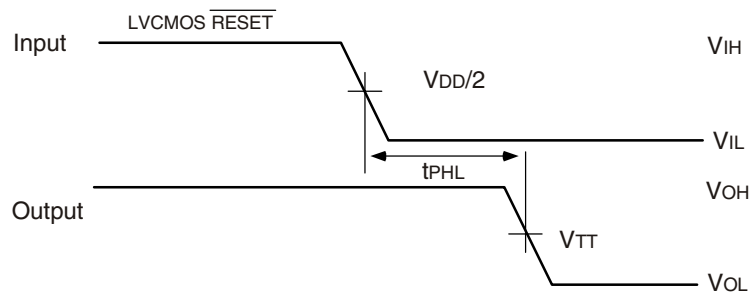


Partial parity out load circuit



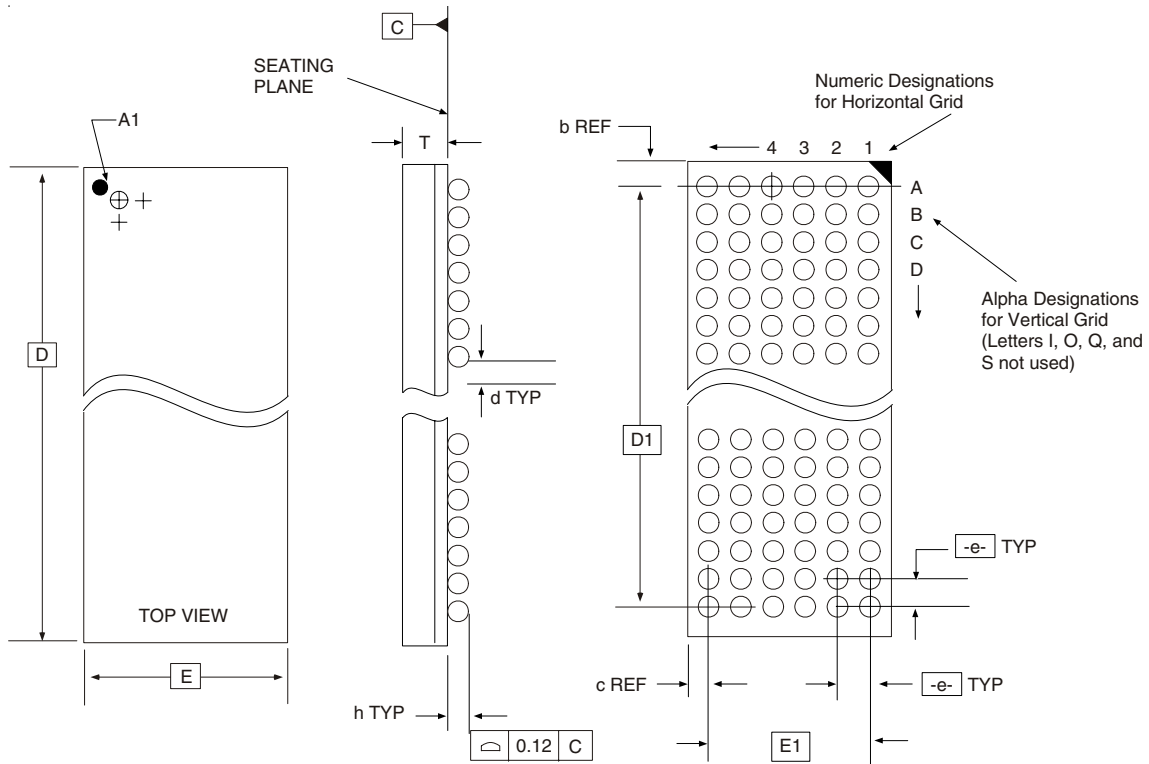
$V_{TT} = V_{DD}/2$   
 $V_{I(P-P)} = 600\text{mV}$   
 $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$

Partial parity out voltage waveform, propagation delay time with respect to CLK input



$V_{TT} = V_{DD}/2$   
 $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$   
 $V_{IH} = V_{REF} + 250\text{mV}$  (AC voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVC MOS inputs.  
 $V_{IL} = V_{REF} - 250\text{mV}$  (AC voltage levels) for differential inputs.  $V_{IL} = V_{DD}$  for LVC MOS inputs.

Partial parity out voltage waveform, propagation delay time with respect to RESET input



ALL DIMENSIONS IN MILLIMETERS

D	E	T	e	---- BALL GRID ----		Max. TOTAL	d	h	REF. DIMENSIONS	
				HORIZ	VERT				b	c
13.50 Bsc	5.50 Bsc	Min/Max	0.80 Bsc	6	16	96	Min/Max	Min/Max	0.75	0.75
11.50 Bsc	5.00 Bsc	1.00/1.20	0.65 Bsc	6	16	96	0.40/0.50	0.25/0.41	0.875	0.875

Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

\* Source Ref.: JEDEC Publication 95, MO-205

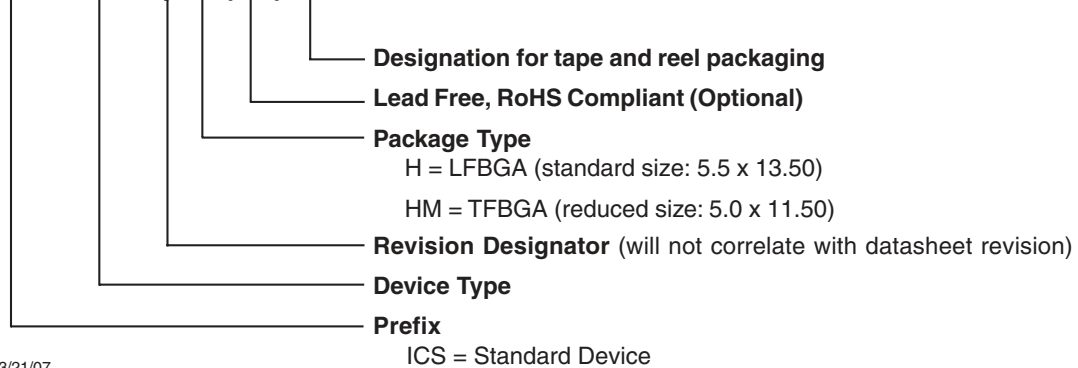
10-0055C

## Ordering Information

### ICSSSTUB32866Bz(LF)T

Example:

**ICS XXXX y z (LF) T**



1165A—3/21/07

<b>Revision History</b>			
<b>Rev.</b>	<b>Issue Date</b>	<b>Description</b>	<b>Page #</b>
0.1	10/3/2005	Initial Release	-
0.2	1/13/2006	Updated Package Dimensions.	27
0.3	1/16/2006	Updated Package Dimensions.	27
0.4	10/25/2006	Added DC table notes 2 and 3	21

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