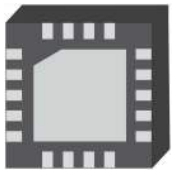
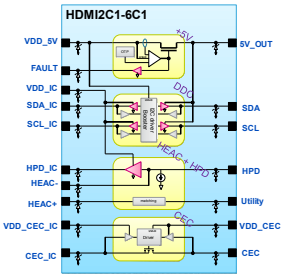
HDMI2C1-6C1

Datasheet

ESD protection and signal booster for HDMI source control stage interface



QFN_18L 3.5 x 3.5
pitch 0.5 mm



Product status link
HDMI2C1-6C1

Features

- For HDMI 1.4 application, operating temperature from -40 to 85 °C
- 8 kV contact ESD protection on the connector side (IEC 61000-4-2 level 4)
- Supports direct connection to low-voltage HDMI ASIC and/or CEC driver (down to 1.8 V)
- High integration level in one package
- DDC (I2C) link protection, bidirectional signal conditioning circuit, and dynamic pull-up
- CEC bus protection, bidirectional level-shifter, backdrive protection, and independent structure from main power supply
- HEAC link protection and line matching
- HPD pulls down, signal conditioning with level shifter and backdrive protection
- Short-circuit protection on 5V output
- Proposed in 500 µm pitch QFN 18L 3.5 x 3.5
- Benefits:
  - Minimal PCB footprint in tablet, set top box, game console, and other consumer application
  - Protection of ultra-sensitive HDMI ASICs
  - Wake-up from standby through CEC bus
  - Ultralow power consumption in standby mode
  - Improved HDMI interface ruggedness and user experience
  - Long and/or poor quality cable support with dynamic pull-up on DDC bus
- Complies with the following standards:
  - Dedicated for HDMI 1.4 version
  - IEC 61000-4-2 level 4
  - JESD22-A114D level 2

Applications

Consumer and computer electronics HDMI source device such as:

- Tablet, smartphone, and notebook
- HD set-top boxes
- Game console
- DVD and blu-ray disk systems
- PC graphic cards

Description

The HDMI2C1-6C1 is an integrated ESD protection and signal conditioning device for control links of HDMI transmitters (source).

This device is a simple solution that provides HDMI designers with an easy and fast way to reach full compliance with the stringent HDMI CTS on a wide temperature range.

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1 Functional description

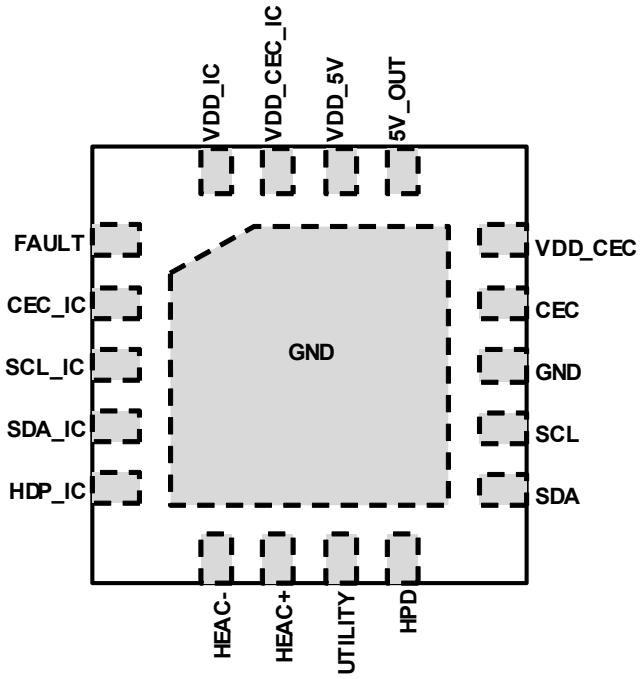
The HDMI2C1-6C1 is a fully integrated ESD protection and signal conditioning device for the control stage of HDMI transmitters (source).

The component offers two buffers, integrating signal conditioning dynamic pull-up on a DDC bus for maximum system robustness and signal integrity. A bidirectional CEC block is integrated, able to wake-up the application from standby mode (all power supply off, except the CEC power supply).

The +5 V supplied to the cable is protected against accidental surge current and short circuit. All these features are provided in an 18 leads QFN package featuring natural PCB routing, cost optimization, and saving space on the board.

The HDMI2C1-6C1 is a simple solution that provides HDMI designers with an easy and fast way to reach full compliance with the stringent HDMI CTS on a wide temperature range. STMicroelectronics proposes also a large range of high speed ESD protections and common mode filter (ECMF series) dedicated to the TMDS lanes giving the flexibility to the designer to filter and protect these (high speed video link against ESD strikes and EMC issues).

Figure 1. Pin configuration (bump side) pin out, top view



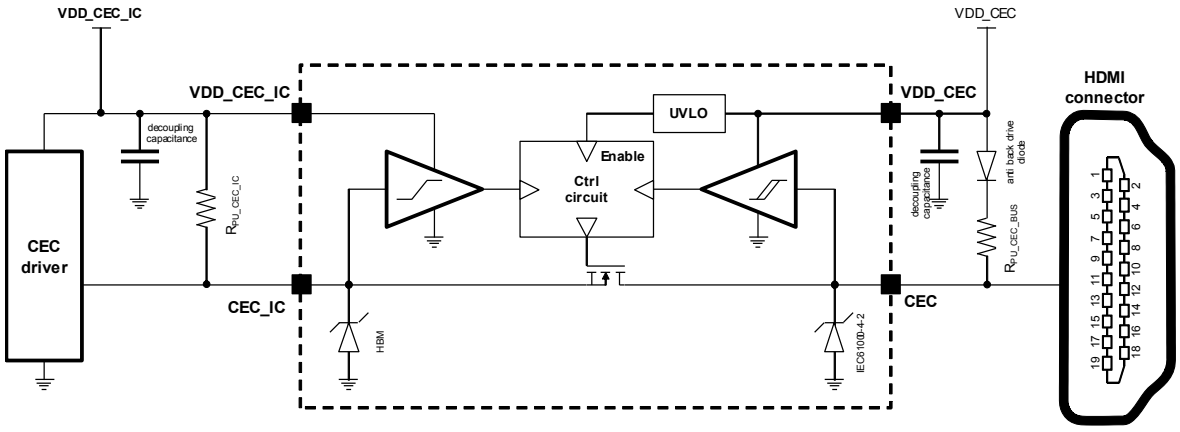
2 Application information

2.1 CEC line description

The CEC bus is described in the HDMI standards as the consumer electronics control. It provides control functions between all the various audiovisual equipment chained in the user's environment.

The CEC block integrated in the HDMI2C1-6C1 implements a level shifter, shifting the cable CEC +3.3 V voltage (V_{DD_CEC}) down to the ASIC power supply voltage (V_{DD_IC}) that can be as low as 1.8 V. The Figure 2 shows the functional diagram of the integrated CEC block.

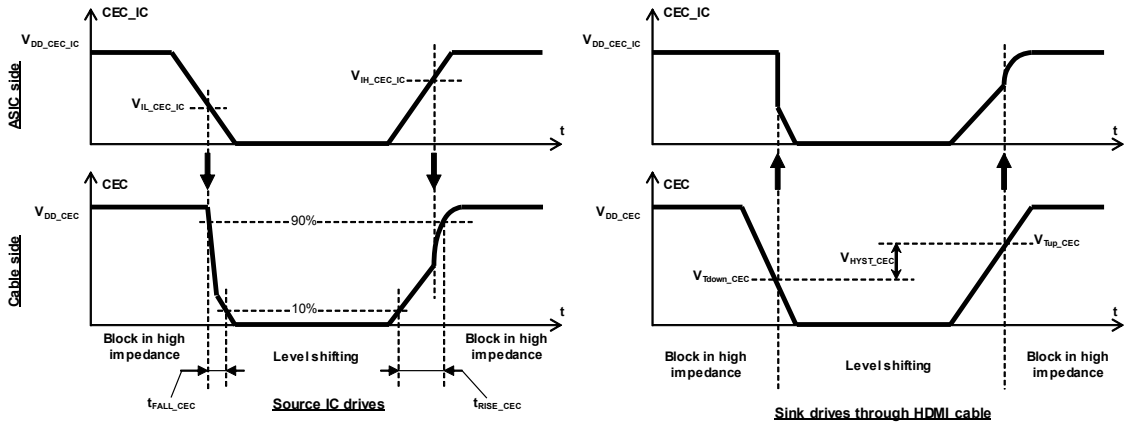
Figure 2. CEC link functional diagram



In case of no activity on the bus, or if the CEC driver is off (V_{DD_CEC} = 0), the output CEC pin is put in high-Z mode (open circuit) protecting the circuitry and the application against hazardous backdrive.

The Figure 3 illustrates the normal operating mode of the CEC block when the IC from the source and when the sink drives the communication.

Figure 3. CEC simplified



In case the application is in standby mode, the +5V main supply of the application is generally powered off in order to reduce as much as possible the global power consumption. The CEC driver can be the only device still working in low power mode, allowing a wake-up of the whole application through the CEC line. When the main power supply +5V is switched off, and if the CEC bus is still active (VDD_CEC power in on state), the HDMI2C1-6C1 keeps the CEC bus working properly while all other outputs are put in high-Z mode.

The CEC output (cable side) integrates a protection against ESD, which is compliant with the IEC61000-4-2 standard, level 4 (8 kV contact).

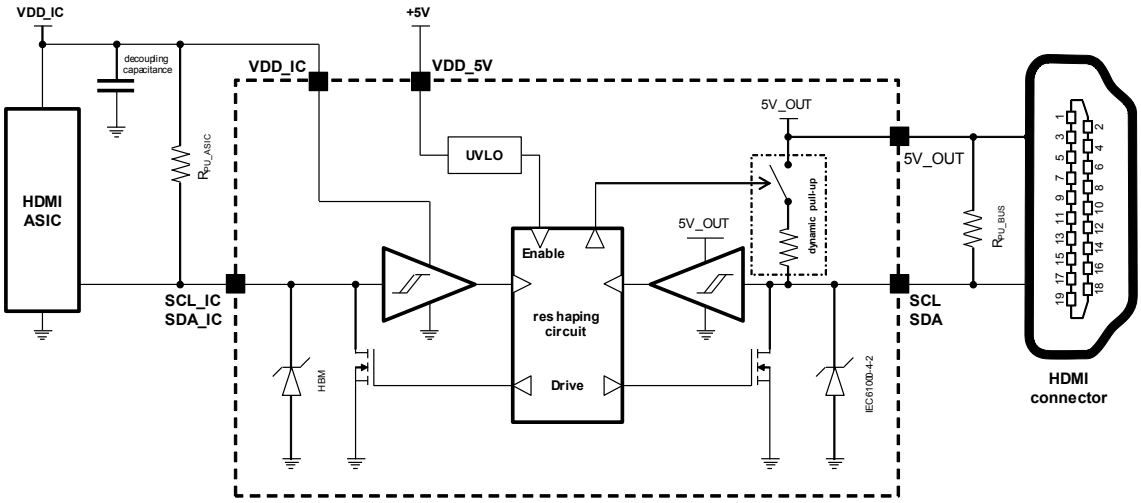
2.2 DDC bus description

The DDC bus is described in the HDMI standards as the display data channel. The topology corresponds to an I2C bus that must be compliant with the I2C bus specification UM10204 revision 5 (October 2012). The DDC bus is made of two lines: data line (SDA) and clock line (SCL). It is used to create a point to point communication link from the source to the sink. EEDID and HDCP protocols are especially flowing through this link, making this I2C communication channel a key element in the HDMI application.

The DDC block integrated in the HDMI2C1-6C1 allows a bidirectional communication between the cable and the ASIC. It is fully compliant with the HDMI 1.4 standard (I2C bus specification) and its CTS. It is shifting the 5 V voltage from the cable (V5V_OUT) down to the ASIC voltage level (VDD_IC) that can be as low as 1.8 V.

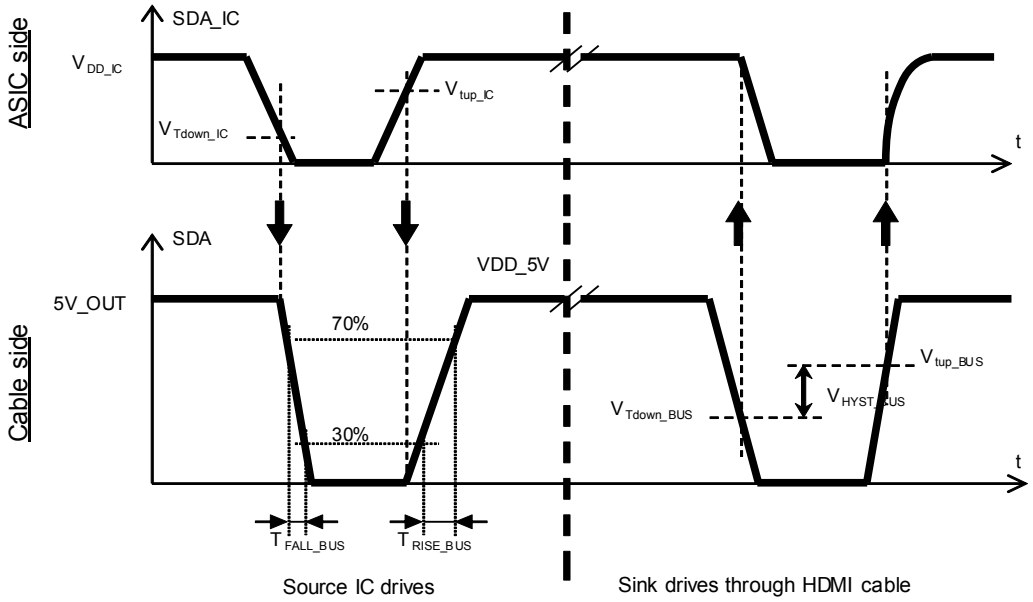
The Figure 4. DDC buffer functional diagram (SCL and SDA lines) shows the functional diagram of the DDC block integrated in the HDMI2C1-6C1 device.

Figure 4. DDC buffer functional diagram (SCL and SDA lines)



The Figure 5. Simplified view of the electrical parameters of the DDC block illustrates the electrical parameter of the DDC block specified by the Table 7. DDC bus (SDA and SCL) line electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, unless otherwise specified).

Figure 5. Simplified view of the electrical parameters of the DDC block

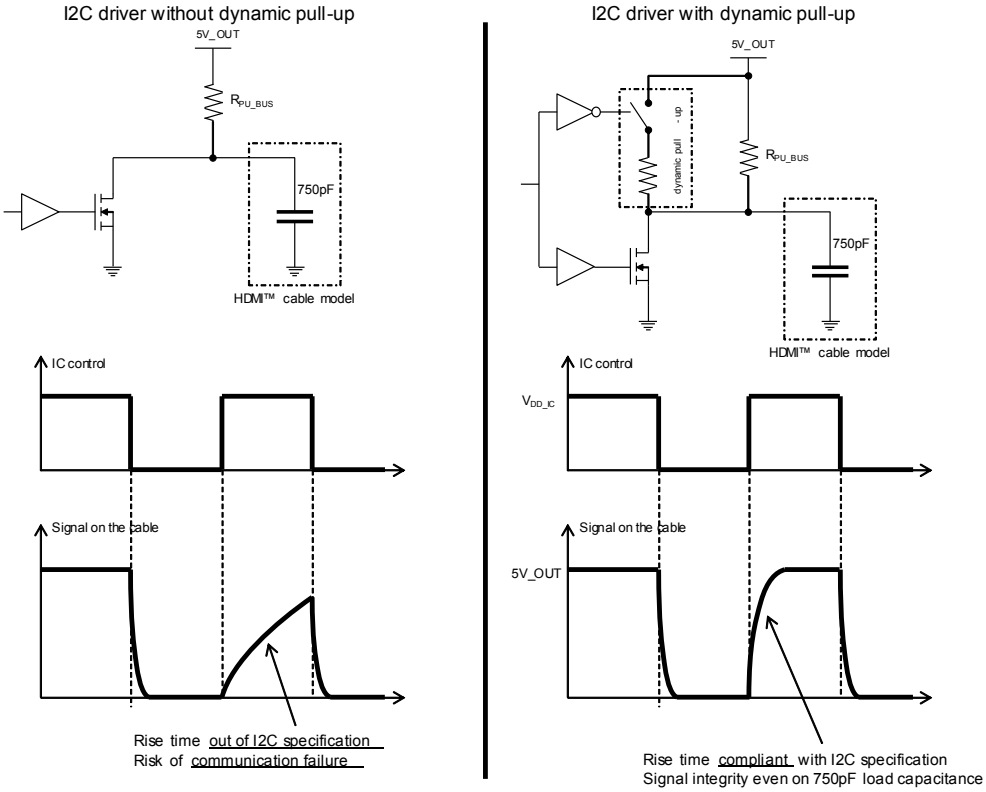


The HDMI standard specifies that the max capacitance of the cable can reach up to 700 pF. Knowing that the max capacitance of the sink input can reach up to 50 pF, this means that the I2C buffer must be able to drive a load capacitance up to 750 pF. On the other hand, the I2C standard specifies a maximum rise time (30%-70%) of the signal must be lower than 1µs in order to keep the signal integrity. Taking into account the max cable capacitance of 750 pF, it is not possible to guarantee a rise time lower than 1µs in the worst case.

Therefore, a dynamic pull-up has been integrated at the output of the SDA and the SCL lines and synchronized with the I2C driver. This signal booster accelerates for a short period the charging time of the equivalent cable capacitance, allowing driving any HDMI cable.

The Figure 6. Benefit of the dynamic pull-up on the DDC bus illustrates the benefit of the dynamic pull-up integrated in the HDMI2C1-6C1 device.

Figure 6. Benefit of the dynamic pull-up on the DDC bus



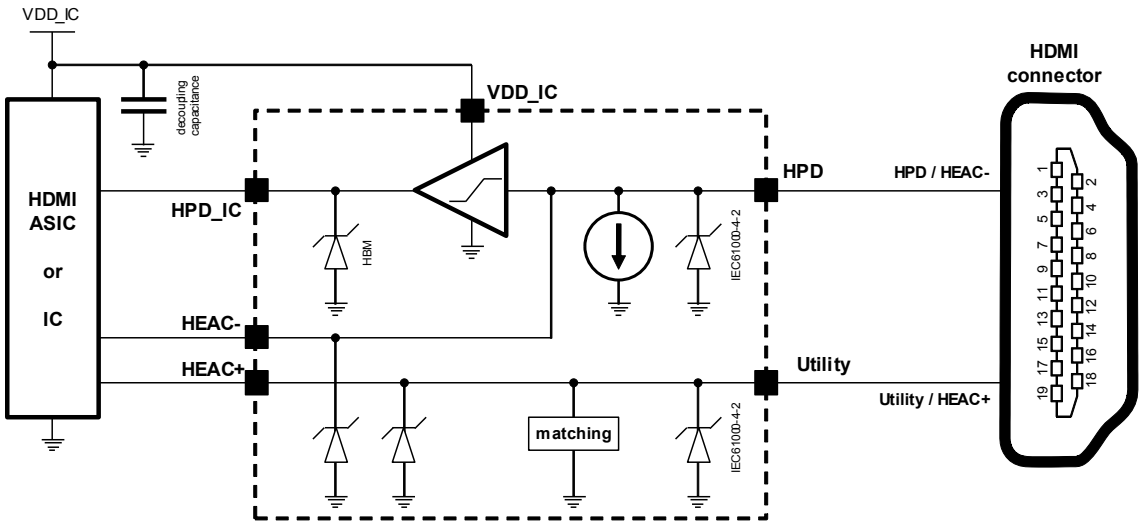
In order to activate the DDC bus, both the following conditions must be respected: VDD_5V must be higher than the VDD_ON threshold (see Table 3. Power supply characteristics (T_{amb} = 25 °C)), and all inputs and outputs (SDA, SCL, SDA_IC, SCL_IC) must be set to a high level at the same time.

The DDC outputs (SCL and SDA on the cable side) integrate a protection against ESD, which is compliant with IEC61000-4-2 standard, level 4 (8 kV contact).

2.3 HEAC link and HPD line description

The HDMI2C1-6C1 proposes a unique solution to manage and to protect both the HEAC and the HPD link. The Figure 7 shows an overview of the function diagram of the integrated block.

Figure 7. HEAC / HPD utility functional block diagram



This block simplifies the design and the PCB layout of the HPD + HEAC functions. Simply connect the two pins from the HDMI connector to one side of the device, and then use the three dedicated outputs on the other side of the device to manage separately the HPD and the HEAC links.

Note that HEAC- and HEAC+ must be kept nonconnected when unused (to avoid connecting to GND when unused).

Both HPD and utility inputs (cable side) integrate a protection against ESD, which is compliant with the IEC61000-4-2 standard, level 4 (8 kV contact).

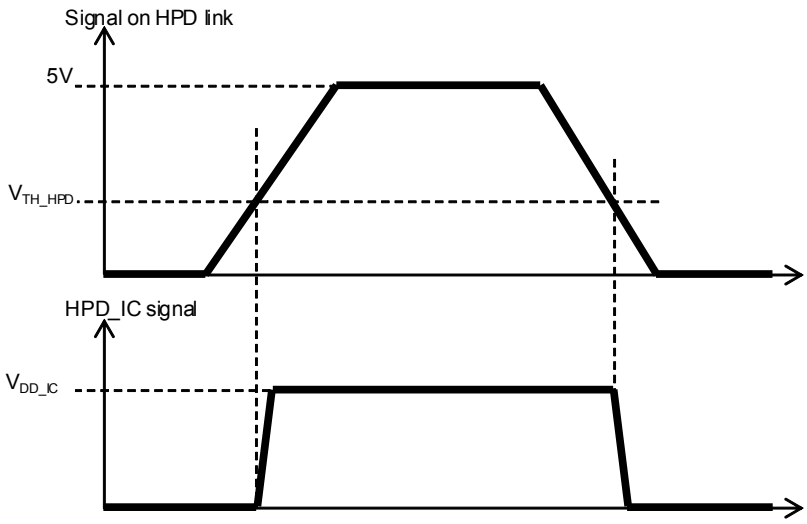
HPD line description

The HPD line is described in the HDMI standards as the hot plug detect function. This line is used by the source device in order to detect if a sink device is connected through an HDMI cable.

The integrated HPD block is pulling down the line via a current source. When the input voltage is detected to be higher than a threshold level, the signal is converted in a high state level on the ASIC side, at the voltage level of the ASIC power supply VDD_IC. Otherwise, the CEC_IC pin remains in low state.

The Figure 8. Simplified view of the electrical parameters of the HPD block show the electrical parameters relevant to the HPD block and specified by the Table 6. HPD, HEAC, and utility line electrical characteristics(T_{amb} = 25 °C, V_{DD_5V} = 5 V, unless otherwise specified).

Figure 8. Simplified view of the electrical parameters of the HPD block



HEAC link

The HEAC link is described in the HDMI 1.4 standards as the HDMI Ethernet and audi return channel. It corresponds physically one differential wired pair made of the utility line and the HPD line. Two signals are transmitted through this link.

The first signal corresponds to the HDMI Ethernet channel (HEC). The signal is transmitted in differential mode (bidirectional) through the HEAC link. The 100Base-TX IEEE 802.3 standard (fast Ethernet 100 Mbps over twisted pair) specifies it. Therefore, the HEC integrates an Ethernet link into the video cable, enabling IP-based applications over the HDMI cable.

The second signal corresponds to the audio return channel (ARC). The signal is transmitted in common mode (unidirectional, from sink to source) through the HEAC link. The IEC 60958-1 standard specify it. The ARC integrates an upstream audio capability, simplifying the cabling of the audiovisual equipment. It is no more necessary to use a coaxial cable from TV to audio amplifier.

The HDMI2C1-6C1 helps the designer to implement this high added value HEAC function in the application, protecting the link against the ESD with no disturbance of the signal. It provides two distinct outputs HEAC+ and HEAC in order to ease as much as possible the PCB layout.

Note that HEAC- and HEAC+ must be kept nonconnected when unused (to avoid connecting to GND when unused).

2.4 +5 V protection and fault line

The HDMI standard describes the +5 V power supply that the source device has to provide to the HDMI cable. It must be protected against the accidental short circuit that could occur on the cable side.

The HDMI2C1-6C1 device embeds a low drop current limiter. If an overcurrent is detected, the HDMI2C1-6C1 limits the current through the +5 V power supply. If the current is too high (short circuit), the device opens the +5V.

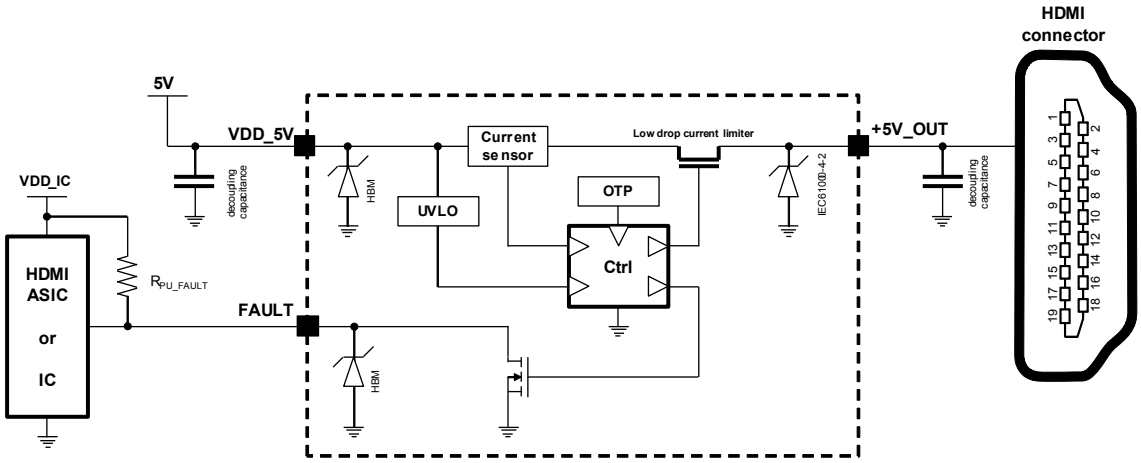
Furthermore, the HDMI2C1-6C1 device embeds also an over temperature protection (OTP). If the internal temperature of the device is reaching a too high value, the +5 V supply is opened in order to protect the application.

In case either the current limiter or the OTP is triggered, a logic signal is sent over the fault line in order to inform the HDMI ASIC that an abnormal situation has been detected (option).

An under voltage lockout (UVLO) is also integrated in the block. It checks the main +5 V power supply state, and enables the +5V_OUT only if the main power supply has reached a minimal value $V_{DD\_5V\_ON}$.

The Figure 9. 5 V link functional diagram shows the functional diagram of the current limiter block.

Figure 9. **5 V link functional diagram**



To summarize, the short circuit protection and the over temperature protection features are providing a high robustness level of the application. On top of this, the fault line feature can be used in order to improve the user experience.

The 5V_OUT pin integrates also a protection against ESD, which is compliant with IEC61000-4-2 standard, level 4 (8 kV contact). The decoupling capacitance is mandatory accordingly to the power management state of the art.

2.5 Application block diagrams

The Figure 10 shows an application block diagram proposal, with all possible options implemented.

The diagram shows that the CEC driver can be totally independent from the HDMI ASIC. By this way, even if the +5V power supply and/or if the HDMI ASIC is sleeping in standby mode, the CEC bus is still active in low power mode. By this way, the designer has then the tools to optimize the power consumption of the global application in standby mode, and in the same time, has the possibility to implement a smart wake-up through the CEC bus enhancing the final user experience.

Figure 10. Application block diagram

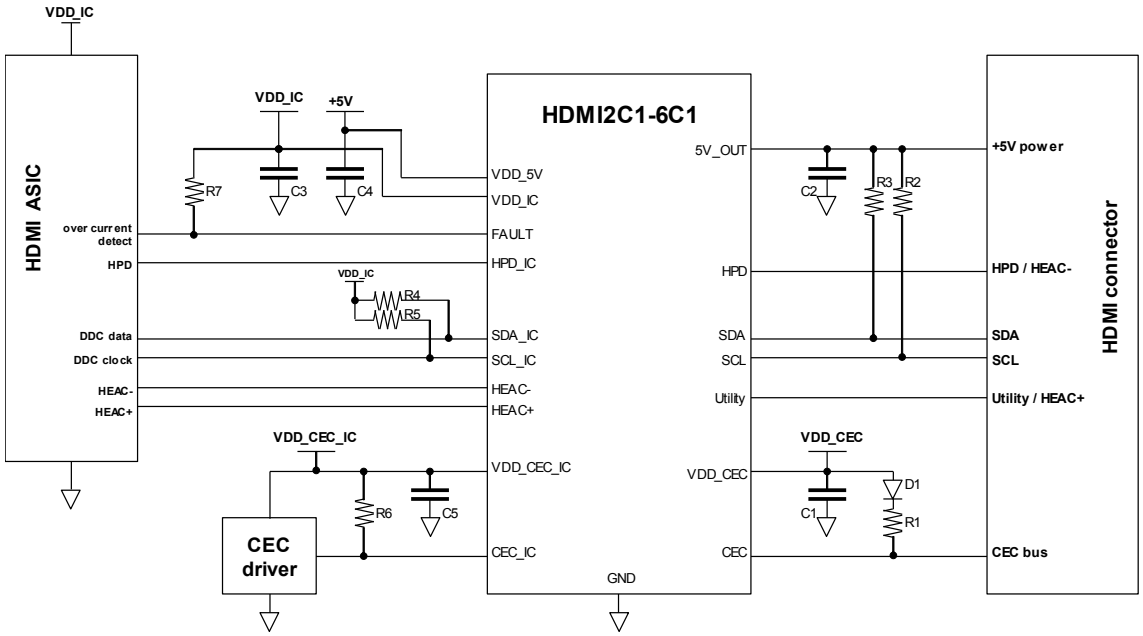
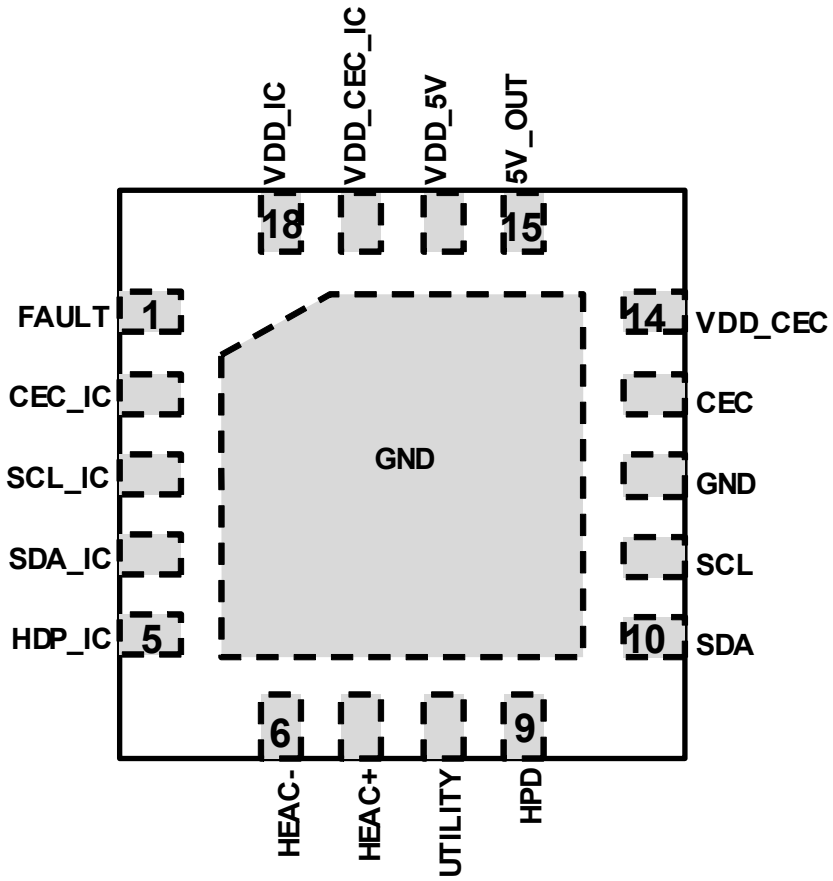


Table 1. External component recommendations

Ref.	Typical value	Comment
R1	27 kΩ	pull up resistance on CEC bus, specified by the HDMI standard
R2, R3	1.8 kΩ	pull up resistance on DDC bus, specified by the HDMI standard
R4, R5	10 kΩ	pull up resistance on DDC bus, ASIC side, value selected to be compliant with I2C levels
R6	270 kΩ to 1 MΩ	pull up resistance on CEC line, ASIC side.
R7	10 kΩ	pull up resistance on FAULT line (option)
D1	BAT54	Small Schottky diode blocking backdrive current flowing toward the VDD_CEC supply
C1 to C5	100 nF	Decoupling capacitance on power supplies

Note: SCL_IC, SDA_IC and CEC_IC have to be driven with an ASIC working with open drain outputs.

Figure 11. **Pin numbering**



3 Electrical characteristics

Table 2. Absolute maximum ratings (limiting values)

Symbol	Parameter	Test conditions	Value	Unit
V_{PP_BUS}	ESD discharge on HDMI cable side (pins 8 to 16) IEC 61000-4-2 level 4	Contact discharge	±8(1)	kV
		Air discharge	±15	
V_{PP_IC}	ESD discharge (all pins) HBM -JESD22-A114D, level 2	Contact discharge	±2	kV
		Air discharge	±2	
T_{STG}	Storage temperature range		-55 to +150	°C
T_{OP}	Operating temperature range		-40 to +85	°C
T_L	Maximum lead temperature		260	°C
V_{DD_5V}, V_{DD_IC}, V_{DD_CEC}, $V_{DD\_CEC\_IC}$	Supply voltages		6	V
Inputs	Logical input min / max voltage range		-0.3 to 6	V

1. *With a 1 µF low ESR capacitor connected to the 5V_OUT pin*

Table 3. Power supply characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD_CEC}	CEC supply voltage, bus side		2.97	3.3	3.63	V
$V_{DD\_CEC\_IC}$	CEC supply voltage, IC side		1.62		3.63	V
V_{DD_IC}	Low-voltage ASIC supply voltage		1.62		3.63	V
V_{DD_5V}	5 V input supply voltage range		4.9	5.0	5.3	V
$V_{DD\_5V\_ON}$(1)	+5 V power-on reset		3.5	3.8	4.1	°C
$V_{DD\_5V\_ON}$	CEC power on reset		2.6	2.8	2.95	V
I_{QS_5V}	Quiescent currents on V_{DD_5V}, V_{DD_IC}, V_{DD_CEC}, $V_{DD\_CEC\_IC}$	V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, V_{DD_CEC} = 3.3 V, $V_{DD\_CEC\_IC}$ = 1.8 V, idle-state on CEC and DDC links, HPD and 5V_OUT links open			600	µA
I_{QS_IC}					75	
I_{QS_CEC}					200	
$I_{QS\_CEC\_IC}$					40	
R_{th}	Junction to ambient thermal resistance	Copper heatsink as shown by Figure 17		70		°C/W
T_{SD}	Thermal shutdown threshold		120		150	°C
P_{TOTAL_SB}	Standby conditions	V_{DD_5V} = V_{DD_IC} = 0 V, V_{DD_CEC} = 3.3 V, $V_{DD\_CEC\_IC}$ = 3.3 V			0.8	mW

1. *In order to activate the DDC lines functional block, the three following conditions have to be met:*
   - *VDD_5V has to reach the VDD_ON threshold*
   - *The inputs and outputs of the bidirectional level shifters must be set to a high level after the power-on*
   - *The HPD line has to be activated one time*

Table 4. CEC electrical characteristics (T_{amb} = 25 °C, V_{DD_CEC} = 3.3 V, $V_{DD\_CEC\_IC}$ = 1.8 V, unless otherwise specified)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tup_CEC}	Upward input voltage threshold on bus side				2.0	V
V_{Tdown_CEC}	Downward input voltage threshold on bus side		0.8			V
V_{HYST_CEC}	Input hysteresis on bus side			0.4		V
T_{RISE_CEC}	Output rise-time (10% to 90%)	R_{UP_CEC} = 14.1 kΩ(1), CCEC_CABLE = 7.9 nF (1)			250	µs
T_{FALL_CEC}	Output fall-time (90% to 10%)				50	µs
I_{OFF_CEC}	Leakage current in powered-off state	V_{DD_5V} = 0 V, V_{DD_IC} = 0 V, V_{DD_CEC} = 3.3			1.8	µA
$V_{IL\_CEC\_IC}$	Input low level on IC side		0.5			V
$V_{IH\_CEC\_IC}$	Input high level on IC side	$V_{DD\_CEC\_IC}$ = 1.8 V			1.5	V
		$V_{DD\_CEC\_IC}$ = 3.3 V			1.9	V
R_{ON_CEC}	On resistance across CEC and CEC_IC pins	CEC pin to 0 V			100	Ω
C_{IN_CEC}	Input capacitance on CEC link	V_{DD_5V} = 0 V, V_{DD_CEC} = 0 V,V_{DD_IC} = 0 V, V_{BIAS} = 0 V, f = 1 MHz, V_{OSC} = 30 mV		25	30(2)	pF

1. *Test conditions are compliant with the worst case CEC specification:*
   - *Correspond to two 27 kΩ +5% pull-up resistances in parallel (compliant with HDMI CTS)*
   - *Max capacitance corresponding to nine equipments chained on the CEC bus*
2. *Maximum capacitance allowed at connector output is 200 pF in the HDMI 1.4 specification.*

Table 5. HDMI 5V_OUT current limiter electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V, unless otherwise specified)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DROP}	Drop-out voltage	I5V_OUT = 55mA	20	50	95(1)	mV
I_{5V_OUT}	Output current	V5V_OUT = 0V	55		115(2)	mA
V_{L_FAULT}	Low level on FAULT pin	RPU_FAULT = 10 kΩ			0.3	V

1. *HDMI 1.4 specification requires a maximum of 100mV voltage-drop.*
2. *Maximum allowed output current is 500 mA when a sink is powered off in the HDMI 1.4 specification.*

Table 6. HPD, HEAC, and utility line electrical characteristics(T_{amb} = 25 °C, V_{DD_5V} = 5 V, unless otherwise specified)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I_{PULL_DOWN}	pull down current in HPD block			15	25	µA
V_{TH_HPD}	HPD input low-level		1.0		1.7	V
C_{IN_HPD} $C_{IN\_Utility}$	Input capacitance	V_{DD_5V} = 0 V, V_{BIAS} = 0 V, f = 1 MHz, V_{OSC} = 30 mV		21	25	pF
f_{CUT_HEAC}	Cut-off frequency of HEAC bus	Single ended mode		200		

Table 7. DDC bus (SDA and SCL) line electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V, V_{DD_IC} = 1.8 V, unless otherwise specified)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tup_BUS}	Upward input voltage threshold on bus side				3.5	V
V_{Tdown_BUS}	Downward input voltage threshold on bus side		1.5			V
V_{HYST_BUS}	Input hysteresis on bus side		1.0		1.3	V
V_{OL_BUS}		Current sunk by SDA pin is 3 mA			0.35	V
T_{RISE_BUS}	Output rise-time (30%-70%)	C_{BUS} = 750 pF(1), R_UP = 2 kΩ // 47 kΩ + 10%(2)			500	ns
T_{FALL_BUS}	Output fall-time (70%-30%)				50	ns
V_{Tup_IC}	Upward input voltage threshold on IC side		55	60	65	$\%V_{DD\_IC}$
V_{Tdown_IC}	Downward input voltage threshold on IC side		35	40	45	$\%V_{DD\_IC}$
V_{OL_IC}	Output low-level on IC side	Current sunk by SDA_IC pin, SCL_IC pins is 500 µA			20	$\%V_{DD\_IC}$
C_{IN_DDC}	Input capacitance on DDC link	V_{DD_5V} = 0 V, V_{DD_IC} = 0 V, V_{DD_CEC} = 0 V, V_{BIAS} = 0 V, f = 1 MHz, V_{OSC} = 30mV		27	32(3)	

1. *Maximum load capacitance allowed on an I2C entire link (cable plus connector) is 750pF in the HDMI 1.4 specification.*
2. *Two pull-up resistors in parallel (sink 47 kΩ + source 2 kΩ).*
3. *Maximum capacitance allowed at connector output is 50pF in the HDMI 1.4 specification.*

Figure 12. CEC typical waveforms (IC to cable communication)

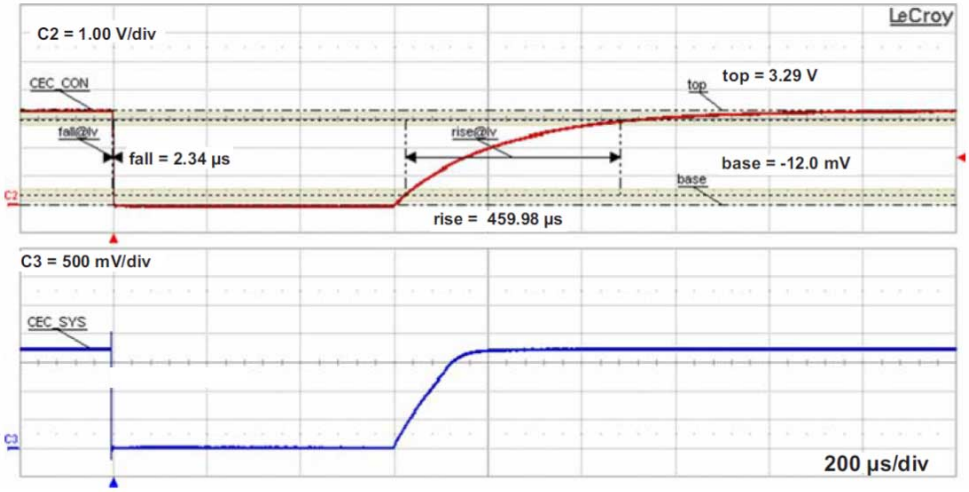


Figure 13. CEC typical waveforms (IC to cable communication)

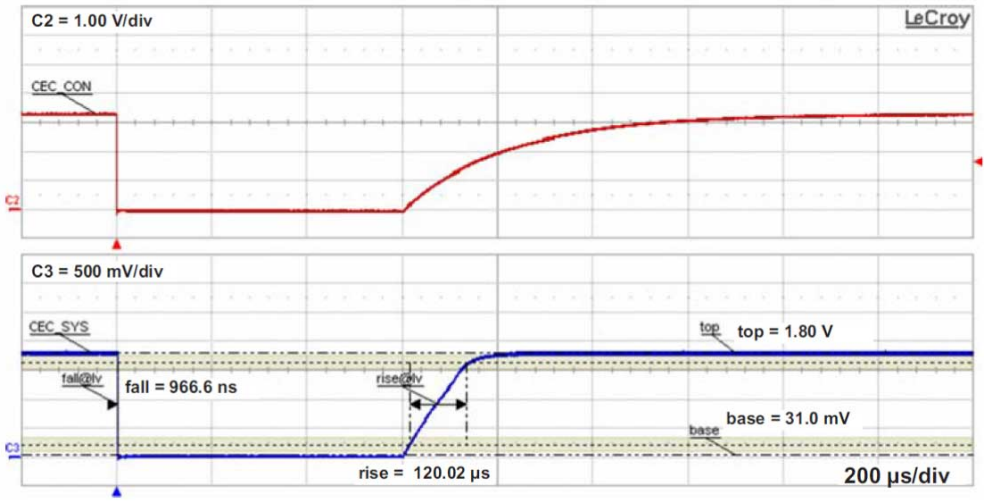


Figure 14. DDC typical waveforms (IC to cable communication)

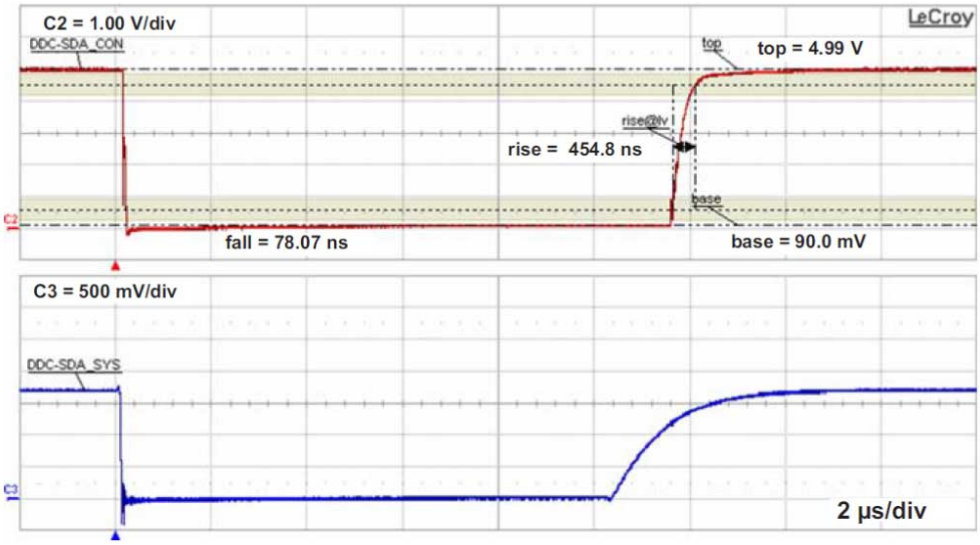


Figure 15. DDC typical waveforms (cable to IC communication)

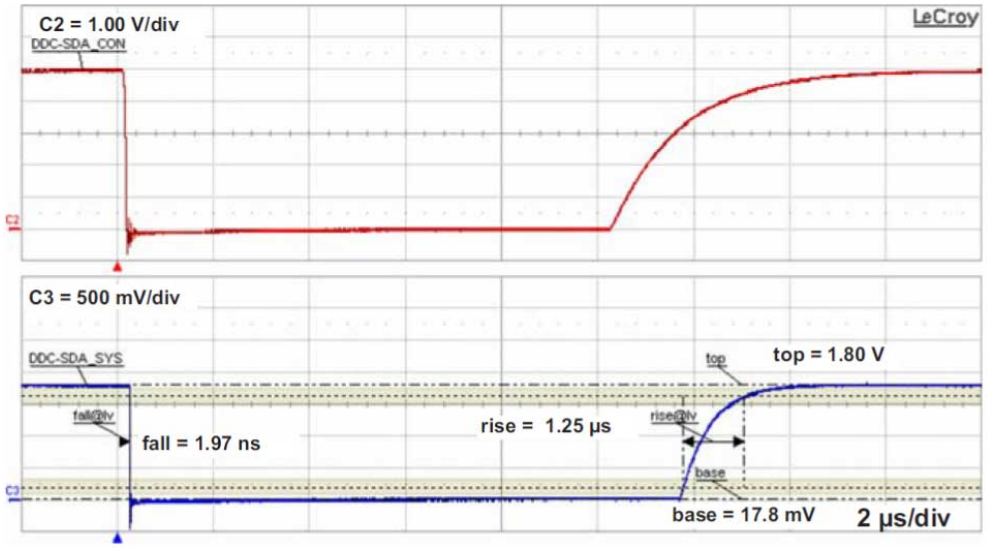


Figure 16. **HPD typical waveform (timing)**

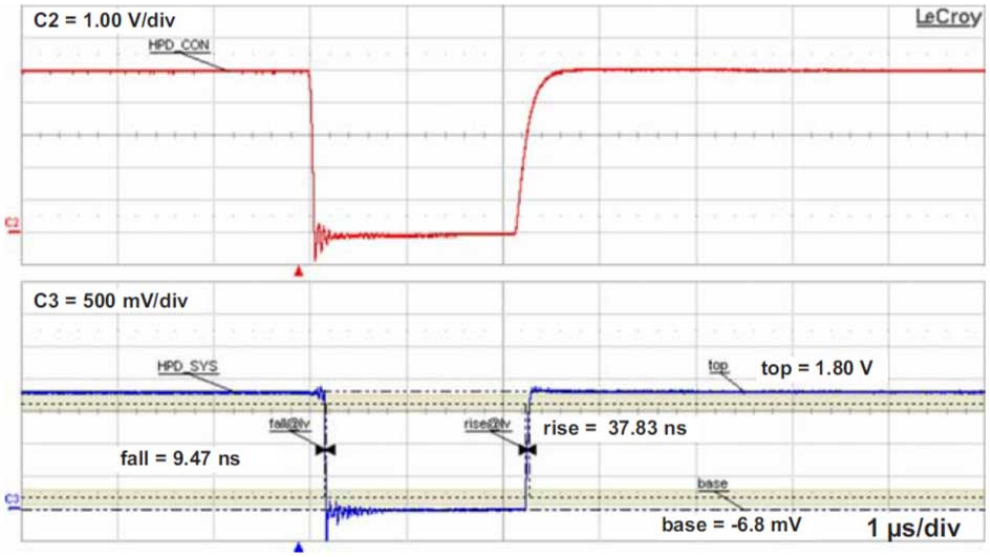
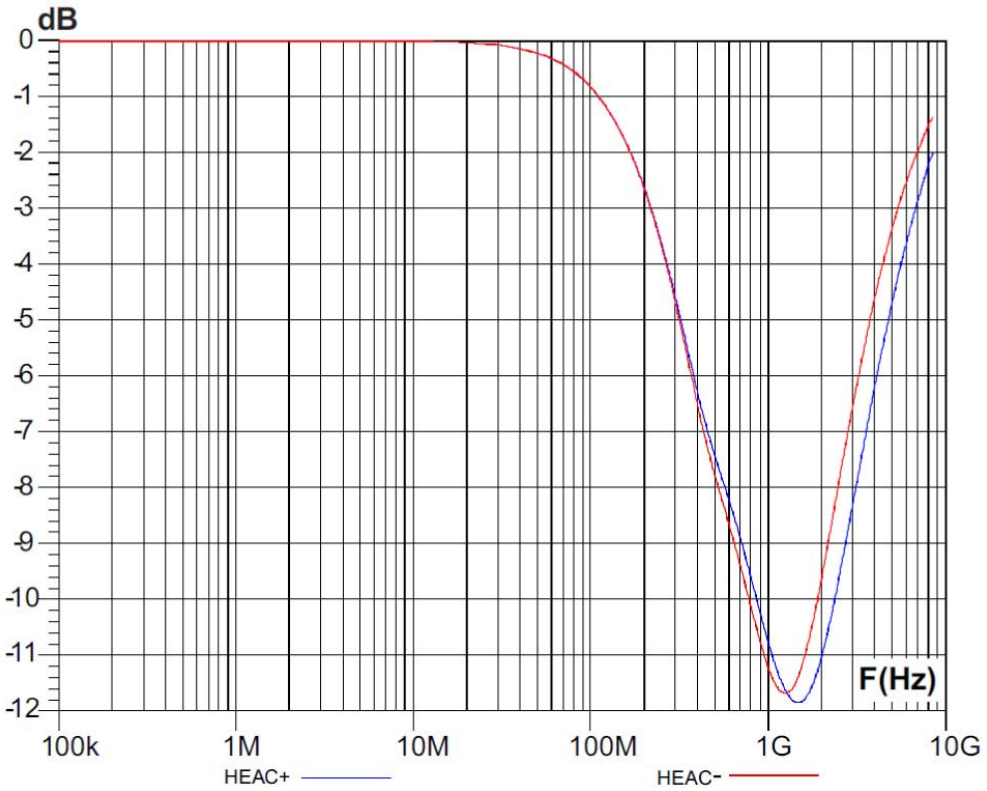


Figure 17. **HEAC single ended mode typical waveform**



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 QFN package information

Figure 18. QFN package outline

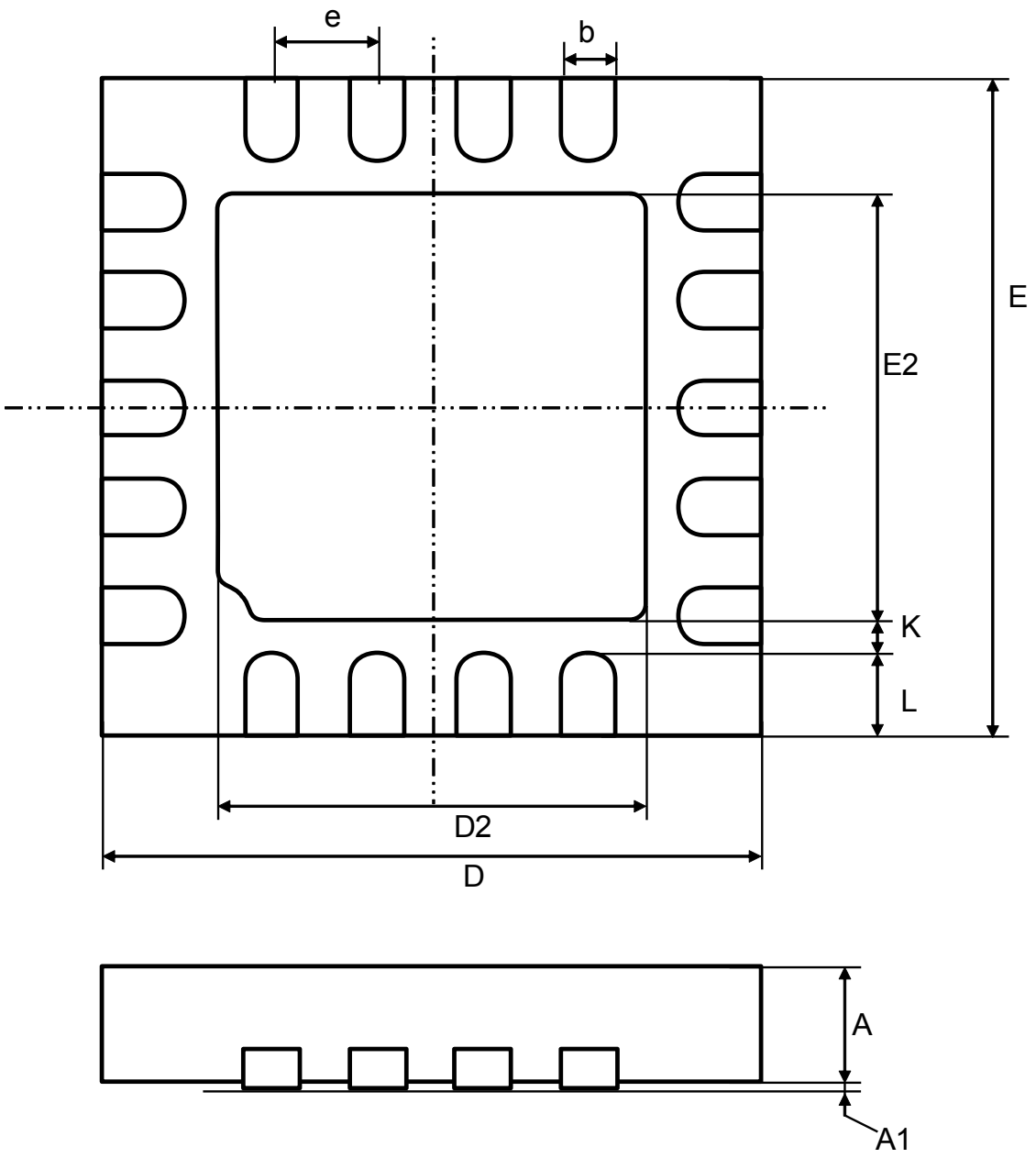
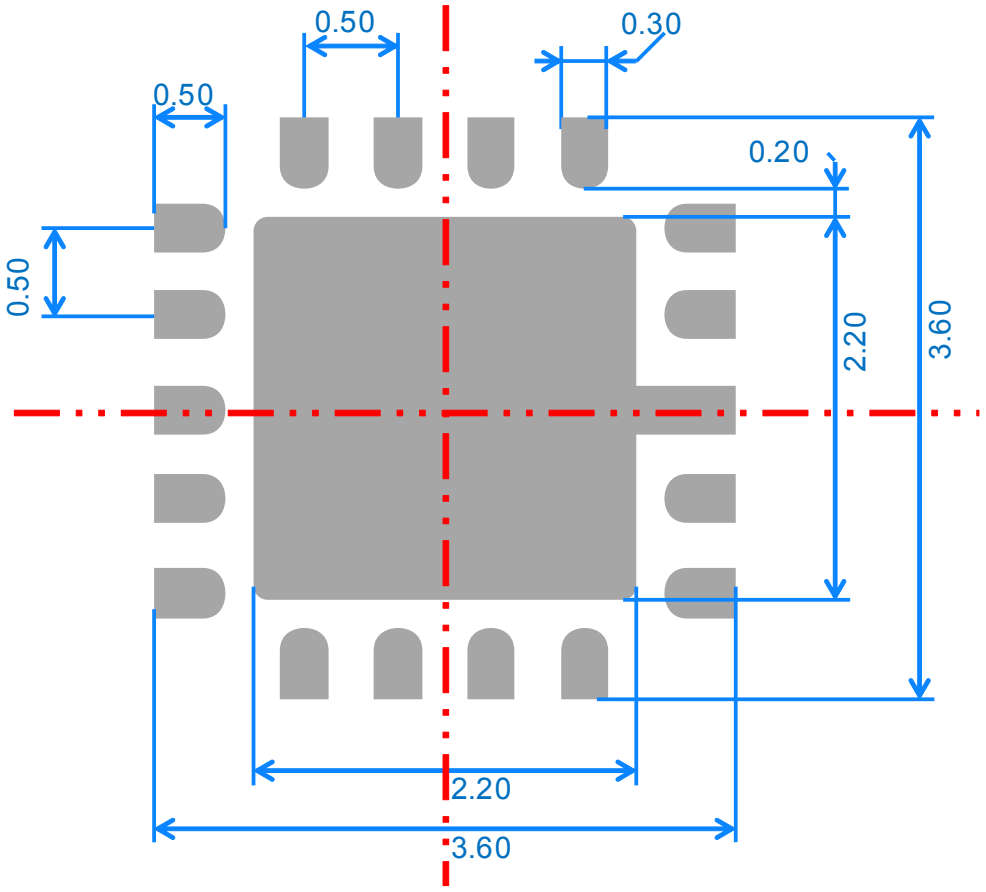


Table 8. **QFN package mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
A	0.51	0.55	0.60
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		3.50	
D2	1.99	2.14	2.24
E		3.50	
E2	1.99	2.14	2.24
e		0.50	
L	0.30	0.40	0.50
K	0.20		

Figure 19. **QFN footprint recommendation (dimensions in mm)**



5 Ordering information

Figure 20. **Ordering information scheme**

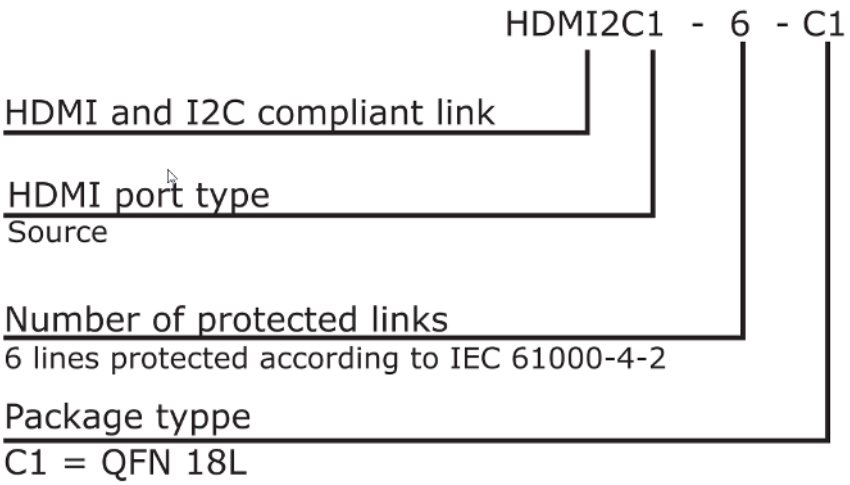


Table 9. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
HDMI2C1-6C1	6HEAC	QFN-18L	12 mg	3000	Tape and reel

Note: More information is available in AN2348 application note :

- *STMicroelectronics 400 micro-meter Flip Chip: package description and recommendation for use*

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
25-Jul-2014	1	Initial release.
10-Aug-2018	2	Minor text changes to improve readability.
15-May-2019	3	Updated Figure 20.
26-Aug-2022	4	Updated Features, Figure 3, Section 2.2 , Table 3, Figure 20 and Table 9. Minor text changes to improve readability.