XCL102/XCL103 Series

ETR28011-005a

Inductor Built-in Step-up “micro DC/DC” Converter (micro DC/DC)

☆Green Operation Compatible

■GENERAL DESCRIPTION

The XCL102/XCL103 series is a synchronous step-up micro DC/DC converter which integrates an inductor and a control IC in one tiny package (2.0mm×2.5mm, h=1.0mm). A stable step-up power supply is configured using only two capacitors connected externally. An internal coil simplifies the circuit and enables minimization of noise and other operational trouble due to the circuit wiring. A wide operating voltage range of 0.65V to 6.0V enables support for applications that require an internally fixed output voltage (2.2V to 5.5V). PWM control (XCL102) or automatic PWM/PFM switching control (XCL103) can be selected.

During the devices enter stand-by mode, XCL102D/XCL103D types prevent the application malfunction by C_L Discharge Function which can quickly discharge the electric charge at the output capacitor (C_L). XCL102/XCL103E types is able to drive Real Time Clock etc.

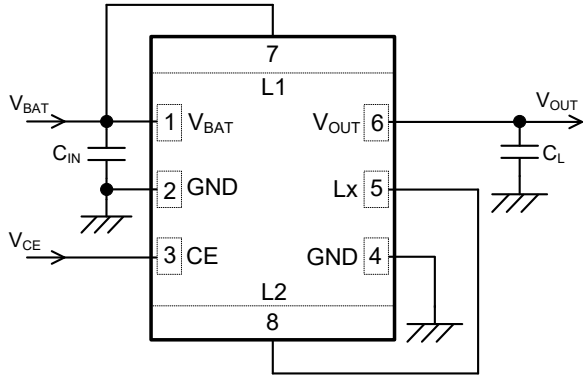
■APPLICATIONS

- Portable equipment
- Beauty & health equipment
- Wearable devices
- Game & Hobby
- PC Peripherals
- Devices with 1~3 Alkaline, 1~3 Nickel Hydride, 1 Lithium and 1 Li-ion

■FEATURES

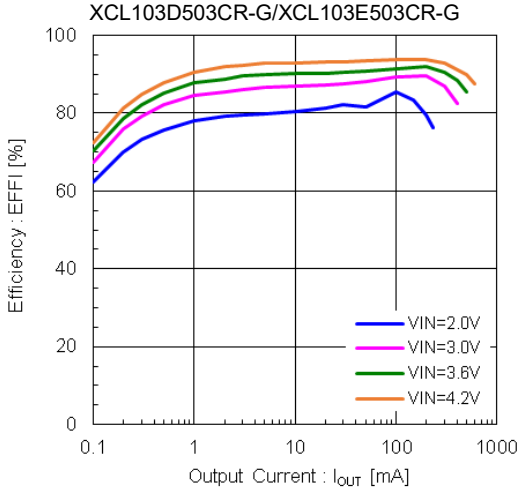
Input Voltage Range	: operating hold voltage 0.65V ~ 6.0V : Start-up voltage 0.9V ~ 6.0V
Fixed Output Voltage	: 2.2V ~ 5.5V (0.1V increments)
Oscillation Frequency	: 3.0MHz
Input Current	: 0.8A
Output Current	: 450mA @V_{OUT}=5.0V, V_{BAT}=3.3V 280mA @V_{OUT}=3.3V, V_{BAT}=1.8V
Control Mode Selection	: PWM (XCL102) PWM/PFM (XCL103)
Load Transient Response	:100mV@V_{OUT}=3.3V, V_{BAT}=1.8V ,I_{OUT}=1mA→200mA
Protection Circuits	: Over-current limit (Integral latch method) Output short-circuit protection
Functions	: Soft-start Load Disconnection (D type) C_L Auto Discharge (D type) Bypass Switch (E type)
Output Capacitor	: Ceramic Capacitor
Operating Ambient Temperature	: -40℃ ~ 85℃
Package	: CL-2025-02
Environmentally Friendly	: EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT



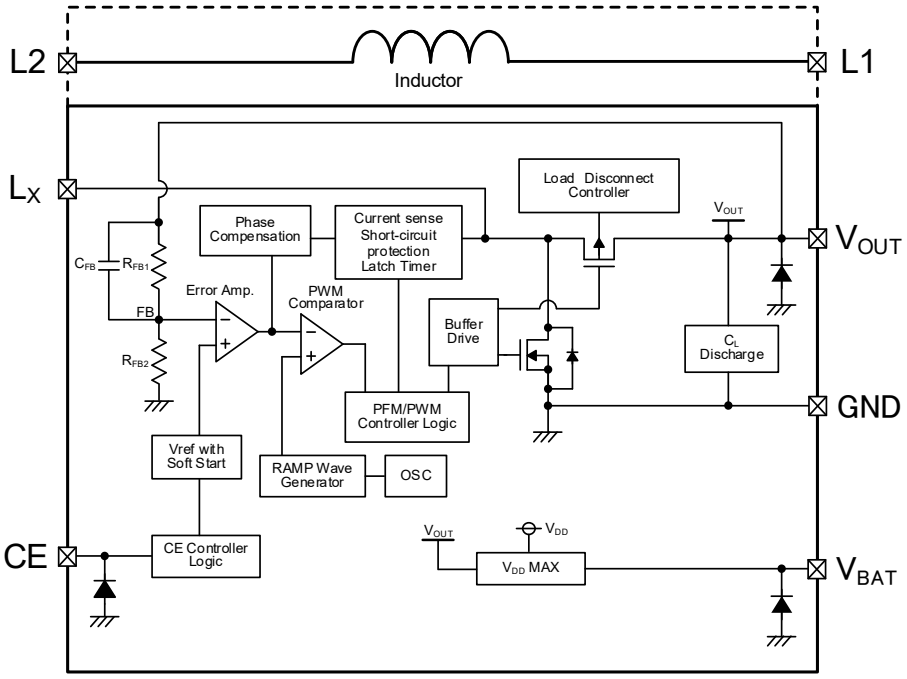
■TYPICAL PERFORMANCE CHARACTERISTICS

XCL103D503CR-G/XCL103E503CR-G



■ BLOCK DIAGRAM

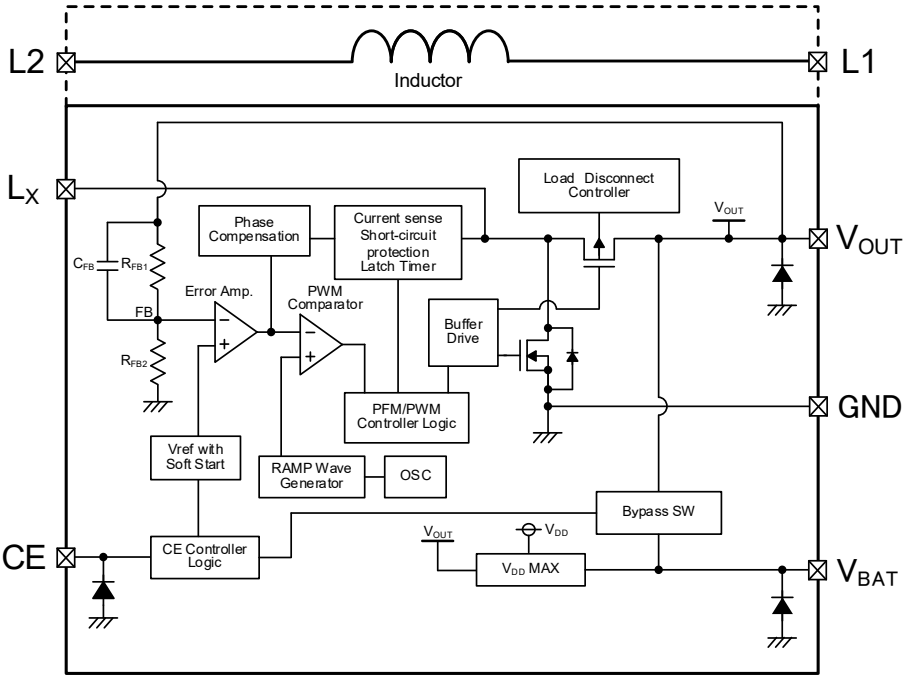
● D Type



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

* XCL102 series chooses only PWM control.

●E Type



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

* XCL102 series chooses only PWM control.

■PRODUCT CLASSIFICATION

●Ordering Information

XCL102①②③④⑤⑥-⑦ PWM control
XCL103①②③④⑤⑥-⑦ PWM/PFM automatic

DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Type	D	Refer to Selection Guide
		E	
②③	Output Voltage	22 ~ 55	Output Voltage options e.g.)3.3V → ②=3, ③=3 5.0V → ②=5, ③=0
④	Oscillation Frequency	3	3.0MHz
⑤⑥-⑦ (*1)	Package (Order Unit)	CR-G	CL-2025-02 (3,000pcs/Reel)

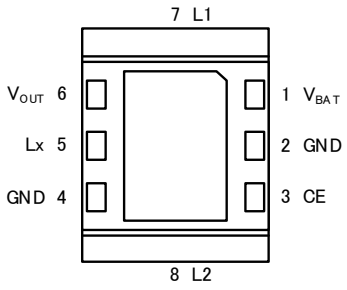
(*1) The "-G" suffix indicates that the products are Halogen and Antimony free as well as being fully EU RoHS compliant.

●Selection guides

Type	Output Voltage	Chip Enable	Soft-Start	Current Limit	Short Protection With Latch	C_L Auto-Discharge	Shutdown at CE="L"
D	Fixed	Yes	Fixed	Yes (with integral latch)	Yes	Yes	Complete Output Disconnect (*1)
E	Fixed	Yes	Fixed	Yes (with integral latch)	Yes	-	Input-to-Output Bypass (*1)

(*1) The V_{OUT} pin cannot be connected to the output pin of another power supply such as AC adapter, etc.

■PIN CONFIGURATION



(BOTTOM VIEW)

* The dissipation pad should be solder-plated in recommended mount pattern and metal masking to enhance mounting strength and heat release. If the pad needs to be connected to other pins, it should be connected to the GND (No. 2,4) pin.

■PIN ASSIGNMENT

PIN NUMBER	PIN NAME	FUNCTIONS
1	V_{BAT}	Power Input
2	GND	Ground
3	CE	Chip Enable
4	GND	Ground
5	Lx	Switching
6	V_{OUT}	Output Voltage
7	L1	Inductor Electrodes
8	L2	

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
CE	L	Stand-by
	H	Active

* Do not leave the CE pin open.

■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNITS
V_{BAT} Pin Voltage	V_{BAT}	-0.3 ~ 7.0	V
Lx Pin Voltage	V_{Lx}	-0.3 ~ 7.0	V
V_{OUT} Pin Voltage	V_{OUT}	-0.3 ~ 7.0	V
CE Pin Voltage	V_{CE}	-0.3 ~ 7.0	V
Power Dissipation (Ta=25℃)	Pd	1000 (40mm x 40mm Standard board) (*1)	mW
Operating Ambient Temperature	Topr	-40 ~ 85	℃
Storage Temperature	Tstg	-55 ~ 125	℃

* GND are standard voltage for all of the voltage.

(*1) The power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■ELECTRICAL CHARACTERISTICS

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
BAT Voltage	V_{BAT}		-	-	6.0	V	①
Output Voltage	V_{OUT}	Voltage to start oscillation while $V_{OUT}=V_{OUT(T)}\times1.03\rightarrow V_{OUT(T)}\times0.97$	<E-1>	<E-2>	<E-3>	V	⑤
Operation Start Voltage	V_{ST1}	R_L=1kΩ	-	-	0.90	V	①
Operation Hold Voltage	V_{HLD}	R_L=1kΩ	-	0.65	-	V	①
Quiescent Current (XCL103 only)	Iq	$V_{OUT}=V_{BAT}=V_{OUT(T)}$+0.5V	-	26	40	μA	③
Supply Current	I_{DD}	$V_{OUT}=V_{BAT}=V_{OUT(T)}$-0.2V	-	<E-5>	3.0	mA	③
Oscillation Frequency	f_{OSC}	$V_{BAT}=V_{OUT(T)}\times0.5$, I_{OUT}=100mA	2.4	3.0	3.6	MHz	①
Maximum Duty Cycle	D_{MAX}	V_{BAT}=1.2V, $V_{OUT}=V_{OUT(T)}$-0.2V	88	93	98	%	⑤
Minimum Duty Cycle	D_{MIN}	$V_{OUT}=V_{BAT}=V_{OUT(T)}$+0.5V	-	-	0	%	⑤
PFM Switching Current (XCL103 only)	I_{PFM}	V_{BAT}=1.5V, R_L is selected with $V_{OUT(T)}$, Refer to Table 1	-	165	230	mA	①
Efficiency (XCL103 only)	EFFI	$V_{BAT}=V_{OUT(T)}\times0.6$, R_L is selected with $V_{OUT(T)}$, Refer to Table 1	-	86(*3)	-	%	①
Efficiency	EFFI	$V_{BAT}=V_{OUT(T)}\times0.6$, I_{OUT}= 100mA	-	90(*3)	-	%	①
Stand-by Current	I_{STB}	$V_{BAT}=V_{Lx}$=6.0V,V_{CE}=0V, (*1)	-	0	1.0	μA	⑦
Lx SW "Pch" ON Resistance	R_{LXP}	$V_{BAT}=V_{Lx}$= 6.0V, I_{OUT}=200mA	-	0.3(*2)	-	Ω	④
Lx SW "Nch" ON Resistance	R_{LXN}		-	0.3(*3)	-	Ω	①
Lx SW"H" Leakage Current	I_{LXLH}	V_{BAT}=6.0,V_{CE}=0V, V_{Lx}=6.0V,V_{OUT}=0V	-	0	1.0	μA	⑦
Current Limit	I_{LIM}	$V_{BAT}=V_{OUT(T)}$-0.2V, R_{Lx}=1Ω	<E-6>	<E-7>	<E-8>	A	⑥
Integral Latch Time	t_{LAT}	$V_{BAT}=V_{OUT(T)}$-0.2V, R_{Lx}=1Ω, Time from current limit start to stop Lx oscillation	25	100	365	μs	⑥
Latch Release Voltage	V_{LAT_R}	R_L is selected with $V_{OUT(T)}$, Refer to Table 1	0.9	1.2	1.5	V	①
Short Protection Threshold Voltage	V_{SHORT}	$V_{BAT}=V_{OUT(T)}$-0.2V, R_L=1Ω	-	(*3)	-	V	①
Soft-Start Time	t_{SS}	$V_{BAT}=V_{OUT(T)}\times0.6$, $V_{OUT}=V_{OUT(T)}\times0.9$, After "H" is fed to CE, the time by when clocks are generated at Lx pin.	0.2	0.5	1.0	ms	⑤
C_L Discharge Resistance (Type D only)	R_{DCHG}	V_{BAT}=3.3V, V_{OUT}=3.3V, V_{CE}=0V	100	180	400	Ω	②
Bypass SW Resistance (Type E only)	R_{BSW}	V_{BAT}= 3.3V, V_{OUT}=0V, V_{CE}=0V	100	180	400	Ω	②
CE "H" Voltage	V_{CEH}	$V_{OUT}=V_{OUT(T)}$-0.15V, Applied voltage to V_{CE}, Voltage changes Lx to be generated.	0.8	-	6.0	V	⑤
CE "L" Voltage	V_{CEL}	$V_{OUT}=V_{OUT(T)}$-0.15V, Applied voltage to V_{CE}, Voltage changes Lx to"H" level	GND	-	0.2	V	⑤
CE "H" Current	I_{CEH}	V_{BAT}=6.0V,V_{OUT}=6.0V, V_{Lx}=6.0V V_{CE}=6.0V,	-0.1	-	0.1	μA	②
CE "L" Current	I_{CEL}	V_{BAT}=6.0V,V_{OUT}=6.0V, V_{Lx}=6.0V ,V_{CE}=0V	-0.1	-	0.1	μA	②
Inductance	L	Test Freq.=1MHz	-	1.5	-	μH	-
Inductor Rated Current	I_{CEL}	ΔT=+40deg	-	1000	-	mA	-

$V_{OUT(T)}$:Target Voltage

Test Conditions: unless otherwise stated、V_{BAT}=1.5V, V_{CE}=3.3V, Lx:OPEN, R_{Lx}=56Ω

(*1) XCL102D/XCL103D: V_{OUT}=0V, XCL102E/XCL103E: V_{OUT}=OPEN

(*2) Design value for the XCL103D

(*3) Designed value

■ELECTRICAL CHARACTERISTICS (Continued)

Table 1. External Components R_L Table

$V_{OUT(T)}$	R_L
UNITS:V	UNITS:Ω
$2.2 \leqq V_{OUT(T)} < 3.1$	220
$3.1 \leqq V_{OUT(T)} < 4.3$	330
$4.3 \leqq V_{OUT(T)} \leqq 5.5$	470

Table 2. SPEC Table

NOMINAL OUTPUT VOLTAGE	V_{OUT}			I_{DD}	I_{LIM}		
	<E-1>	<E-2>	<E-3>	<E-5>	<E-6>	<E-7>	<E-8>
UNITS	V	V	V	mA	A	A	A
$V_{OUT(T)}$	MIN.	TYP.	MAX.	TYP.	MIN.	TYP.	MAX.
2.2	2.156	2.200	2.244	0.705	-	1.11	2.30
2.3	2.254	2.300	2.346	0.736	-	1.14	2.30
2.4	2.352	2.400	2.448	0.767	-	1.17	2.30
2.5	2.450	2.500	2.550	0.797	-	1.19	2.30
2.6	2.548	2.600	2.652	0.828	-	1.22	2.30
2.7	2.646	2.700	2.754	0.858	-	1.24	2.30
2.8	2.744	2.800	2.856	0.889	-	1.26	2.30
2.9	2.842	2.900	2.958	0.919	-	1.28	2.30
3.0	2.940	3.000	3.060	0.950	0.96	1.30	2.30
3.1	3.038	3.100	3.162	0.981	0.97	1.30	2.30
3.2	3.136	3.200	3.264	1.011	0.97	1.30	2.30
3.3	3.234	3.300	3.366	1.042	0.98	1.30	2.30
3.4	3.332	3.400	3.468	1.072	0.98	1.30	2.30
3.5	3.430	3.500	3.570	1.103	0.99	1.30	2.30
3.6	3.528	3.600	3.672	1.134	0.99	1.30	2.30
3.7	3.626	3.700	3.774	1.164	1.00	1.30	2.30
3.8	3.724	3.800	3.876	1.195	1.00	1.30	2.30
3.9	3.822	3.900	3.978	1.225	1.01	1.30	2.30
4.0	3.920	4.000	4.080	1.256	1.01	1.30	2.30
4.1	4.018	4.100	4.182	1.286	1.02	1.30	2.30
4.2	4.116	4.200	4.284	1.317	1.02	1.30	2.30
4.3	4.214	4.300	4.386	1.348	1.03	1.30	2.30
4.4	4.312	4.400	4.488	1.378	1.03	1.30	2.30
4.5	4.410	4.500	4.590	1.409	1.04	1.30	2.30
4.6	4.508	4.600	4.692	1.439	1.04	1.30	2.30
4.7	4.606	4.700	4.794	1.470	1.05	1.30	2.30
4.8	4.704	4.800	4.896	1.501	1.06	1.30	2.30
4.9	4.802	4.900	4.998	1.531	1.06	1.30	2.30
5.0	4.900	5.000	5.100	1.562	1.07	1.30	2.30
5.1	4.998	5.100	5.202	1.592	1.07	1.30	2.30
5.2	5.096	5.200	5.304	1.623	1.08	1.30	2.30
5.3	5.194	5.300	5.406	1.653	1.08	1.30	2.30
5.4	5.292	5.400	5.508	1.684	1.09	1.30	2.30
5.5	5.390	5.500	5.610	1.715	1.09	1.30	2.30

■TEST CIRCUIT

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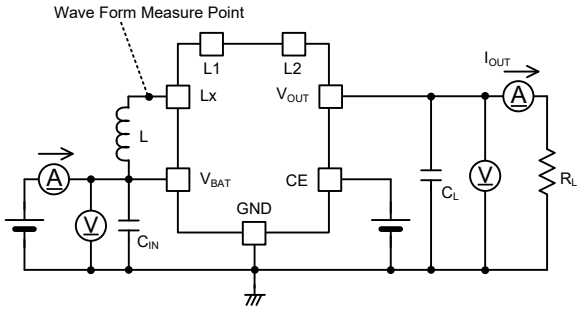

※External Components
C_{IN} : 10μF(ceramic)
C_L : 10μF(ceramic)
L : 1.5μH(selected inductor)

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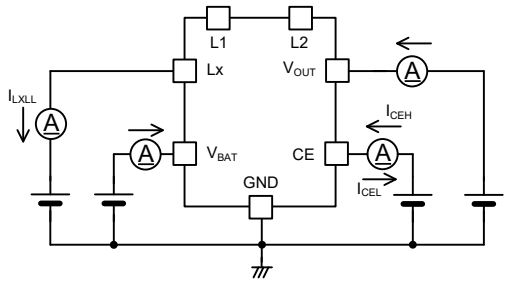

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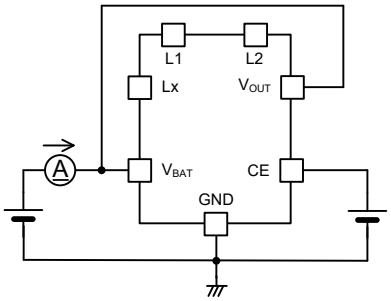

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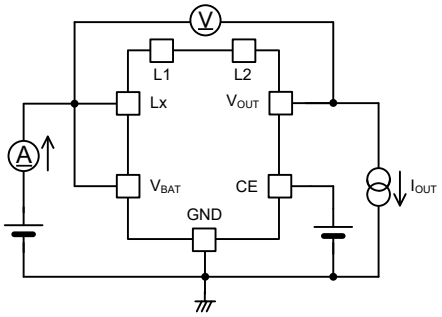

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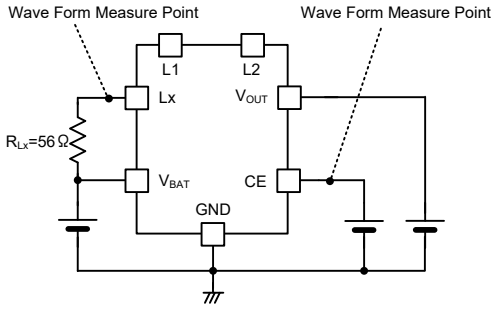

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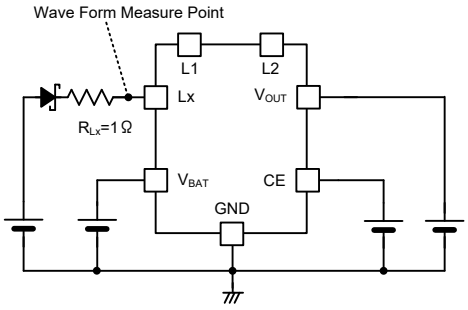

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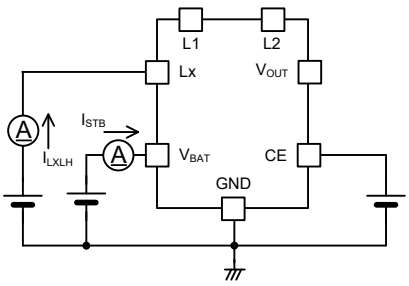
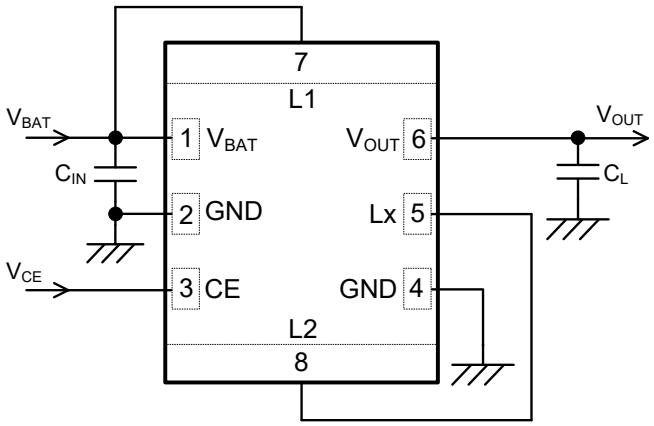


■TYPICAL APPLICATION CIRCUIT



【Typical Examples】

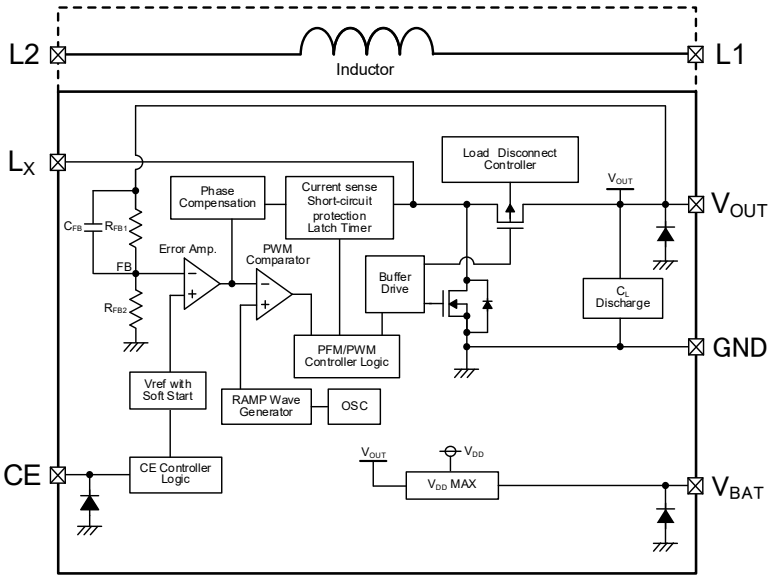
	MANUFACTURER	PRODUCT NUMBER	VALUE
C_{IN}	Taiyo Yuden	LMK107BBJ106MALT	10V/10uF
	Taiyo Yuden	TMK107BBJ106MA-T	25V/10uF
	TDK	C1608X5R0J106MT0A0E	6.3V/10uF
	TDK	C1608X5R1A106M	10V/10uF
C_L (*1)	Taiyo Yuden	TMK107BBJ106MA-T	25V/10uF
	TDK	C1608X5R0J106MT0A0E	6.3V/10uF

* Select components appropriate to the usage conditions (ambient temperature, input & output voltage).
While selecting a part, please concern about capacitance reduction and voltage durability.

(*1) If $V_{BAT} \geqq 2V$, $V_{OUT(T)} \geqq 3.5V$ and the load current rises above 200mA, use two or more in a parallel connection.
For the actual load capacitance, use a ceramic capacitor that ensures a capacitance equivalent to or greater than the TMK107BBJ106MA-T (Taiyo Yuden).
If using tantalum or low ESR electrolytic capacitors please be aware that ripple voltage will be higher due to the larger ESR (Equivalent Series Resistance) values of those types of capacitors. Please also note that the IC's operation may become unstable with such capacitors so that we recommend to test on the board before usage.

■OPERATIONAL EXPLANATION

The XCL102/XCL103 series consists of a reference voltage source, ramp wave circuit, error amplifier, PWM comparator, phase compensation circuit, N-channel driver transistor, P-channel synchronous rectification switching transistor and current limiter circuit.



< BLOCK DIAGRAM (D type) >

The error amplifier compares the internal reference voltage with the resistors RFB1 and RFB2. Phase compensation is performed on the resulting error amplifier output, to input a signal to the PWM comparator to determine the turn-on time of the N-channel driver transistor during PWM operation. The PWM comparator compares, in terms of voltage level, the signal from the error amplifier with the ramp wave from the ramp wave circuit and delivers the resulting output to the buffer driver circuit to cause the Lx pin to output a switching duty cycle. This process is continuously performed to ensure stable output voltage.

The current feedback circuit monitors the N-channel driver transistor's turn-on current for each switching operation and modulates the error amplifier output signal to provide multiple feedback signals. This enables a stable feedback loop even when a low ESR capacitor, such as a ceramic capacitor, is used, ensuring stable output voltage.

<Reference voltage source, soft start function>

The reference voltage forms a reference that is used to stabilize the output voltage of the IC.

After "H" level is fed to CE pin, the reference voltage connected to the error amp increases linearly during the soft start interval. This allows the voltage divided by the internal RFB1 and RFB2 resistors and the reference voltage to be controlled in a balanced manner, and the output voltage rises in proportion to the rise in the reference voltage. This operation prevents rush input current and enables the output voltage to rise smoothly.

<Ramp Wave Circuit>

The ramp wave circuit determines switching frequency. The frequency is fixed internally at 3.0MHz. The Clock generated is used to produce ramp waveforms needed for PWM operation, and to synchronize all the internal circuits.

<Error Amplifier>

The error amplifier is designed to monitor output voltage. The amplifier compares the reference voltage with the feedback voltage divided by the internal resistors (RFB1 and RFB2). When the FB is lower than the reference voltage, output voltage of the error amplifier increases. The gain and frequency characteristics of the error amplifier are optimized internally.

<V_{DDMAX}>

$V_{DD\ MAX}$ circuit compares the input voltage and the output voltage then it will select the higher one as the power supply for the IC.

<Shutdown function, load disconnection function>

The IC enters chip disable state by applying low level voltage to the CE pin. At this time, the N-channel and P-channel synchronous switching transistors are turned OFF

With the XCL102D/103D types, the orientation of the parasitic diode of the P-channel synchronous switching transistor is fixed at anode: V_{OUT} and cathode: Lx during shutdown to break conduction from the input side to the output side by the parasitic diode of the P-channel synchronous switching transistor.

<PWM/PFM control circuit>

When PFM operates, the N-channel driver transistor turns on at the timing of the signal sent from the PWM comparator. The N-channel driver transistor remains on until the current in the coil reaches a constant current (I_{PFM}). The PWM/PFM control circuit compares the signal sent from the PWM comparator to the time it takes the current in the coil to reach a constant current (I_{PFM}), and outputs the pulse that results in a longer on-time of the N-channel driver transistor. This enables smooth switching between PWM and PFM. The XCL102 series directly outputs the signal that is sent from the PWM comparator.

■OPERATIONAL EXPLANATION (Continued)

<Maximum current limit function, short-circuit protection>

The maximum current limit function of XCL102D/E and XCL103D/E types monitors the current that flows in the Nch driver transistor connected to the Lx pin and consists of both maximum current limiting and a latch function. (Fig.1)
Short-circuit protection (V_{SHORT}) is a latch-stop function that activates when the output voltage drops below the short-circuit protection threshold voltage in the overcurrent state. (Fig.2)

① If the current flowing in the Nch (I_{LIM}) driver transistor exceeds the current limit value (equivalent to the peak coil current), the Nch driver transistor turns off, and remains off during the clock interval. In addition, an integral latch timer starts the count.
② The N-channel driver transistor turns on at the next pulse. If in the overcurrent state at this time, the Nch driver transistor turns off as in (1). The integral latch timer continues the count.
③ If the count of the integral latch timer continues for 100µs (t_{LAT} Typ.), a function that latches the Nch driver transistor and Pch synchronous switching transistor to the off state activates.
④ If no longer in the overcurrent state at the next pulse, normal operation resumes. The integral latch timer stops the count.

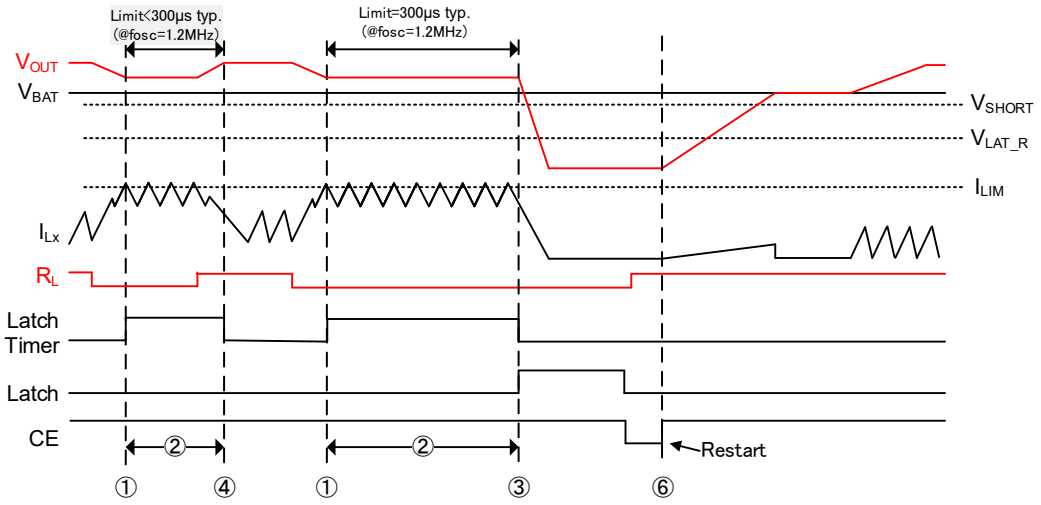


Fig. 1

⑤ If the output voltage V_{OUT} drops below the short-circuit protection threshold voltage V_{SHORT} during the count of the integral latch timer, a function that latches the Nch driver transistor and Pch synchronous switching transistor in the off state activates. The short-circuit protection threshold voltage V_{SHORT} is a threshold voltage that is linked to the input voltage V_{BAT}.
⑥ In the latched state, either restart by shutting down once with the CE pin, or resume operation by lowering the input voltage V_{BAT} below the latch release voltage V_{LAT_R}(1.2V typ.). The soft start function operates during restart. During the soft-start interval t_{SS}, the integral latch timer and latch function are stopped.
⑦ When the input voltage V_{BAT} is below the latch release voltage V_{LAT_R}(1.2V typ.), the integral latch timer and latch function stop, but the current limiting function continues operating.
⑧

* Note that the current in the internal Nch driver transistor is not the same as the output current I_{OUT}.

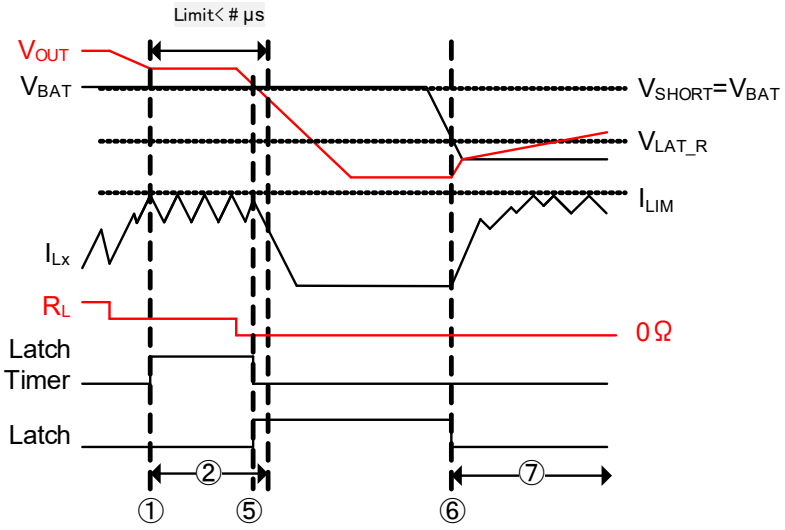


Fig. 2

■OPERATIONAL EXPLANATION (Continued)

<Bypass switch>

At shutdown, XCL102E type and XCL103E type conduct between the BAT pin and V_{OUT} pin by means of a bypass switch. If the output is shorted to ground, the current is limited by the resistance (R_{BSW}) of the bypass switch.

<C_L Discharge>

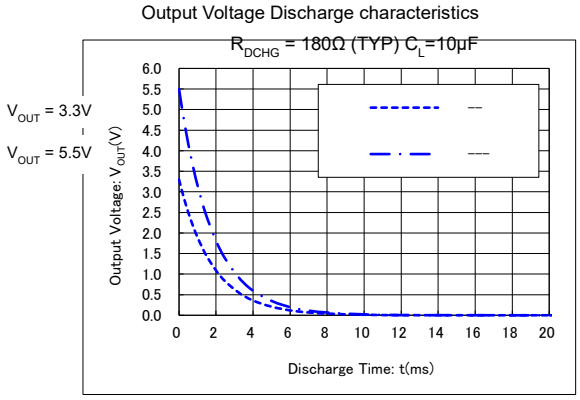
The XCL102D and XCL103D can discharge the electric charge at the output capacitor (C_L) when a low signal to the CE pin which enables a whole IC circuit put into OFF state, is inputted via the N-channel transistor located between the V_{OUT} pin and the GND pin.

When the IC is disabled, electric charge at the output capacitor (C_L) is quickly discharged so that it may avoid application malfunction. Discharge time of the output capacitor (C_L) is set by the C_L auto-discharge resistance (R) and the output capacitor (C_L). By setting time constant of a C_L auto-discharge resistance value [R_{DCHG}] and an output capacitor value (C_L) as τ(τ= C_L x R_{DCHG}), discharge time of the output voltage after discharge via the N channel transistor is calculated by the following formulas.

However, the C_L discharge resistance [R_{DCHG}] is depends on the V_{BAT} or V_{OUT}, so it is difficult to make sure the discharge time. We recommend that you fully check actual performance.

$$V = V_{OUT} \times e^{-t/\tau} \quad or \quad t = \tau \times \ln(V_{OUT}/V)$$

V	: Output voltage after discharge
$V_{OUT(T)}$	: Target voltage
t	: Discharge time
τ	: $C_L \times R_{DCHG}$
C_L	: Capacitance of Output capacitor (C_L)
R_{DCHG}	: C_L Discharge resistance, it depends on supply voltage



■NOTE ON USE

1) For the phenomenon of temporal and transitional voltage decrease or voltage increase, the IC may be damaged or deteriorated if IC is used beyond the absolute maximum ratings.

2) Spike noise and ripple voltage arise in a switching regulator as with a DC/DC converter. These are greatly influenced by external component selection, such as the capacitance values, and board layout of external components. Once the design has been completed, verification with actual components should be done.

3) The DC/DC converter performance is greatly influenced by not only the ICs' characteristics, but also by those of the external components. Care must be taken when selecting the external components. Especially for C_L load capacitor, it is recommended to use type B capacitors (JIS regulation) or X7R, X5R capacitors (EIA regulation).

4) Use a ground wire of sufficient strength. Ground potential fluctuation caused by the ground current during switching could cause the IC operation to become unstable, so reinforce the area around the GND pin of the IC in particular.

5) Please mount each external component as close to the IC as possible. Also, please make traces thick and short to reduce the circuit impedance.

6) With regard to the current limiting value (I_{LIM}), the actual coil current may at times exceed the electrical characteristics due to propagation delay inside the product.

7) The CE pin is a CMOS input pin. Do not use with the pin open. If connecting to the BAT pin or ground pin, use the resistor which is 1MΩ or less. To prevent malfunctioning of the device connected to this product or the input/output due to short circuiting between pins, it is recommended that a resistor be connected.

8) The maximum current limiter controls the limit of the N-channel driver transistor by monitoring current flow. This function does not limit the current flow of the P-channel synchronous transistor. When used with the condition $V_{BAT} > V_{OUT}$ (input voltage higher than the output voltage), the IC may be destroyed if overcurrent flows to the P-channel synchronous switching transistor due to short-circuiting of the load or other reason.

9) When the device is used in high step-up ratio, the current limit function may not work during excessive load current. In this case, the maximum duty cycle limits maximum current. In this event, latching may not take place, because the maximum current limit cannot be detected.

10) On latch types, some board conditions may cause release from the maximum current limit, and the integrated latch time may become longer or latching may not take place.

11) On latch type, the maximum current limit may be detected, and this will cause the latch function to activate and stop operation after the soft start time elapses. In particular, note that the soft start time becomes shorter when the IC is used at high temperatures.

12) When the step-up voltage difference is small, the XCL102 series for PWM control may oscillate intermittently.

13) When the voltage boost difference is small, the current limiting function may not operate if the on time of the N-channel driver transistor is shorter than the propagation delay time of the current limit circuit. In this case, latching may not take place on a latch type because the maximum current limit is not detected.

14) $V_{BAT} > V_{OUT}$, The case and Pch synchronous rectification switch Tr used in (input voltage more expensive than the output voltage). But the output voltage will be on and becomes equal to input voltage.

15) When connecting large-volume condenser (100μF) etc. to the loading capacity, a protection circuit of IC moves, and the output voltage doesn't stand up.

16) When input voltage and output voltage are low, integral latch function and short-circuit protection may not operate.
We recommend that you fully check actual performance.

17) TOREX places an importance on improving our products and its reliability. However, by any possibility, we would request user fail-safe design and post-aging treatment on system or equipment.

■NOTE ON USE(Continued)

18) Since this IC is a coil-integrated product, do not mount it in an environment with a strong magnetic field such as near a magnet. The influence of a strong magnetic field may cause a decrease in inductance value, deterioration of efficiency, and malfunction of the IC.

19) Instructions of pattern layouts

The operation may become unstable due to noise and/or phase lag from the output current when the wire impedance is high, please place the input capacitor(C_{IN}) and the output capacitor (C_L) as close to the IC as possible.

(1) In order to stabilize V_{BAT} voltage level, we recommend that a by-pass capacitor (C_{IN}) be connected as close as possible to the V_{BAT} pin, GND pin.

(2) Please mount each external component as close to the IC as possible.

(3) Wire external components as close to the IC as possible and use thick, short connecting traces to reduce the circuit impedance.

(4) Make sure that the GND traces are as thick as possible, as variations in ground potential caused by high ground currents at the time of switching may result in instability of the IC.

(5) This series' internal driver transistors bring on heat because of the output current and ON resistance of P-channel and N-channel MOS driver transistors. Please consider the countermeasures against heat if necessary.

20) Please make the equipped location accuracy within the 0.05mm as a careful point on the mounting.

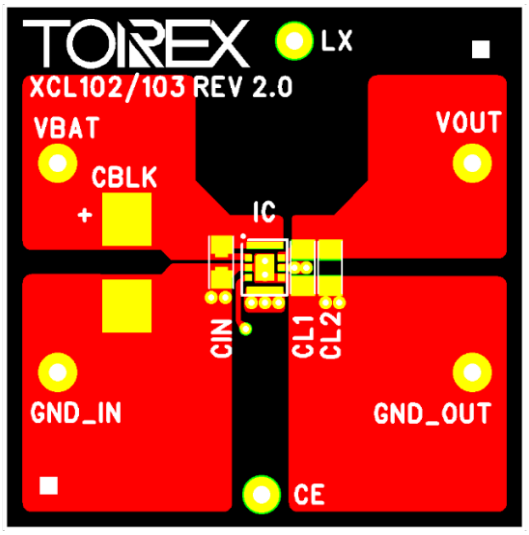
21) The proper position of mounting is based on the coil terminal

22) Appearance (Coil)

1. Coils are compliant with general surface mount type chip coil (inductor) specifications and may have scratches, flux contamination and the like.

<Reference pattern layout>

< Layer 1 >



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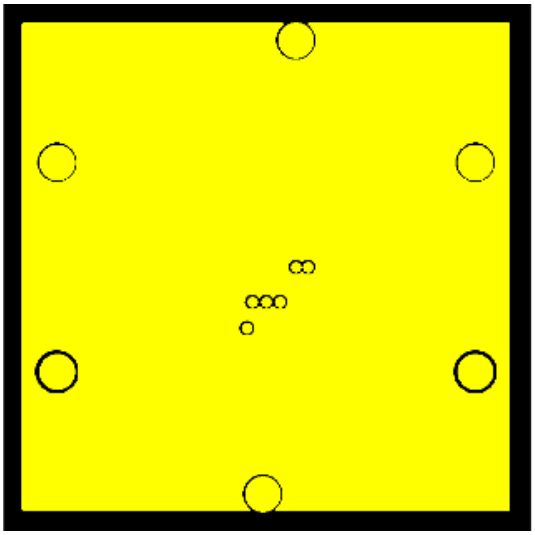

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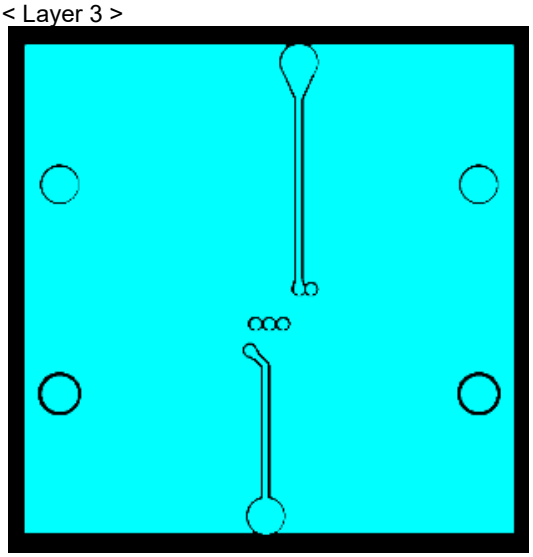

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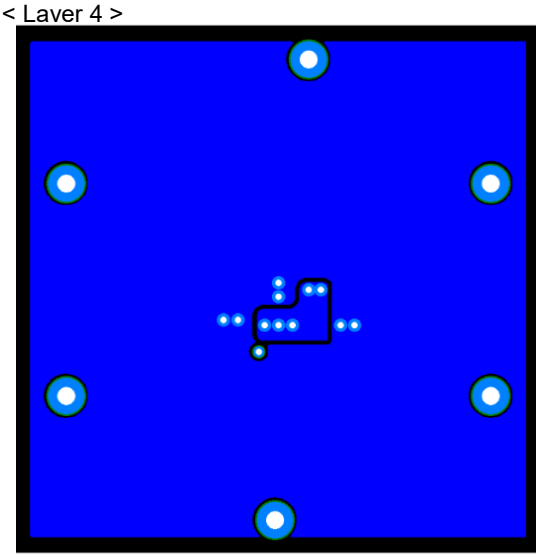
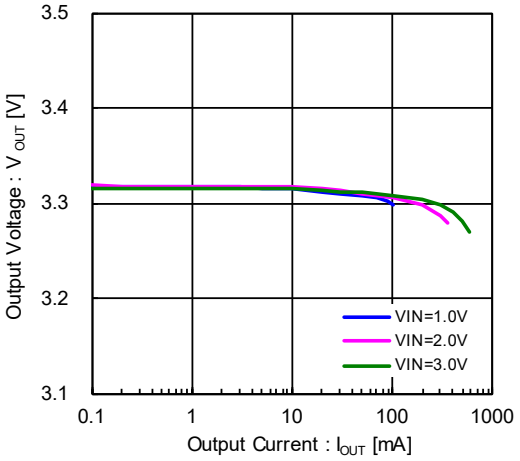


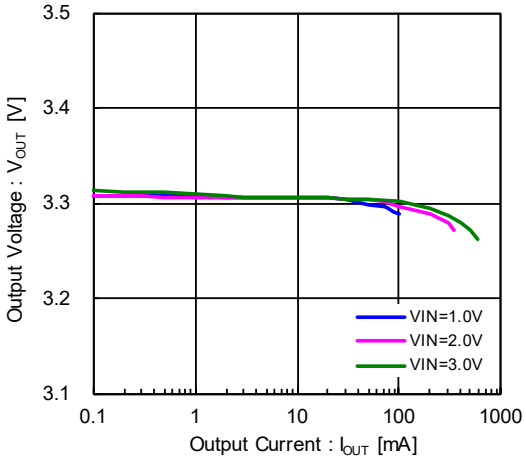
■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Output Voltage vs Output Current

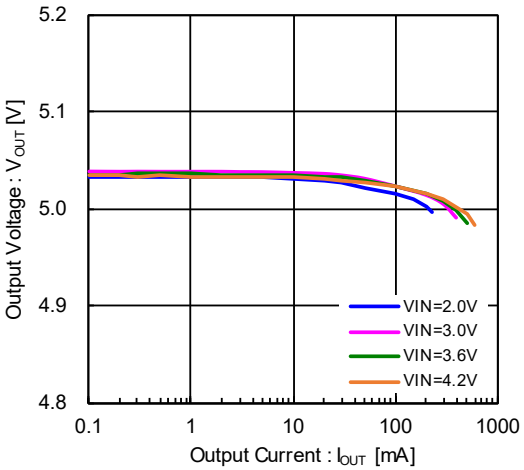
XCL102D333CR-G/XCL102E333CR-G



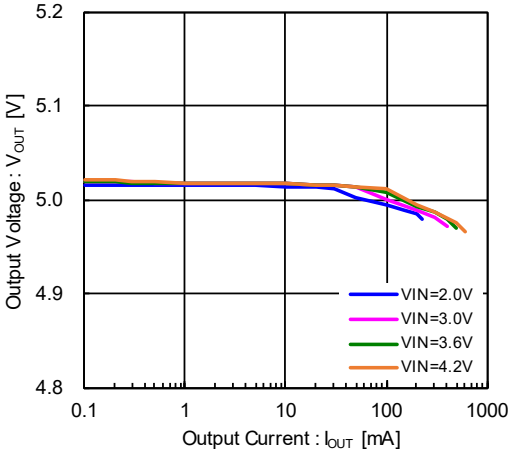
XCL103D333CR-G/XCL103E333CR-G



XCL102D503CR-G/XCL102E503CR-G

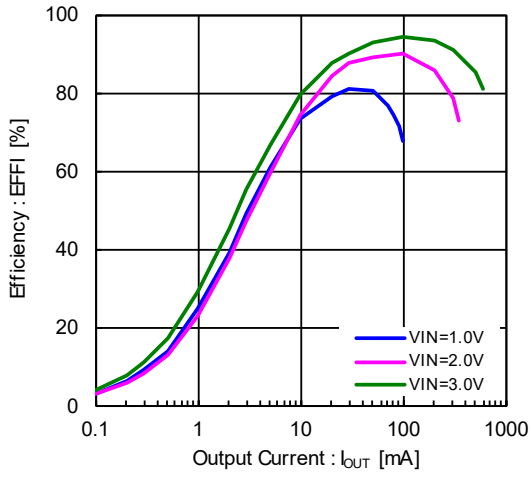


XCL103D503CR-G/XCL103E503CR-G

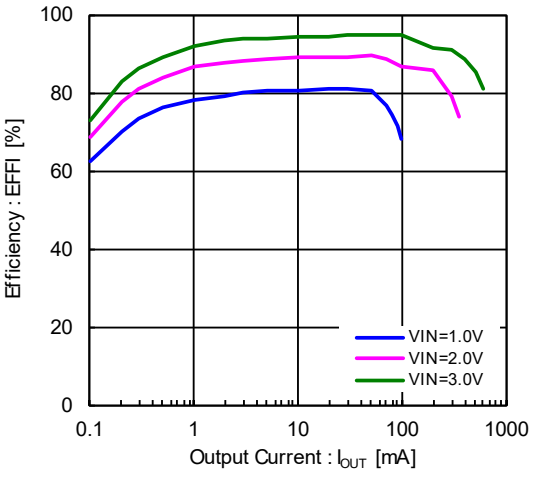


(2) Efficiency vs Output Current

XCL102D333CR-G/XCL102E333CR-G



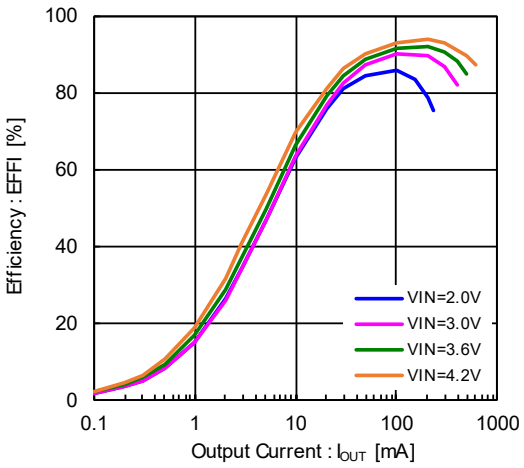
XCL103D333CR-G/XCL103E333CR-G



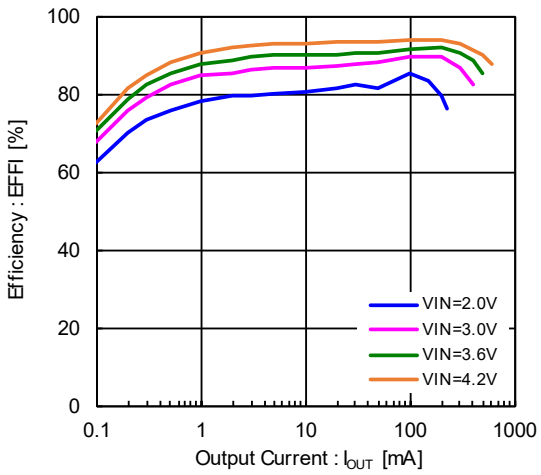
■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

(2) Efficiency vs Output Current

XCL102D503CR-G/XCL102E503CR-G

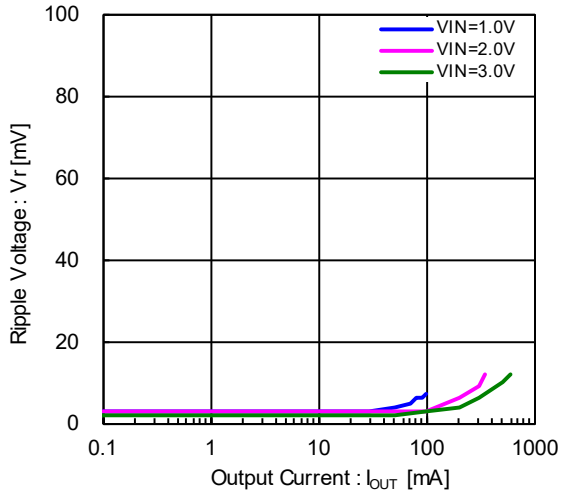


XCL103D503CR-G/XCL103E503CR-G

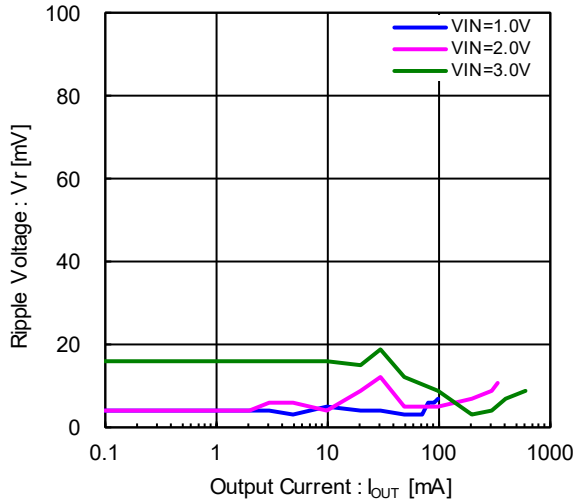


(3) Ripple Voltage vs Output Current

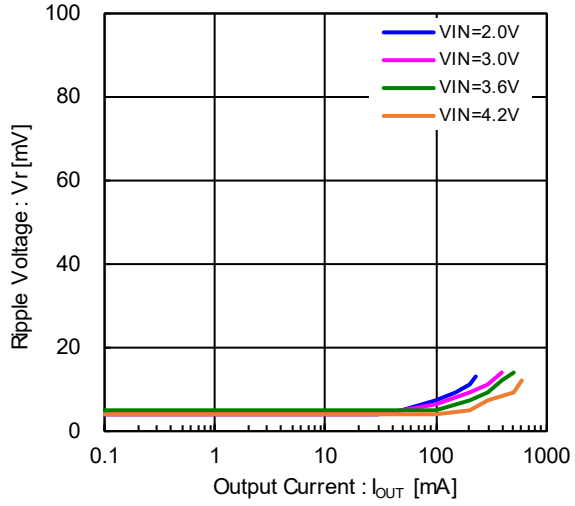
XCL102D333CR-G/XCL102E333CR-G



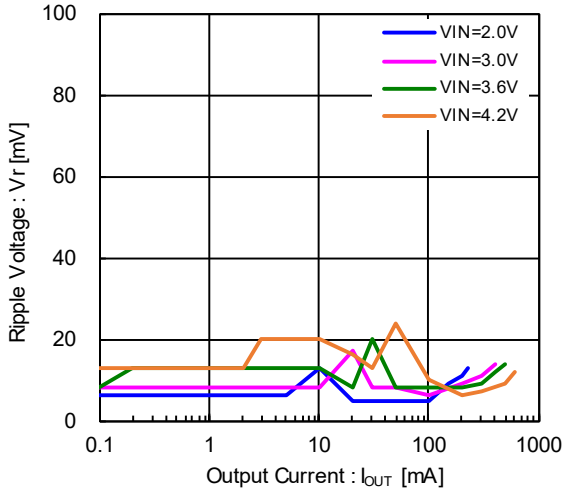
XCL103D333CR-G/XCL103E333CR-G



XCL102D503CR-G/XCL102E503CR-G



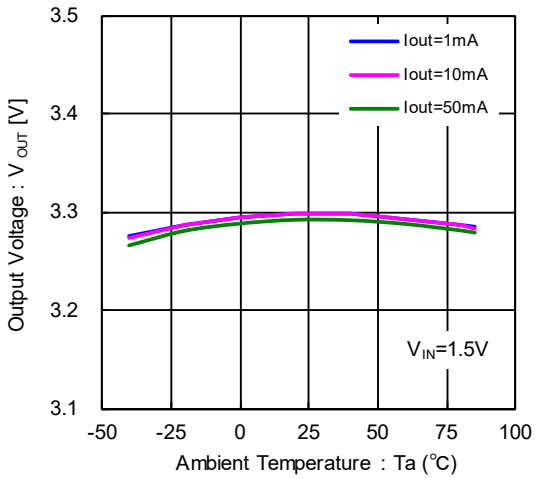
XCL103D503CR-G/XCL103E503CR-G



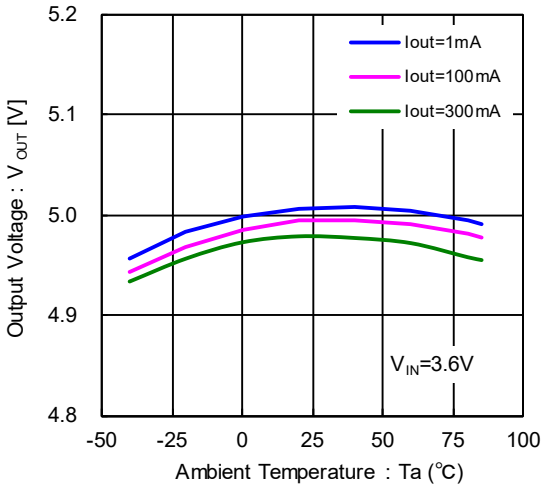
■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

(4) Output Voltage vs Ambient Temperature

XCL102D333CR-G/XCL102E333CR-G

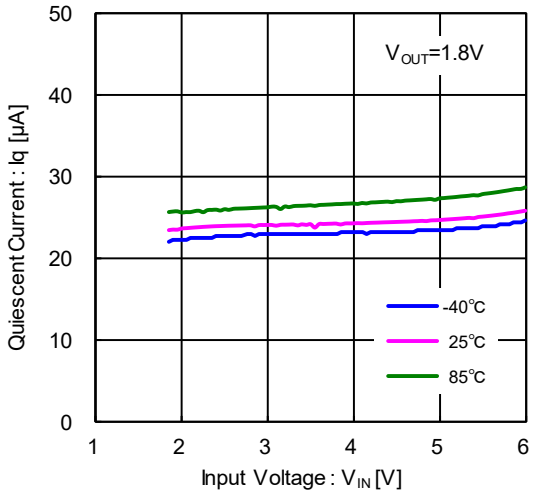


XCL102D503CR-G/XCL102E503CR-G



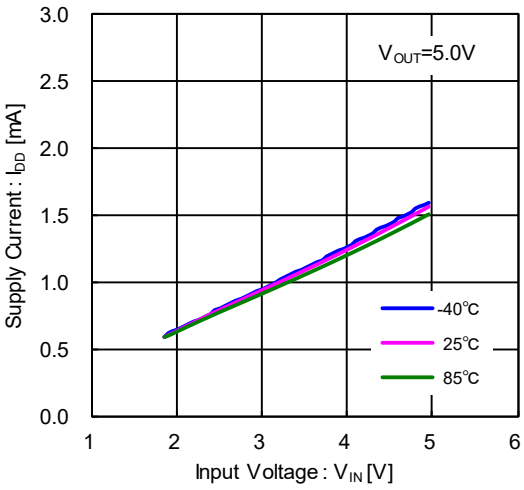
(5) Quiescent Current vs. Input Voltage

XCL103D183CR-G/XCL103E183CR-G



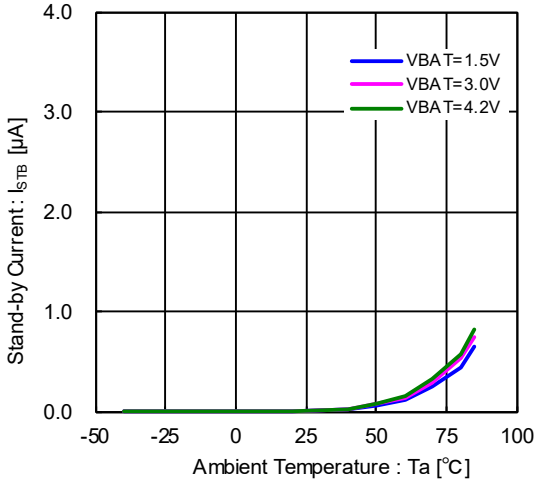
(6) Supply Current vs. Input Voltage

XCL103D503CR-G/XCL103E503CR-G



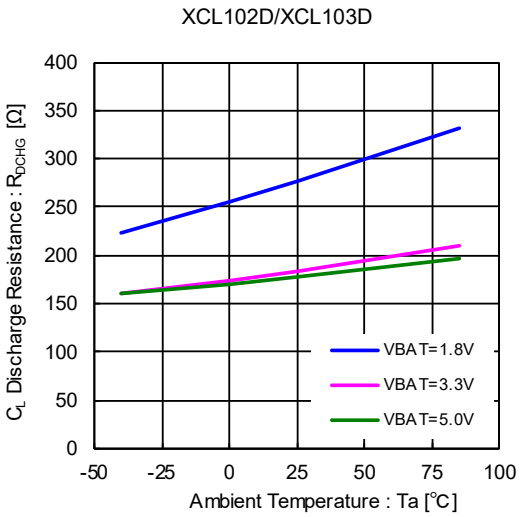
(7) Stand-by Current vs. Ambient Temperature

XCL102/XCL103

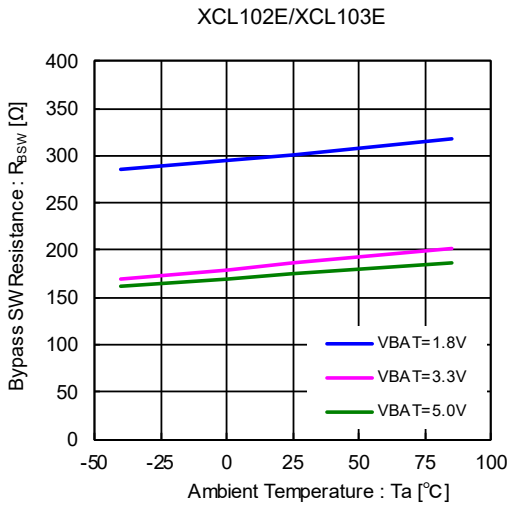


■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

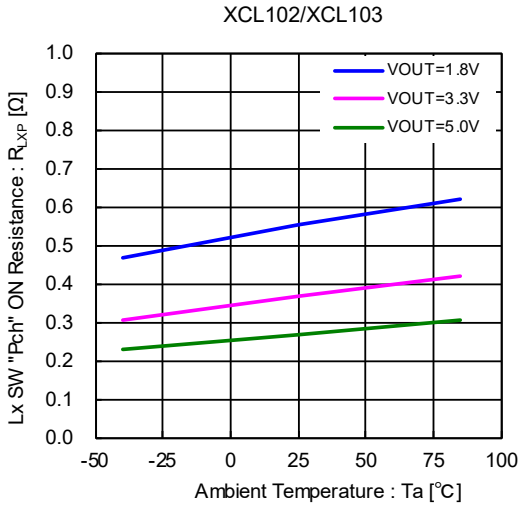
(8) CL Discharge Resistance vs. Ambient Temperature



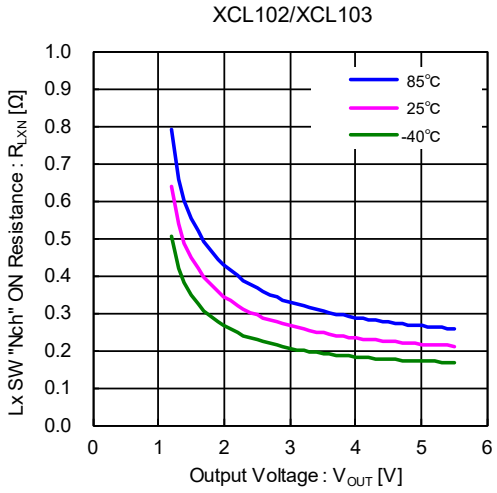
(9) Bypass SW Resistance vs. Ambient



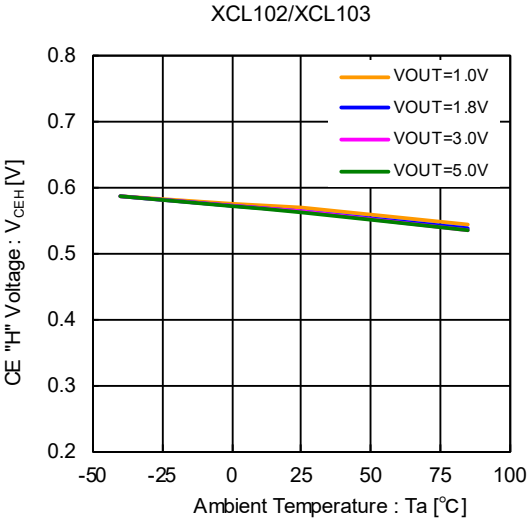
(10) Lx SW "Pch" ON Resistance vs. Ambient Temperature



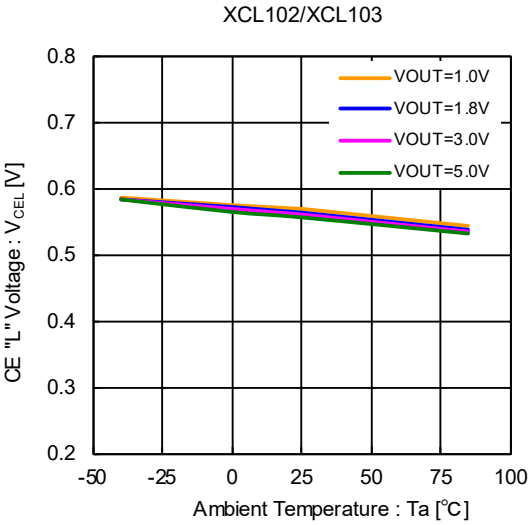
(11) Lx SW "Nch" ON Resistance vs. Output Voltage



(12) CE "H" Voltage vs. Ambient Temperature



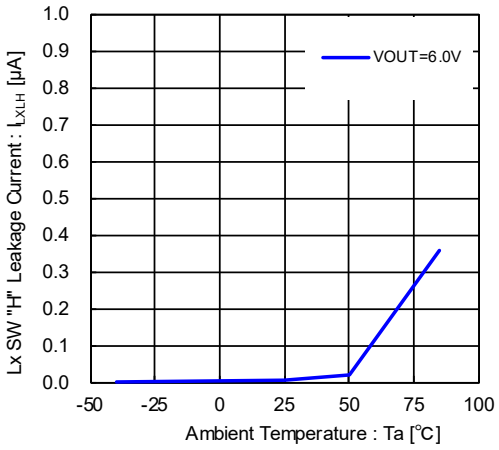
(13) CE "L" Voltage vs. Ambient Temperature



■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

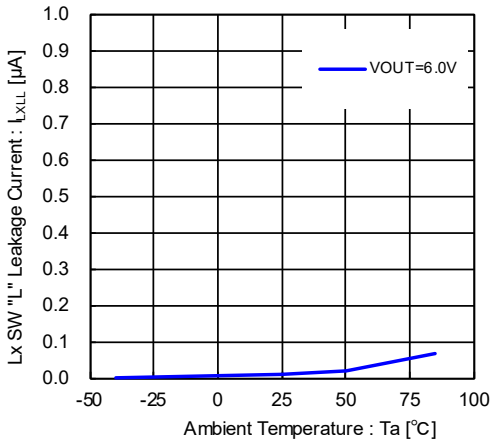
(14) Lx SW "H" Leakage Current vs. Ambient temperature

XCL102/XCL103

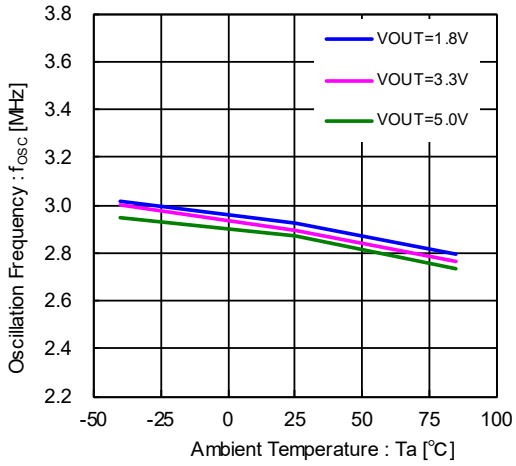


(15) Lx SW "L" Leakage Current vs. Ambient temperature

XCL102/XCL103

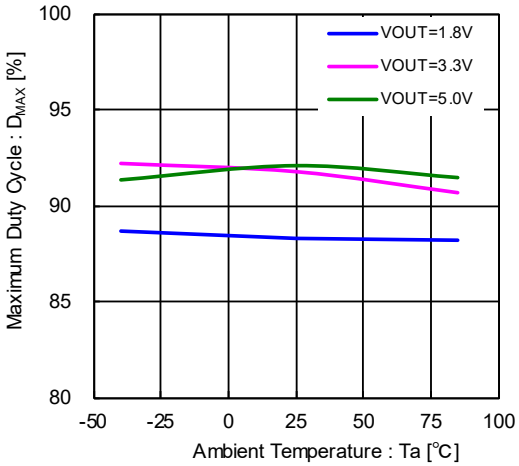


(16) Oscillation Frequency vs. Ambient temperature

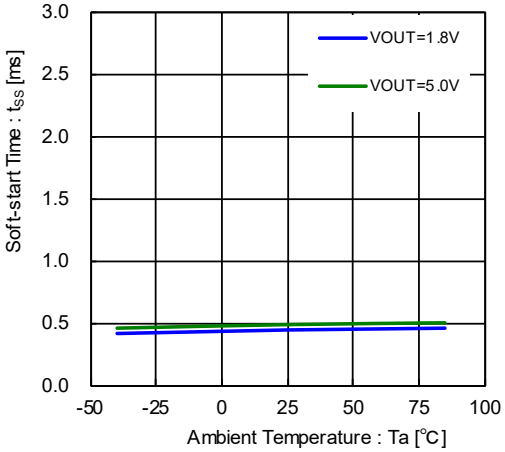


(17) Maximum Duty Cycle vs. Ambient temperature

XCL102/XCL103



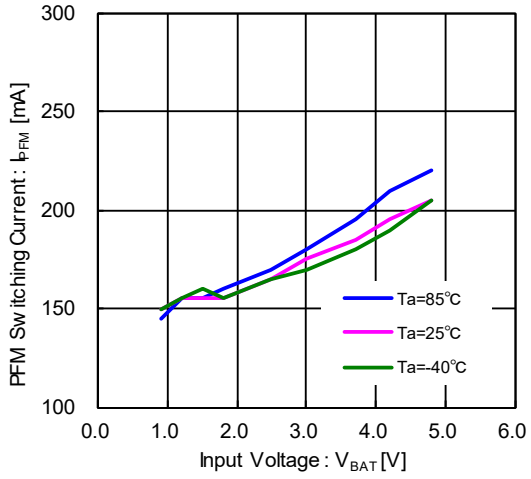
(18) Soft-Start Time vs. Ambient temperature



■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

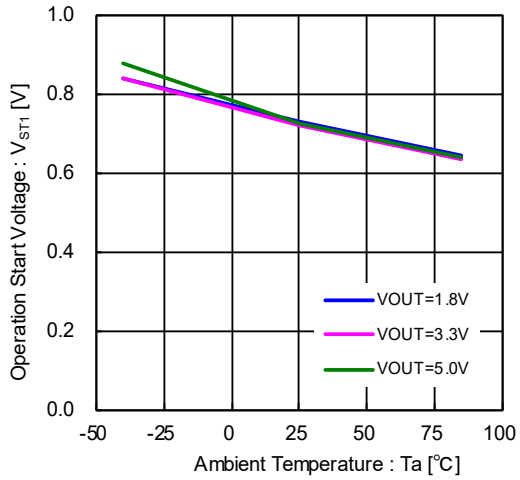
(19) PFM Switching Current vs. Input Voltage

XCL102D/XCL103D

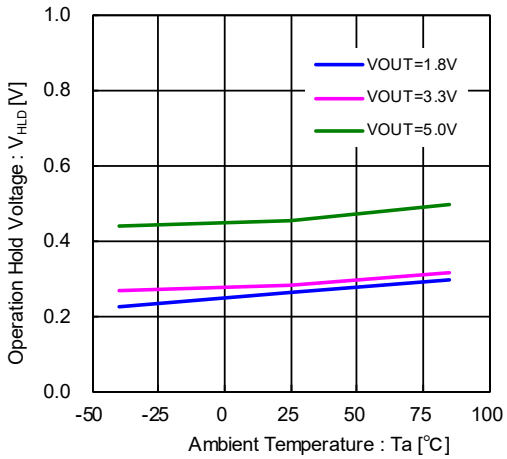


(20) Operation Start Voltage vs. Ambient temperature

XCL102/XCL103

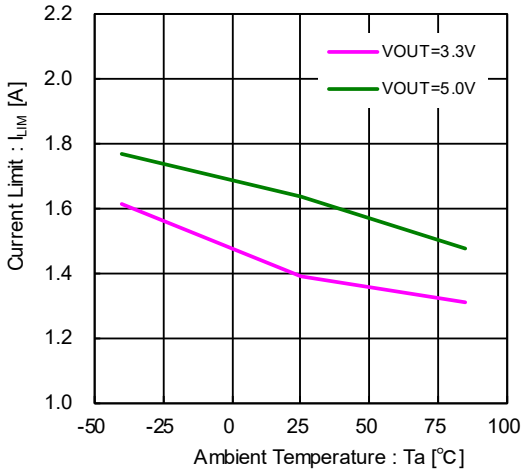


(21) Operation Hold Voltage vs. Ambient temperature



(22) Current Limit vs. Ambient temperature

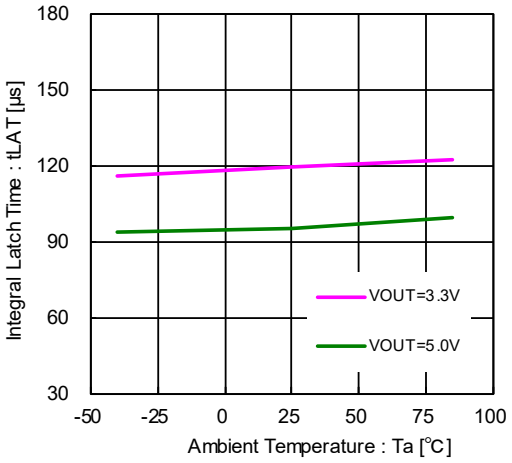
XCL102/XCL103



■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

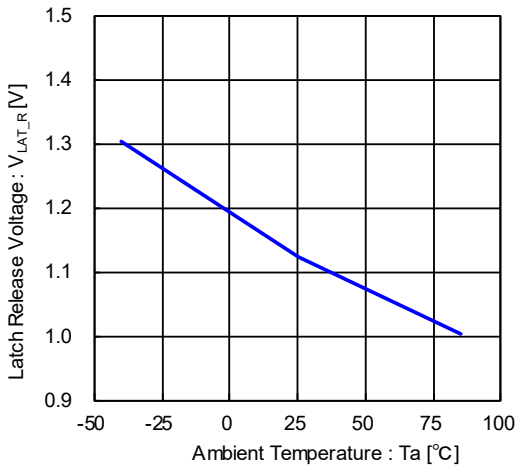
(23) Integral Latch Time vs. Ambient temperature

XCL102/XCL103



(24) Latch Release Voltage vs. Ambient temperature

XCL102/XCL103



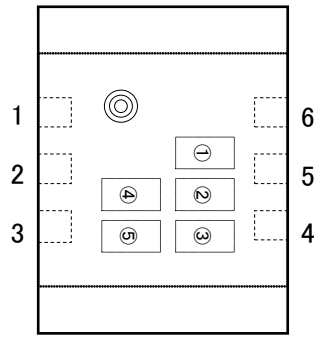
■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
CL-2025-02	CL-2025-02 PKG	CL-2025-02 Power Dissipation

■MARKING RULE

●CL-2025-02



① represents products series

MARK	PRODUCT SERIES
2	XCL102******-G
3	XCL103******-G

② represents integer and oscillation frequency of the output voltage

MARK	Type	OUTPUT VOLTAGE(V)	Oscillation Frequency(MHz)	PRODUCT SERIES
2	D	2.x	3.0	XCL102/3D2*3**-G
3		3.x		XCL102/3D3*3**-G
4		4.x		XCL102/3D4*3**-G
5		5.x		XCL102/3D5*3**-G
C	E	2.x	3.0	XCL102/3E2*3**-G
D		3.x		XCL102/3E3*3**-G
E		4.x		XCL102/3E4*3**-G
F		5.x		XCL102/3E5*3**-G

③ represents the decimal part of output voltage

OUTPUT VOLTAGE(V)	MARK	PRODUCT SERIES
X.0	0	XCL102/3**03**-G
X.1	1	XCL102/3**13**-G
X.2	2	XCL102/3**23**-G
X.3	3	XCL102/3**33**-G
X.4	4	XCL102/3**43**-G
X.5	5	XCL102/3**53**-G
X.6	6	XCL102/3**63**-G
X.7	7	XCL102/3**73**-G
X.8	8	XCL102/3**83**-G
X.9	9	XCL102/3**93**-G

④,⑤ represents production lot number
01～09、0A～0Z、11～9Z、A1～A9、AA～AZ、B1～ZZ in order.
(G, I, J, O, Q, W excluded)
Note: No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

2. The information in this datasheet is intended to illustrate the operation and characteristics of our products. We neither make warranties or representations with respect to the accuracy or completeness of the information contained in this datasheet nor grant any license to any intellectual property rights of ours or any third party concerning with the information in this datasheet.

3. Applicable export control laws and regulations should be complied and the procedures required by such laws and regulations should also be followed, when the product or any information contained in this datasheet is exported.

4. The product is neither intended nor warranted for use in equipment of systems which require extremely high levels of quality and/or reliability and/or a malfunction or failure which may cause loss of human life, bodily injury, serious property damage including but not limited to devices or equipment used in 1) nuclear facilities, 2) aerospace industry, 3) medical facilities, 4) automobile industry and other transportation industry and 5) safety devices and safety equipment to control combustions and explosions. Do not use the product for the above use unless agreed by us in writing in advance.

5. Although we make continuous efforts to improve the quality and reliability of our products; nevertheless Semiconductors are likely to fail with a certain probability. So in order to prevent personal injury and/or property damage resulting from such failure, customers are required to incorporate adequate safety measures in their designs, such as system fail safes, redundancy and fire prevention features.

6. Our products are not designed to be Radiation-resistant.

7. Please use the product listed in this datasheet within the specified ranges.

8. We assume no responsibility for damage or loss due to abnormal use.

9.

TOREX SEMICONDUCTOR LTD.