LOW PHASE NOISE ZERO DELAY BUFFER AND MULTIPLIER ICS670-04

Description

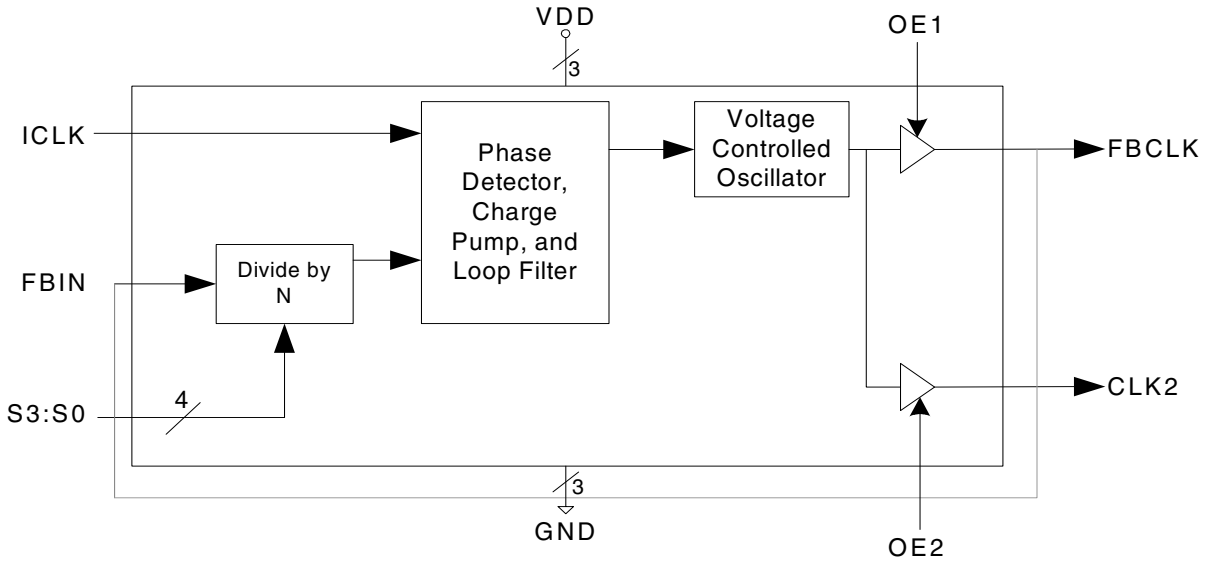
The ICS670-04 is a high speed, low phase noise, Zero Delay Buffer (ZDB) which integrates IDT's proprietary analog/digital Phase Locked Loop (PLL) techniques. It is identical to the ICS670-02, but with an increased maximum output frequency of 210 MHz. There are two identical outputs on the chip. The FBCLK should be used to connect to the FBIN. Each output has its own output enable pin.

The ICS670-04 is ideal for synchronizing outputs in a large variety of systems, from personal computers to data communications to video. By allowing off-chip feedback paths, the chip can eliminate the delay through other devices. The 15 different on-chip multipliers work in a variety of applications. For other multipliers, including functional multipliers, see the ICS527.

Features

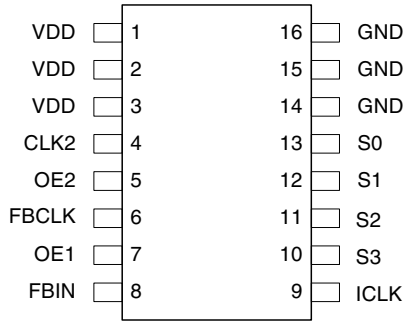
- Packaged in 16-pin SOIC – Pb (lead) free
- Clock inputs from 5 to 210 MHz (see page 2)
- Patented PLL with low phase noise
- Output clocks up to 210 MHz at 3.3 V
- 15 selectable on-chip multipliers
- Power down mode available
- Low phase noise: -111 dBc/Hz at 10 kHz
- Output enable function tri-states outputs
- Low jitter 15 ps one sigma
- Advanced, low power, sub-micron CMOS process
- Operating voltage of 3.3 V or 5 V
- Industrial temperature grade

Block Diagram



External Feedback from FBCLK is recommended.

Pin Assignment



Multiplier Select Table

S3	S2	S1	S0	CLK2 (and FBCLK)	Input Range (MHz)
0	0	0	0	Low (Power down entire chip)	—
0	0	0	1	Input x1.333	18 - 157.5
0	0	1	0	Input x6	5 - 35
0	0	1	1	Input x1.5	16.67 - 140
0	1	0	0	Input x3.333	7.5 - 63
0	1	0	1	Input x2.50	10 - 84
0	1	1	0	Input x4	6 - 52.5
0	1	1	1	Input x1	25 - 210
1	0	0	0	Input x2.333	11 - 90
1	0	0	1	Input x2.666	10 - 78.75
1	0	1	0	Input x12	5 - 17.5
1	0	1	1	Input x3	8 - 70
1	1	0	0	Input x10	5 - 21
1	1	0	1	Input x5	6 - 42
1	1	1	0	Input x8	5 - 26.25
1	1	1	1	Input x2	12 - 105

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1 - 3	VDD	Input	Power supply. Connect both pins to the same voltage (either 3.3 V or 5 V).
4	CLK2	Output	Clock output from VCO. Output frequency equals the input frequency times multiplier.
5	OE2	Input	Output clock enable 2. Tri-states the clock 2 output when low.
6	FBCLK	Output	Clock output from VCO. Output frequency equals the input frequency times multiplier.
7	OE1	Input	Output clock enable 1. Tri-states the feedback clock output when low.
8	FBIN	Input	Feedback clock input.
9	ICLK	Input	Clock input. Connect to a 5 - 210 MHz clock.
10	S3	Input	Multiplier select pin 3. Determines outputs per table above. Internal pull-up.
11	S2	Input	Multiplier select pin 2. Determines outputs per table above. Internal pull-up.
12	S1	Input	Multiplier select pin 1. Determines outputs per table above. Internal pull-up.
13	S0	Input	Multiplier select pin 0. Determines outputs per table above. Internal pull-up.
14 - 16	GND	Power	Connect to ground.

External Components

The ICS670-04 requires a minimum number of external components for proper operation. Tie all VDD pins together, all ground pins together, and connect a 0.01µF decoupling capacitor between them. A series termination resistor of 33Ω must be used on each clock output.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS670-04. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	-40 to +85° C
Storage Temperature	-65 to +150° C
Junction Temperature	150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	° C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=3.3 V ±10%, Ambient temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	No Load		35		mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Short Circuit Current	I_{OS}	Each output		±50		mA
Internal Pull-up Resistor	R_{PU}	OE, select pins		200		kΩ
Input Capacitance	C_{IN}	OE, select pins		5		pF

AC Electrical Characteristics

VDD = 3.3V ±10%, Ambient Temperature -40 to +85° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Clock Frequency	f_{IN}	See table on page 2	5		210	MHz
Output Clock Frequency					210	MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, no load			1.5	ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, no load			1.5	ns
Output Clock Duty Cycle	t_{DC}	measured at VDD/2	45	50	55	%
Input to Output Skew		Note 1		±100		ps
Maximum Absolute Jitter		short term		±45		ps
Maximum Jitter		one sigma		15		ps
Phase Noise, relative to carrier, 125 MHz (x5)		100 Hz offset		-103		dBc/Hz
		1 kHz offset		-117		dBc/Hz
		10 kHz		-111		dBc/Hz
		200 kHz		-88		dBc/Hz

Note 1: Rising edge of ICLK compared with rising edge of CLK2, with FBCLK connected to FBIN, and 15 pF load on CLK2.

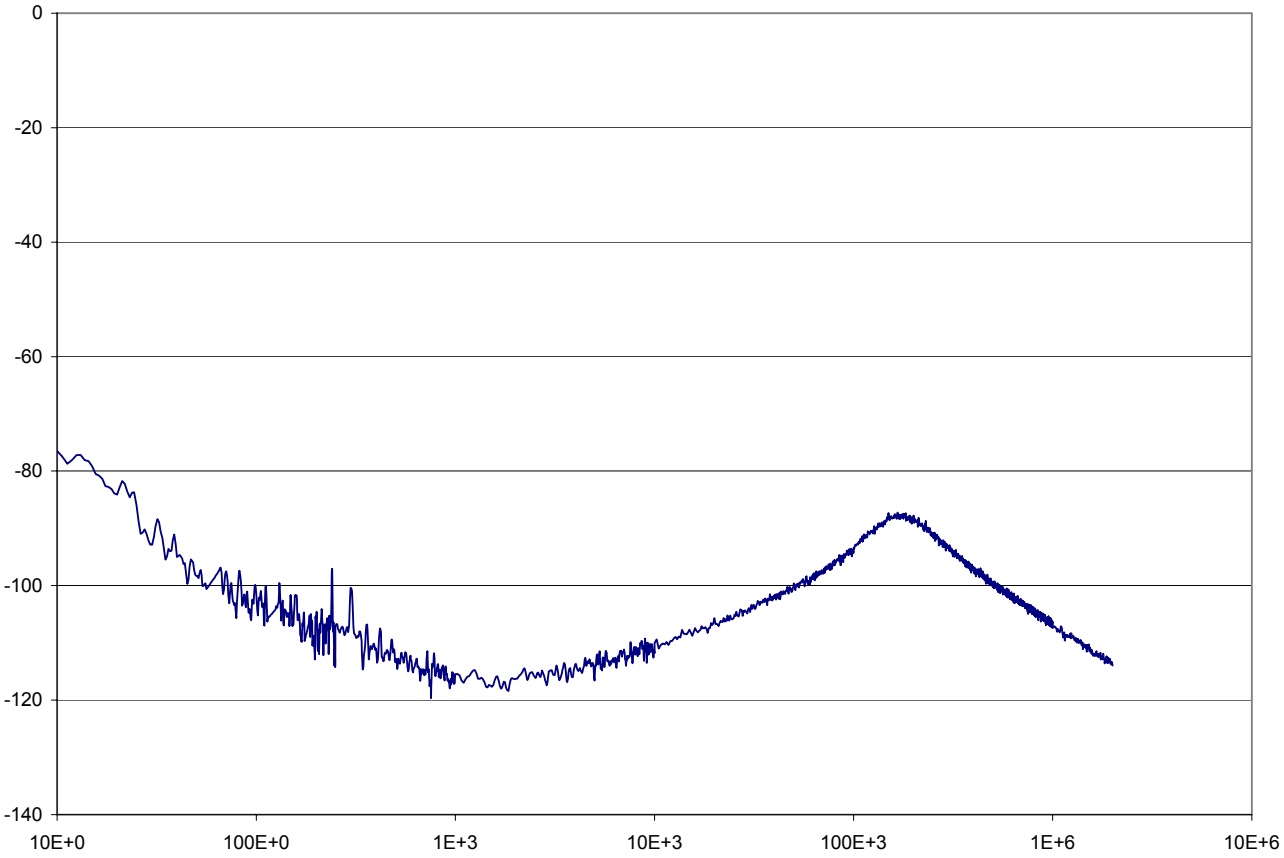
Note for OE1

The OE1 pin is intended to facilitate board test. Note that disabling the FBLK will open the loop, causing a high-frequency to be output from CLK2. Therefore, set OE1 low only if the chip is in power-down (S3:S0 = 0).

Thermal Characteristics

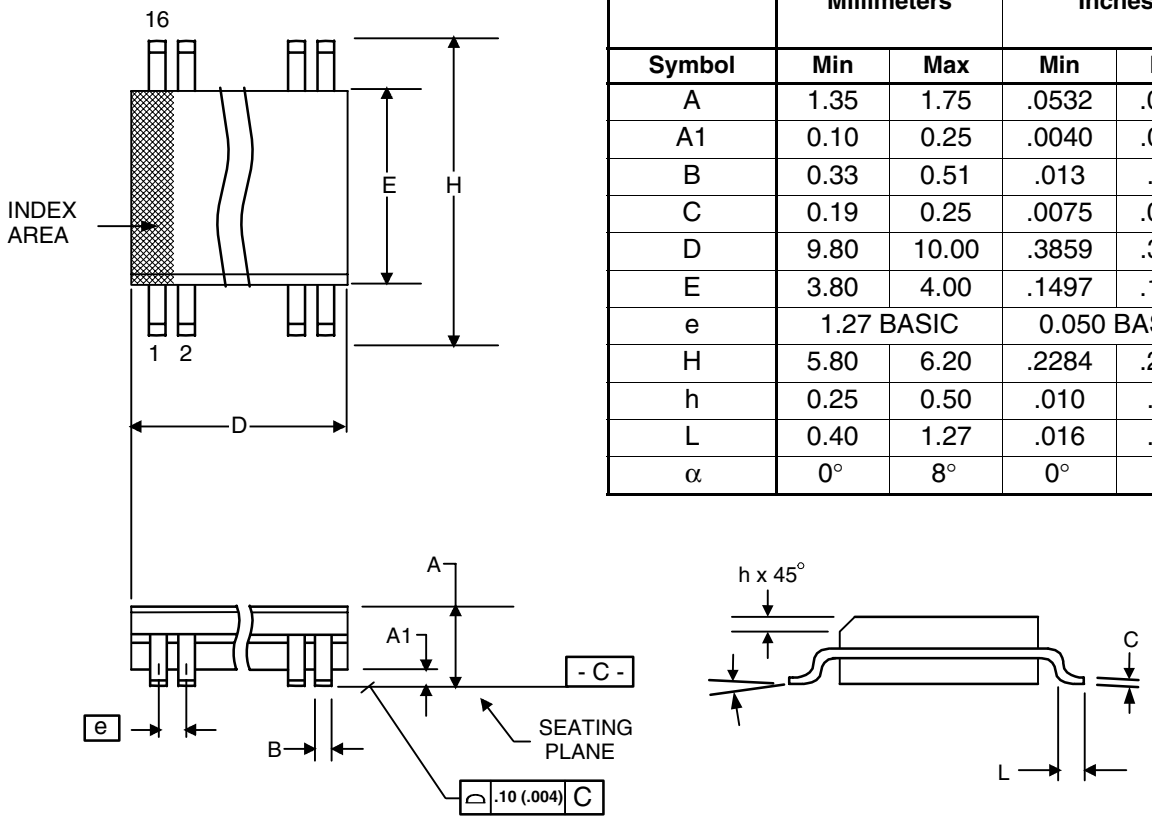
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Phase Noise for 125 MHz output, 25 MHz clock input (VDD = 3.3 V)



Package Outline and Package Dimensions (16-pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
670M-04ILF	670M-04ILF	Tubes	16-pin SOIC	-40 to +85° C
670M-04ILFT	670M-04ILF	Tape and Reel	16-pin SOIC	-40 to +85° C

"LF" denotes Pb (lead) free package.

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