SY89645L

Precision Low Skew, 1-to-4 LVCMOS/LVTTL-to-LVDS Fanout Buffer

General Description

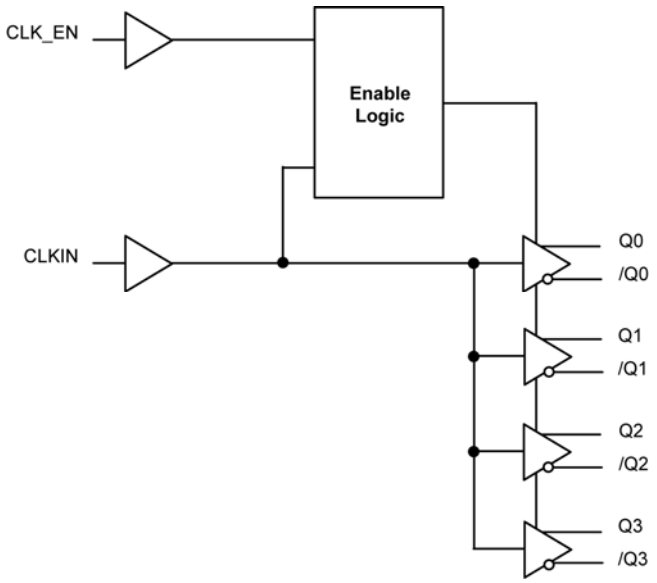
The SY89645L is a 3.3V, fully differential, low skew, 1:4 LVDS fanout buffer that accepts LVTTL or LVCMOS inputs. It is capable of processing clock signals as fast as 650MHz. The LVDS signals are optimized to provide less than 40ps of output skew.

The single-ended input takes a 3.3V LVTTL or LVCMOS, with a signal swing as small as 1.2V. The outputs are 280mV LVDS, with fast rise and fall times, guaranteed to be less than 400ps.

The SY89645L operates from a 3.3V ± 5% power supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). The SY89645L is part of Micrel's Precision Edge® product line.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Block Diagram



Precision Edge®

Features

- Four identical LVDS outputs
- CLKIN accepts LVCMOS or LVTTL input levels
- Maximum output frequency: 650MHz
- Translates LVCMOS/LVTTL input signals to LVDS levels
- <40ps output-to-output skew
- <3ns propagation delay
- <400ps rise/fall times
- 3.3V ±5% operating supply
- Industrial temperature range: –40°C to +85°C
- Available in 20-pin TSSOP

Applications

- Communications
- High-performance computing
- Clock and data distribution

Markets

- Datacom
- Telecom
- Storage
- ATE
- Test and Measurement

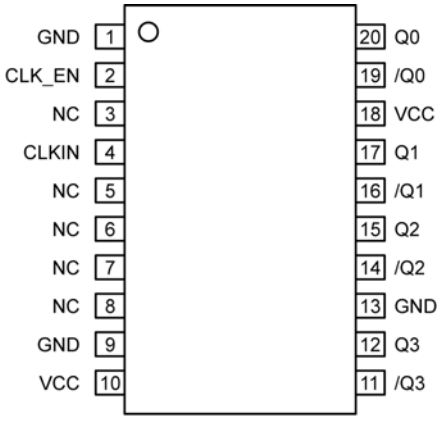
Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89645LK4G	K4-20-1	Industrial	SY89645LK4G with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY89645LK4GTR[2]	K4-20-1	Industrial	SY89645LK4G with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



20-Pin TSSOP (K4-20-1)

Pin Description

Pin Number	Pin Name	Pin Function
1, 9, 13	GND	Power Supply Ground.
2	CLK_EN	Clock Enable. When LOW, Q outputs are forced low, /Q outputs are forced high. The synchronous nature of the enable function forces the output clocks to enable or disable following a rising and a falling edge of the input clock. When HIGH, clock outputs follow input clock. Internal 50kΩ pull-up resistor. $V_{TH} = V_{CC}/2$. See “Clock Enable (CLK_EN) Description” section.
3, 5, 6, 7, 8	NC	No Connect.
4	CLKIN	LVCMOS/LVTTL Clock Input. This is the input to the device. Input accepts single-ended input signals as small as 1.2V. $V_{TH} = V_{CC}/2$. Internal 50kΩ pull-down resistor.
10, 18	VCC	Positive Supply Pins. Connect to 3.3V supply, bypass with low ESR capacitors, as close to pins as possible.
11, 12 14, 15 16, 17 19, 20	/Q3, Q3 /Q2, Q2 /Q1, Q1 /Q0, Q0	LVDS Differential Output Pairs: Differential buffered copies of the input signal. The output swing is typically 280mV. Normally terminated with 100Ω across the output pairs (Q and /Q). See “LVDS Output Termination” section.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.6V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} +0.3V
LVDS Output Current (I_{OUT}) ..... ±10mA
Lead Temperature (soldering, 20sec.) ..... 260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{IN}) ..... +3.135V to +3.465V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
TSSOP
Junction-to-Ambient (θ_{JA})
Still-Air, Multi-Layer Board ..... 75°C/W
Junction-to-Case (θ_{JC}) ..... 21°C/W

DC Electrical Characteristics[4]

V_{DD} = 3.3V ±5%, T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	Positive Supply Voltage Range		3.135	3.3	3.465	V
I_{CC}	Power Supply Current	No Load		43	60	mA

LVCMOS/LVTTL DC Electrical Characteristics[4]

V_{CC} = 3.3V ±5%, T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	Input HIGH Voltage CLKIN, CLK_EN		2		V_{CC}+0.15	V
V_{IL}	Input LOW Voltage CLKIN, CLK_EN		-0.3		0.8	V
I_{IH}	Input HIGH Current CLKIN CLK_EN	V_{CC} = V_{IN} = 3.465V V_{CC} = V_{IN} = 3.465V			150 70	µA
I_{IL}	Input LOW Current CLKIN CLK_EN	V_{CC} = 3.465V, V_{IN} = 0V V_{CC} = 3.465V, V_{IN} = 0V	-70 -150			µA

LVDS Outputs DC Electrical Characteristics[4]

V_{CC} = 3.3V ±5%, R_L = 100Ω across the outputs, T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{OUT}	Output Voltage Swing	See Figure 1a	200	280		mV
V_{DIFF_OUT}	Differential Output Voltage Swing	See Figure 1b	400	560		mV
V_{OCM}	Output Common Mode Voltage		1.125	1.25	1.375	V
ΔV_{OCM}	Change in Common Mode Voltage			5	25	mV

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. ψ_{JB} and θ_{JA} values are determined for a 4-layer board in still-air number, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC Electrical Characteristics[5]

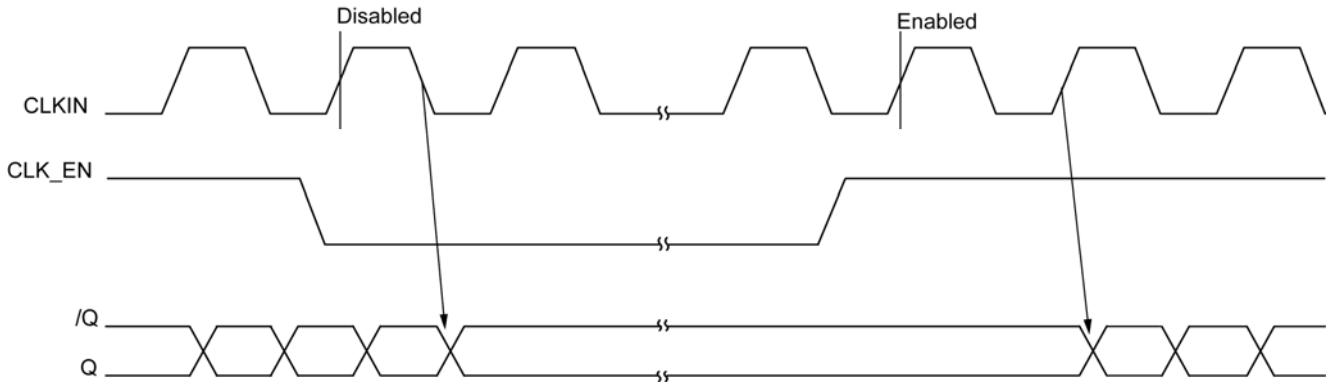
V_{CC} = +3.3V ±5%, R_L = 100Ω across the outputs, T_A = –40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{MAX}	Maximum Frequency	V_{OUT} > 140mV	650			MHz
t_{PD}	Propagation Delay	f_{MAX} ≤ 650MHz, Note 6	1.0	1.8	3.0	ns
t_{SKEW}	Output Skew	Note 7			40	ps
	Part-to-Part Skew	Note 8			500	ps
t_r, t_f	Output Rise/Fall Times (20% to 80%)	f_{MAX} ≤ 266MHz	150	250	400	ps
	Duty Cycle	f_{MAX} ≤ 266MHz	45		55	%
		f_{MAX} > 266MHz	40		60	%

Notes:

5. All parameters measured at f_{MAX} ≤ 650MHz, unless otherwise stated.
6. Measured from V_{CC}/2 of the input to the differential output crossing point.
7. Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{CC}/2 of the input to the differential output crossing point.
8. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Timing Diagram



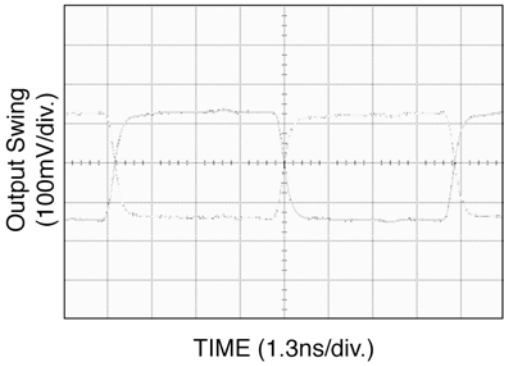
Clock Enable (CLK_EN) Description

The enable function is synchronous so that the clock outputs will be enabled or disabled following a rising and a falling edge of the input clock.

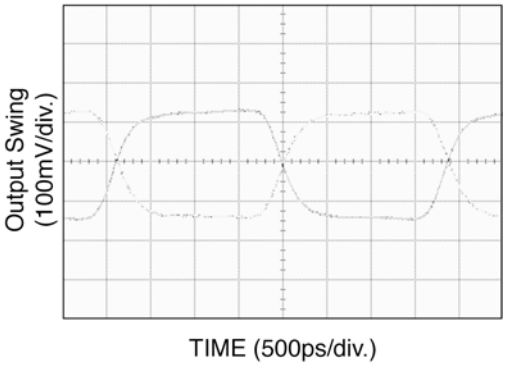
Typical Operating Techniques

V_{CC} = 3.3V ± 5%; V_{IN} > 2V; T_A = 25°C, R_L = 100Ω across output pair; unless otherwise stated.

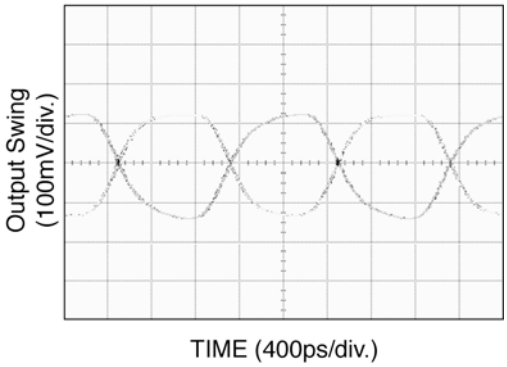
100MHz Clock



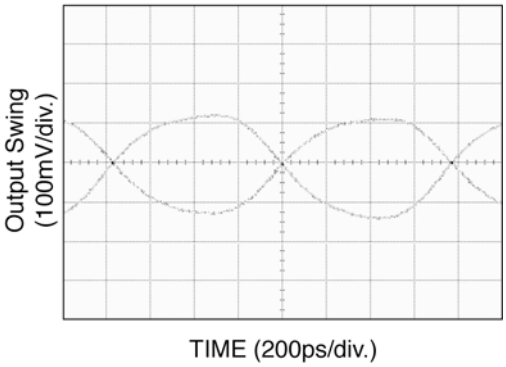
266MHz Clock



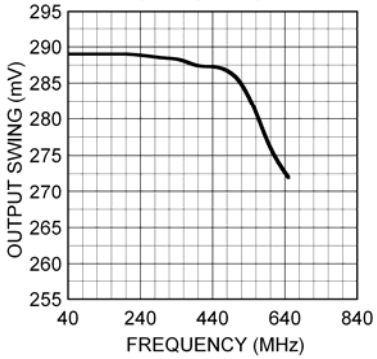
500MHz Clock



650MHz Clock



Frequency Response



hbwhelp@micrel.com or (408) 955-1690

Single-Ended and Differential Swings

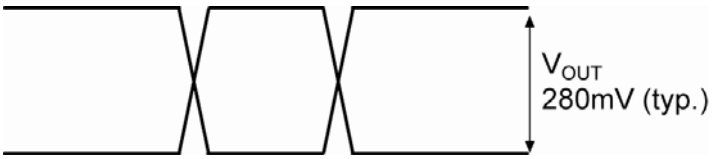


Figure 1a. Single-Ended Voltage Swing

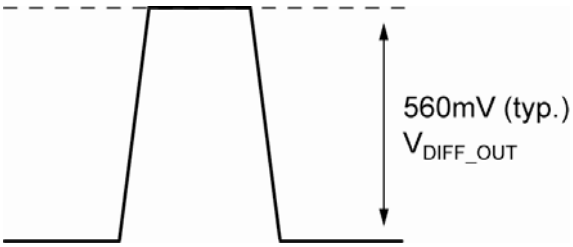


Figure 1b. Differential Voltage Swing

LVDS Output Interface Applications

LVDS specifies a small swing of 280mV typical, on a nominal 1.25V common mode above ground. The common mode voltage has tight limits to permit large variations in ground between an LVDS driver and receiver. Also, change in common mode voltage, as a function of data input, is kept to a minimum, to keep EMI low.

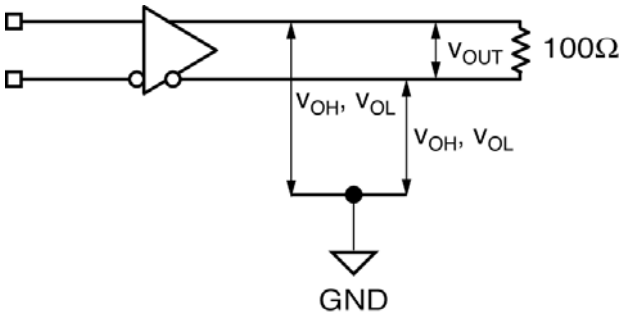


Figure 2a. LVDS Differential Measurement

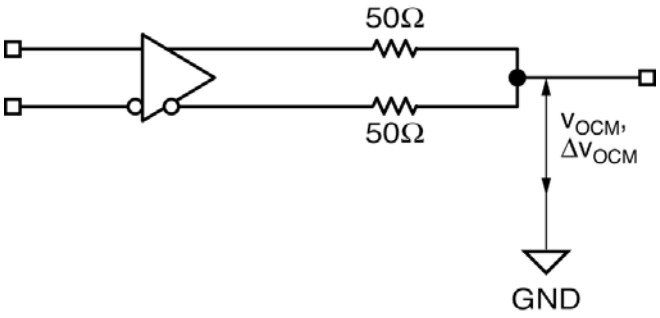
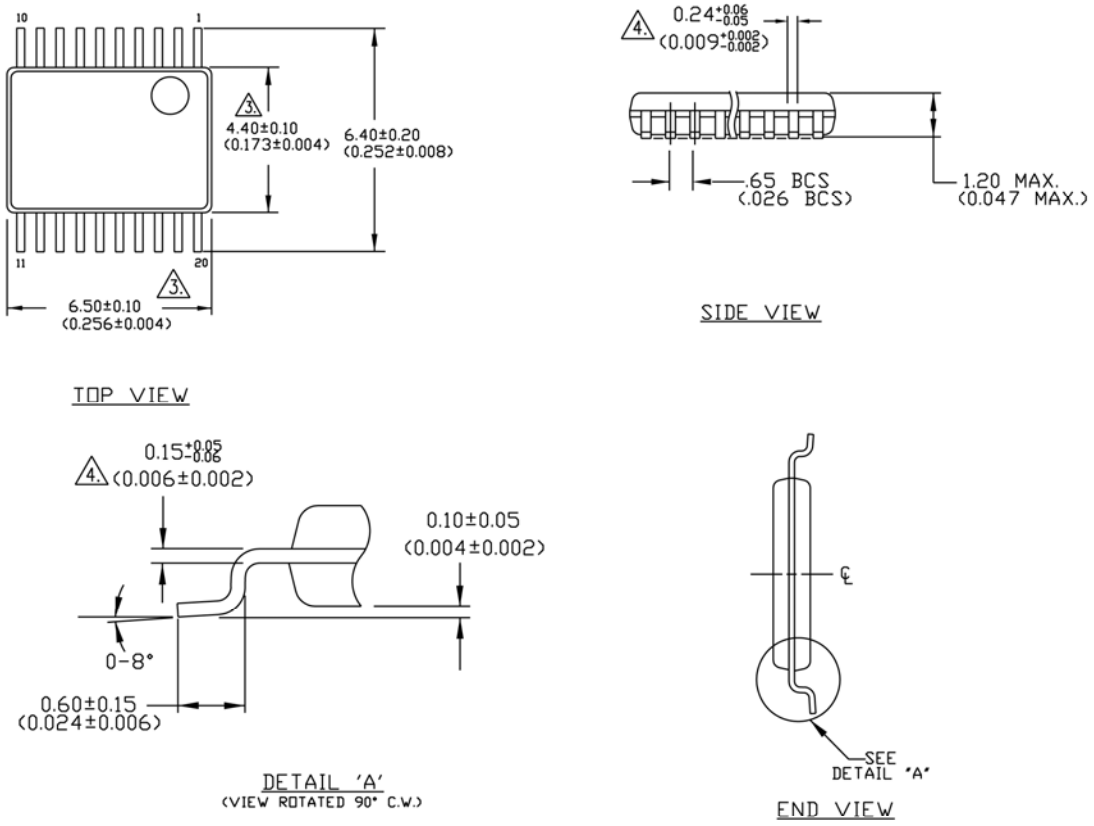


Figure 2b. LVDS Common-Mode Measurement

Package Information



NOTES:
1. DIMENSIONS ARE IN MM[INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. THIS DIMENSION INCLUDES LEAD FINISH.

20-Pin TSSOP (MM)

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