
11.3-Gbps Limiting Amplifier

FEATURES

- Up to 11.3-Gbps Operation
- Loss-of-Signal Detection (LOS)
- Adjustable Output Voltage
- Low Power Consumption
- Input Offset Cancellation
- CML Data Outputs With On-Chip, 50- Ω Back-Termination to VCC
- Single 3.3 V Supply
- Surface-Mount, Small-Footprint, 3-mm \times 3-mm, 16-Pin QFN Package

APPLICATIONS

- 10 Gigabit Ethernet Optical Transmitters
- 8 \times and 10 \times Fibre Channel Optical Transmitters
- SONET OC-192/SDH-64 Optical Transmitters
- XFP and SFP+ Transceiver Modules
- XENPAK, XPAK, X2 and 300-Pin MSA Transponder Modules
- Cable Driver and Receiver

DESCRIPTION

The ONET1191P is a high-speed, 3.3-V limiting amplifier for copper-cable and fiber-optic applications with data rates up to 11.3 Gbps.

This device provides a gain of about 40 dB which ensures a fully differential output swing for input signals as low as 5 mV_{pp}. The output amplitude can be adjusted from 400 mV_{pp} to 700 mV_{pp}. Loss-of-signal detection and output disable are also provided.

The part is available in a small-footprint, 3-mm \times 3-mm, 16-pin QFN package, typically dissipates less than 110 mW, and is characterized for operation from -40°C to 85°C .

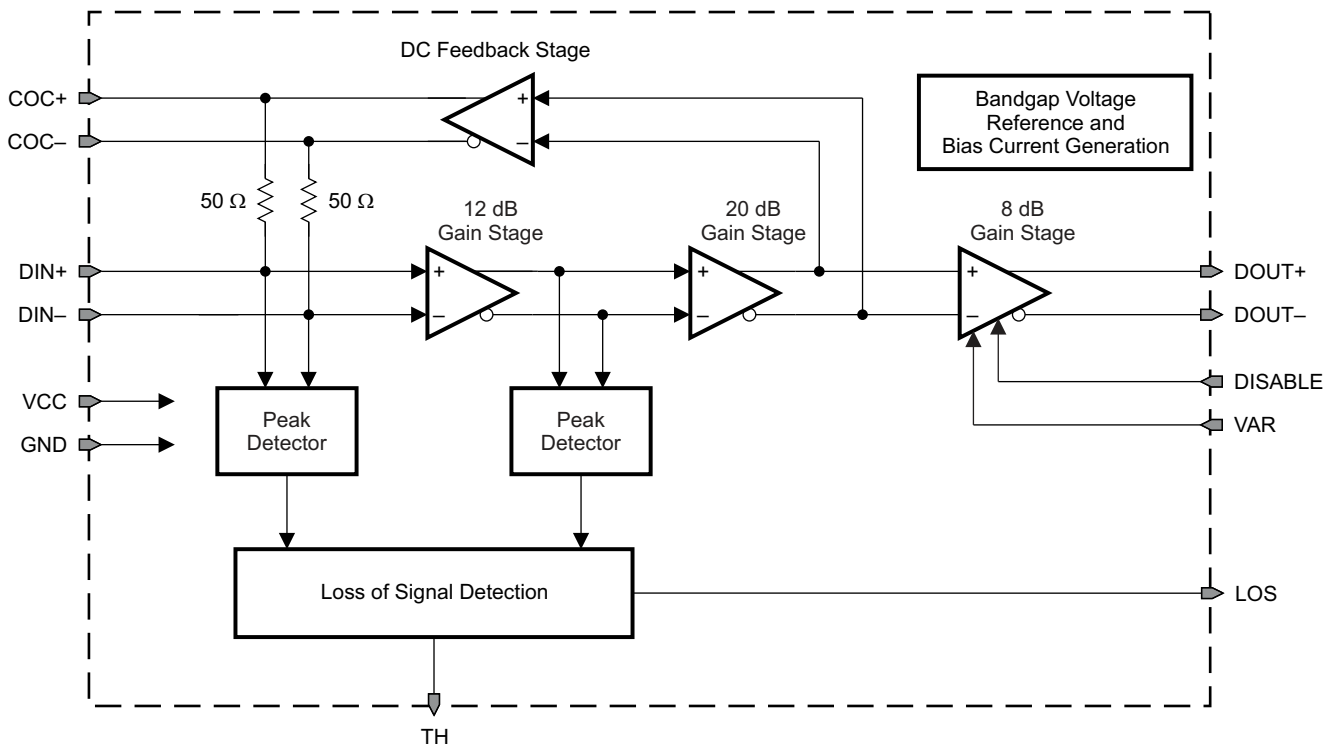


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BLOCK DIAGRAM

A simplified block diagram of the ONET1191P is shown in Figure 1.

This compact, low-power, 11.3-Gbps limiting amplifier consists of a high-speed data path with offset cancellation (dc feedback), a loss-of-signal detection block using two peak detectors, and a band-gap voltage reference and bias current generation block.



B0067-02

Figure 1. Simplified Block Diagram of the ONET1191P

HIGH-SPEED DATA PATH

The high-speed data signal is applied to the data path by means of the input signal pins, DIN+/DIN-. The data path consists of a 12-dB input gain stage with $2 \times 50\text{-}\Omega$ on-chip line-termination resistors, a second gain stage with 20 dB of gain, and a variable-gain output stage which provides another 8 dB of gain. The amplified data output signal is available at the output pins DOUT+/DOUT-, which include on-chip $2 \times 50\text{-}\Omega$ back-termination to VCC. The output amplitude can be adjusted between 400 mV_{pp} and 700 mV_{pp} by connecting an external resistor between the VAR pin and ground (GND).

A dc feedback stage compensates for internal offset voltages and thus ensures proper operation even for very small input data signals. This stage is driven by the output signal of the second gain stage. The signal is low-pass filtered, amplified, and fed back to the input of the first gain stage via the on-chip, $50\text{-}\Omega$ termination resistors. The required low-frequency cutoff is determined by an external $0.1\text{ }\mu\text{F}$ capacitor, which must be differentially connected to the COC+/COC- pins.

LOSS-OF-SIGNAL DETECTION

The peak values of the input signal and output signal of the first gain stage are monitored by two peak detectors. The peak values are compared to a predefined loss-of-signal threshold voltage inside the loss-of-signal detection block. As a result of the comparison, the LOS signal, which indicates that the input signal amplitude is below the defined threshold level, is generated.

The threshold voltage can be set within a certain range by means of an external resistor connected between the TH pin and ground.

BAND-GAP VOLTAGE AND BIAS GENERATION

The ONET1191P limiting amplifier is supplied by a single 3.3-V supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

On-chip band-gap voltage circuitry generates a reference voltage, independent of supply voltage, from which all other internally required voltages and bias currents are derived.

PACKAGE

For the ONET1191P, a small-footprint, 3-mm × 3-mm, 16-pin QFN package, with a lead pitch of 0,5 mm, is used. The pinout is shown in [Figure 2](#).

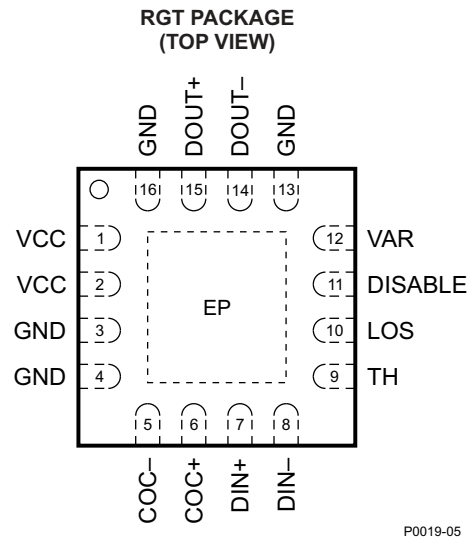


Figure 2. Pinout of ONET1191P in a 3-mm × 3-mm, 16-Pin QFN Package

TERMINAL FUNCTIONS

| TERMINAL | | TYPE | DESCRIPTION |
|----------|------------------|----------------|---|
| NAME | NO. | | |
| COC+ | 6 | Analog | Offset cancellation filter capacitor plus terminal. An external 0.1 μF filter capacitor must be connected between this pin and COC– (pin 5). |
| COC– | 5 | Analog | Offset cancellation filter capacitor minus terminal. An external 0.1 μF filter capacitor must be connected between this pin and COC+ (pin 6). |
| DIN+ | 7 | Analog input | Noninverted data input. On-chip, 50-Ω terminated to COC+. Differentially 100-Ω terminated to DIN–. |
| DIN– | 8 | Analog input | Inverted data input. On-chip, 50-Ω terminated to COC–. Differentially 100-Ω terminated to DIN+. |
| DISABLE | 11 | CMOS input | Disables the output stage when set to a high level |
| DOU+ | 15 | CML out | Noninverted data output. On-chip, 50-Ω back-terminated to VCC. |
| DOU– | 14 | CML out | Inverted data output. On-chip, 50-Ω back-terminated to VCC. |
| GND | 3, 4, 13, 16, EP | Supply | Circuit ground. Exposed die pad (EP) must be grounded. |
| LOS | 10 | Open-drain MOS | High level indicates that the input signal amplitude is below the programmed threshold level. Open-drain output. Requires an external 10-kΩ pullup resistor to VCC for proper operation. |
| TH | 9 | Analog input | LOS threshold adjustment with resistor to GND |
| VAR | 12 | Analog input | Variable output amplitude control. Output amplitude can be reduced to 400 mV _{pp} by grounding the VAR pin. Output amplitude can be set from 400 mV _{pp} to 700 mV _{pp} by connecting a 0 to 100-kΩ resistor to GND or leaving the pin open. |
| VCC | 1, 2 | Supply | 3.3-V ±10% supply voltage |

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | VALUE | UNIT |
|--|--|-----------|----------|
| V_{CC} | Supply voltage ⁽²⁾ | –0.3 to 4 | V |
| V_{DIN+} , V_{DIN-} | Voltage at DIN+, DIN– ⁽²⁾ | 0.5 to 4 | V |
| V_{LOS} , V_{COC+} , V_{COC-} , V_{TH} , V_{DOUT+} , V_{DOUT-} | Voltage at LOS, COC+, COC–, TH, DOUT+, DOUT– ⁽²⁾ | –0.3 to 4 | V |
| $V_{DIN,DIFF}$ | Differential voltage between DIN+ and DIN– | ±1.25 | V |
| I_{LOS} | Current into LOS | 1 | mA |
| I_{DIN+} , I_{DIN-} , I_{DOUT+} , I_{DOUT-} | Continuous current at inputs and outputs | 20 | mA |
| ESD | ESD rating at all pins | 1.5 | kV (HBM) |
| $T_{J,max}$ | Maximum junction temperature | 125 | °C |
| T_{STG} | Storage temperature range | –65 to 85 | °C |
| T_A | Characterized free-air operating temperature range | –40 to 85 | °C |
| T_{LEAD} | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | TYP | MAX | UNIT |
|----------|--------------------------------|-----|-----|------|------------|
| V_{CC} | Supply voltage | 2.9 | 3.3 | 3.6 | V |
| T_A | Operating free-air temperature | –40 | | 85 | °C |
| | Disable input high voltage | 2 | | | V |
| | Disable input low voltage | | | 0.25 | V |
| | Optimum LOS threshold resistor | 32 | | 62 | k Ω |
| | R_{VAR} range | 0 | | open | k Ω |

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, outputs connected to a 50- Ω load, R_{VAR} = open (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|------------------------|--|------|-----|----------|
| V_{CC} | Supply voltage | 2.9 | 3.3 | 3.6 | V |
| I_{VCC} | Supply current | | 33 | 49 | mA |
| R_{IN} | Data input resistance | | 50 | | Ω |
| R_{OUT} | Data output resistance | | 50 | | Ω |
| | Voltage at TH pin | | 1.25 | | V |
| | LOS HIGH voltage | 10-k Ω pullup to V_{CC} , $I_{SOURCE} = 50 \mu A$ | 2.4 | | |
| | LOS LOW voltage | 10-k Ω pullup to V_{CC} , $I_{SINK} = 200 \mu A$ | | 0.5 | V |

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, outputs connected to a 50-Ω load, R_{VAR} = open (unless otherwise noted). Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|----------------------------------|---|------|------|------|-------------------|
| f_{3dB-H} | High-frequency –3-dB bandwidth | | 8 | 11 | 15 | GHz |
| f_{3dB-L} | Low-frequency –3-dB bandwidth | $C_{OC} = 0.1 \mu F$, ac coupling capacitors = 0.1 μF | | 30 | | kHz |
| $V_{IN,MIN}$ | Data input sensitivity | $K28.5$ at 11.3 Gbps, BER < 10^{-12} | | 2.5 | 5 | mV _{pp} |
| | | $V_{OD-min} \geq 0.95 \times V_{OD}$ (output limited) | | 10 | 20 | |
| A | Small-signal gain | | 34 | 40 | 44 | dB |
| $V_{IN,MAX}$ | Data input overload | | 2000 | | | mV _{pp} |
| DJ | Deterministic jitter | $V_{IN} = 5 \text{ mV}_{pp}$, K28.5 at 11.3 Gbps | | 4 | 7 | ps _{pp} |
| | | $V_{IN} = 20 \text{ mV}_{pp}$, K28.5 at 11.3 Gbps | | 4 | 9 | |
| RJ | Random jitter | Input = 5 mV _{pp} | | 1.6 | | ps _{RMS} |
| | | Input = 20 mV _{pp} | | 0.7 | | |
| V_{OD} | Differential data output voltage | $V_{IN} \geq 20 \text{ mV}_{pp}$, DISABLE = LOW | 600 | 700 | 900 | mV _{pp} |
| | | DISABLE = HIGH | | 25 | 100 | |
| t_r | Output rise time | 20% to 80%, $V_{IN} \geq 20 \text{ mV}_{pp}$ | | 25 | 35 | ps |
| t_f | Output fall time | 20% to 80%, $V_{IN} \geq 20 \text{ mV}_{pp}$ | | 25 | 35 | ps |
| V_{TH} | LOS assert threshold range | K28.5 pattern at 10.7 Gbps, $R_{TH} = 62 \text{ k}\Omega$ | | 40 | | mV _{pp} |
| | | K28.5 pattern at 10.7 Gbps, $R_{TH} = 32 \text{ k}\Omega$ | | 65 | | |
| | LOS threshold variation | Versus temperature | | 3 | | dB |
| | | Versus supply voltage V_{CC} | | 1 | | dB |
| | LOS hysteresis | K28.5 pattern at 11.3 Gbps | 1.5 | | 7 | dB |
| t_{LOS_AST} | LOS assert time | | | 1300 | 2000 | ns |
| t_{LOS_DEA} | LOS deassert time | | | 120 | | ns |
| t_{DIS} | Disable response time | | | 90 | | ns |

TYPICAL OPERATION CHARACTERISTICS

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $R_{VAR} = \text{open}$ (unless otherwise noted)

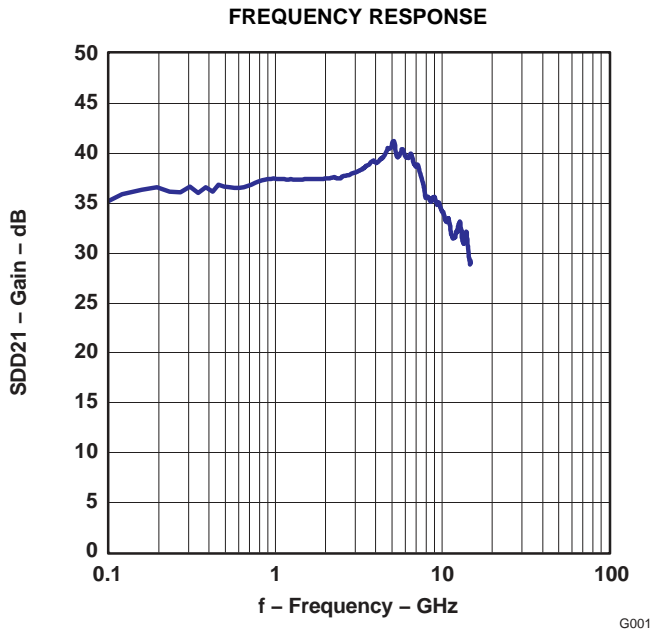


Figure 3.

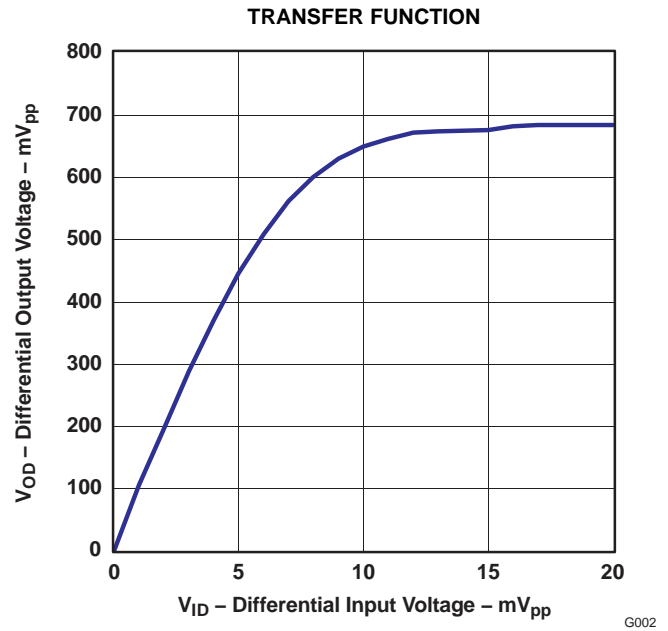


Figure 4.

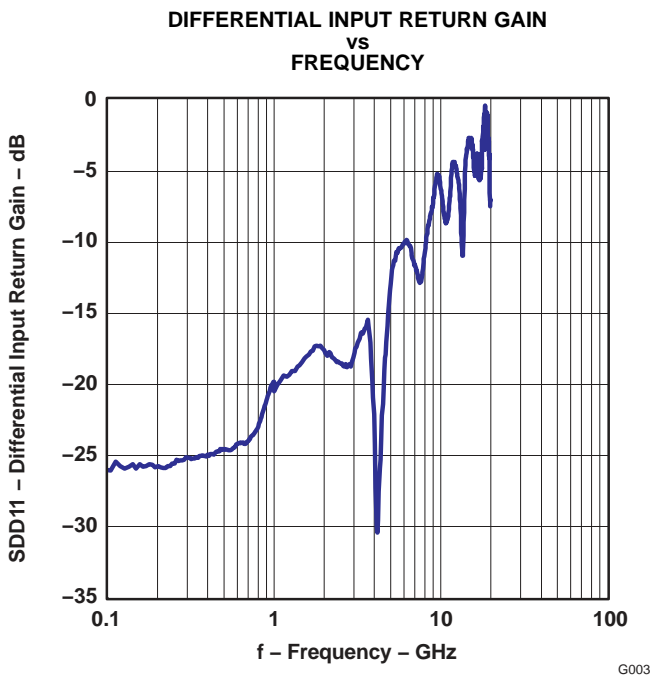


Figure 5.

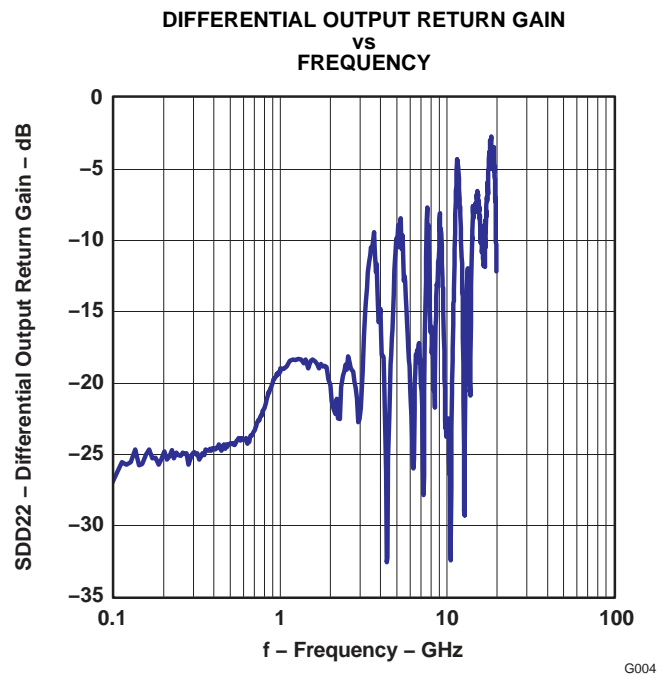


Figure 6.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $R_{VAR} = \text{open}$ (unless otherwise noted)

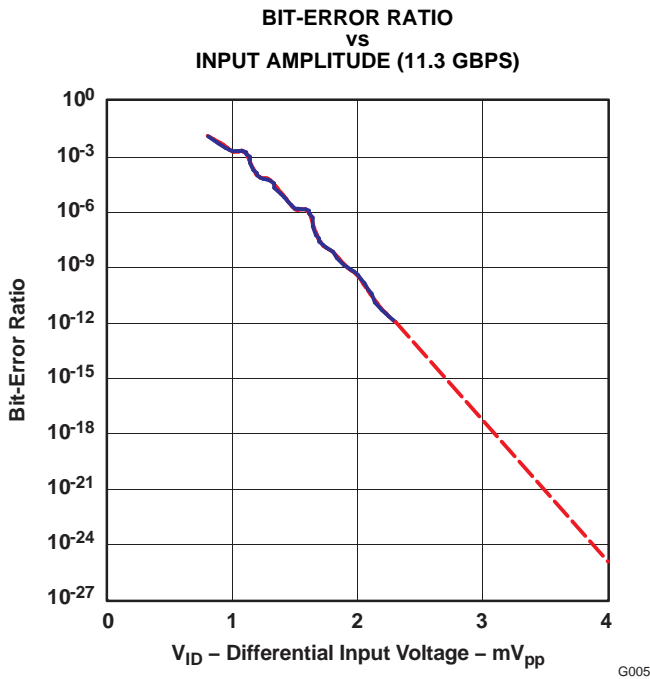


Figure 7.

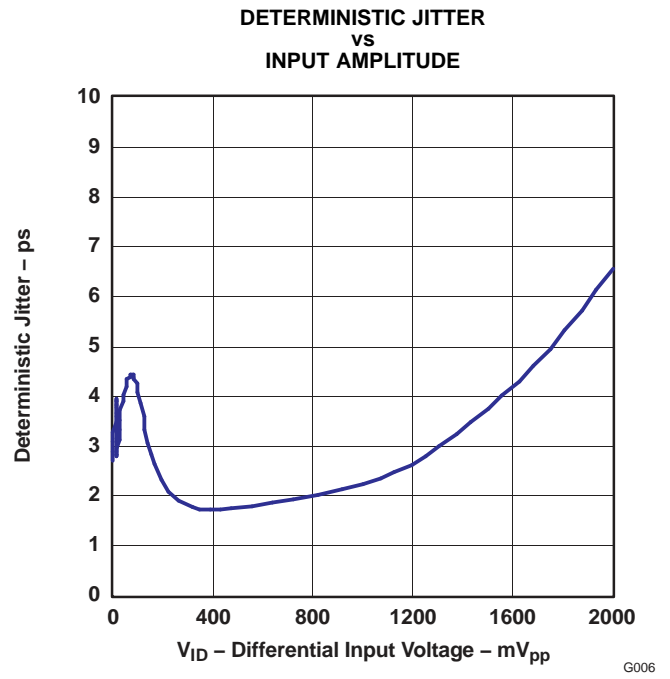


Figure 8.

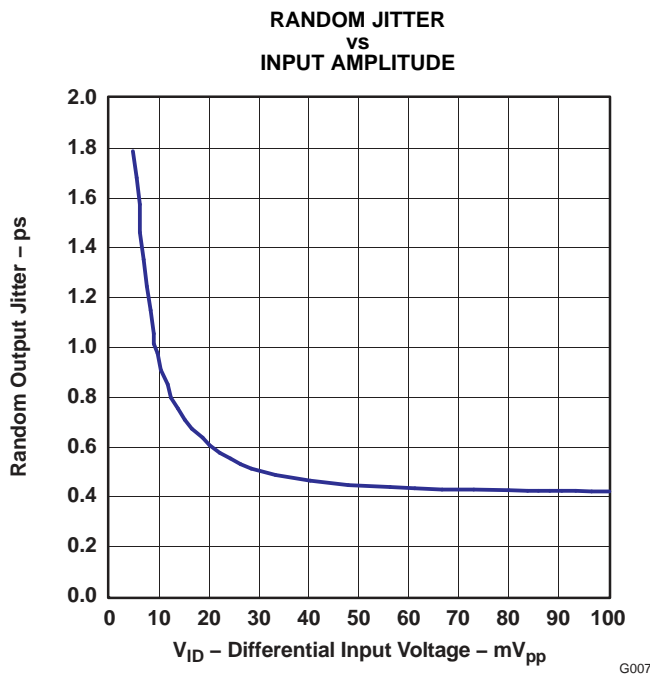


Figure 9.

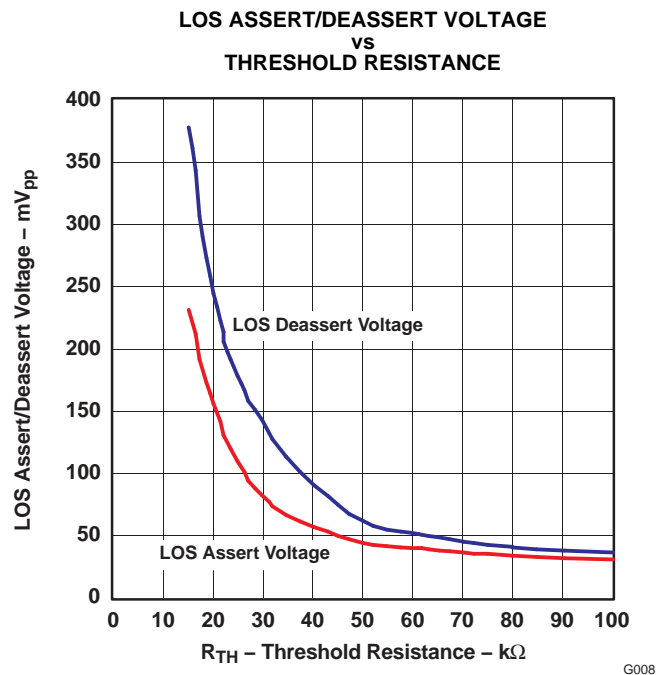


Figure 10.

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $R_{VAR} = \text{open}$ (unless otherwise noted)

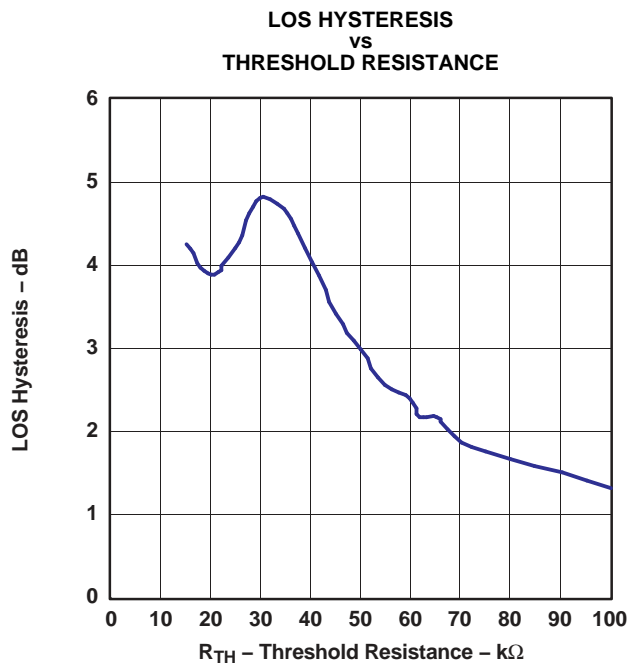


Figure 11.

G009

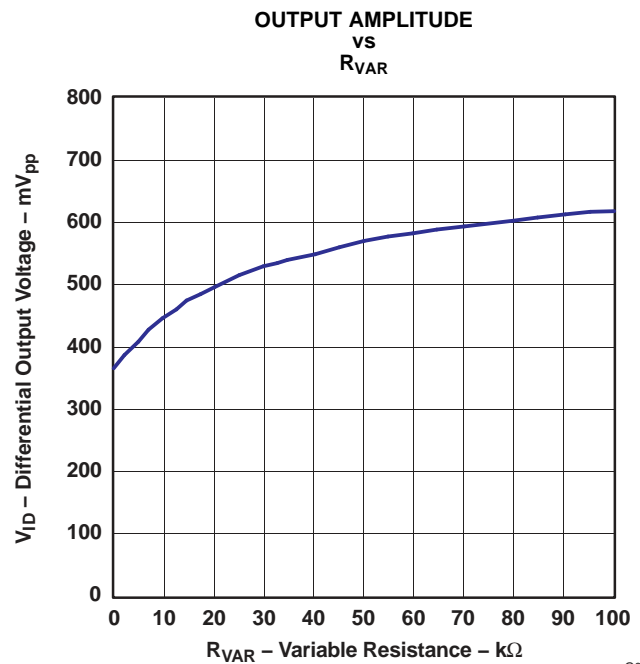


Figure 12.

G010

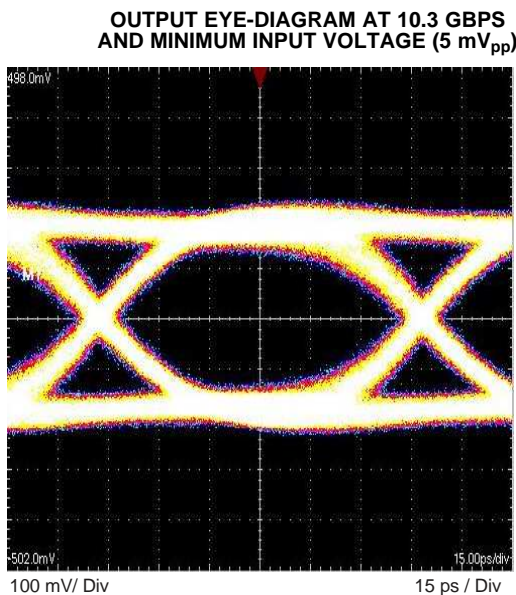


Figure 13.

G011

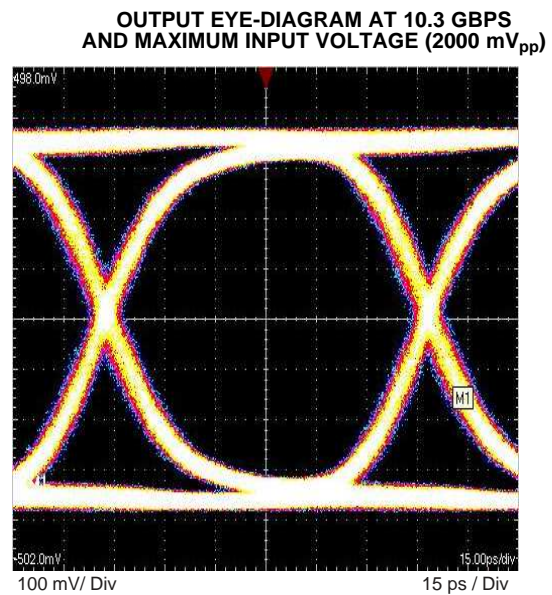


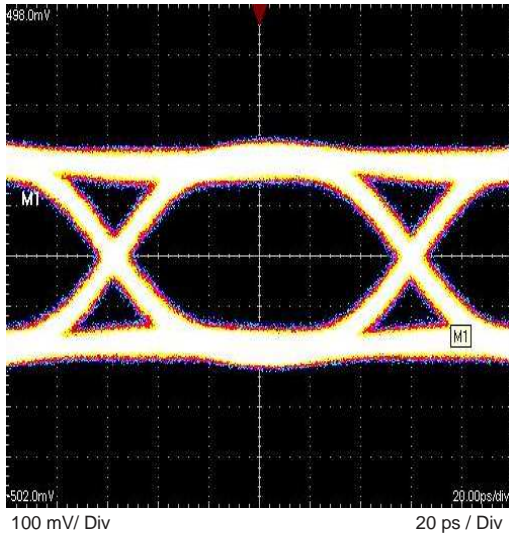
Figure 14.

G012

TYPICAL OPERATION CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$, and $R_{VAR} = \text{open}$ (unless otherwise noted)

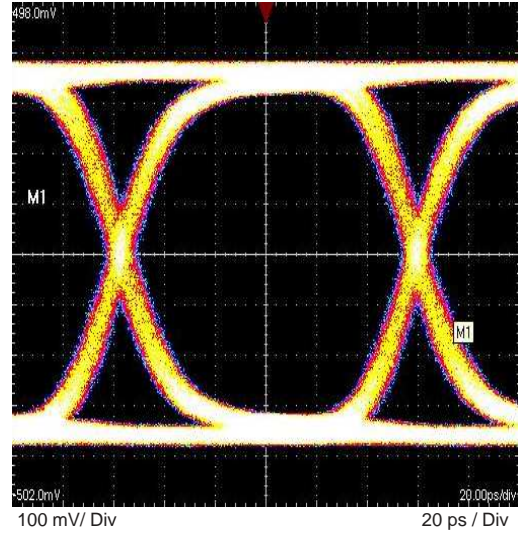
OUTPUT EYE-DIAGRAM AT 8.5 GBPS
AND MINIMUM INPUT VOLTAGE (5 mV_{pp})



G013

Figure 15.

OUTPUT EYE-DIAGRAM AT 8.5 GBPS
AND MAXIMUM INPUT VOLTAGE (2000 mV_{pp})

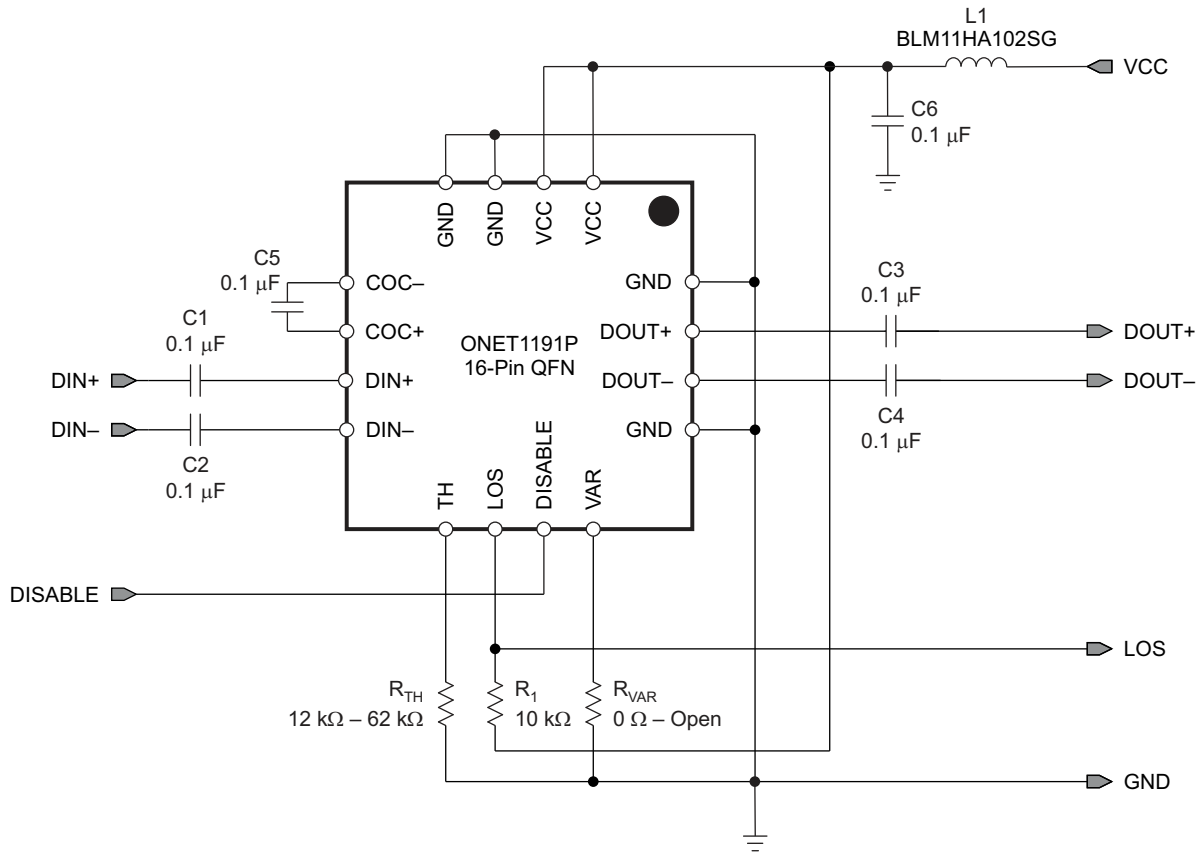


G014

Figure 16.

APPLICATION INFORMATION

Figure 17 shows a typical application circuit using the ONET1191P. The output amplitude can be adjusted with R_{VAR} and the LOS assert voltage is adjusted with R_{TH} .



S0099-03

Figure 17. Basic Application Circuit

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| ONET1191PRGTR | ACTIVE | VQFN | RGT | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 191P | Samples |
| ONET1191PRGTT | ACTIVE | VQFN | RGT | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 191P | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

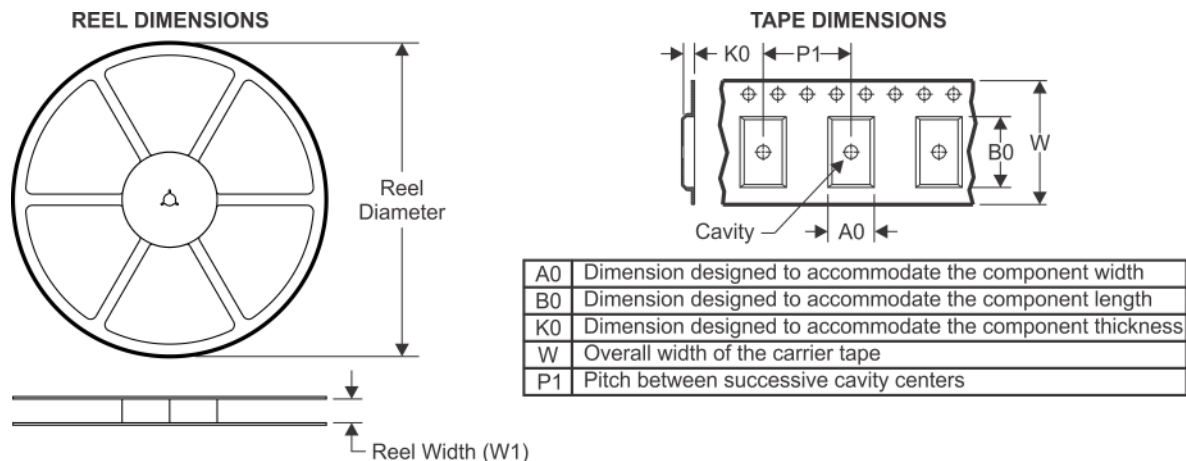
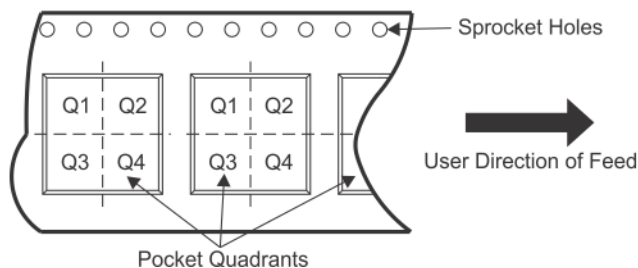
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ONET1191PRGTR | VQFN | RGT | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

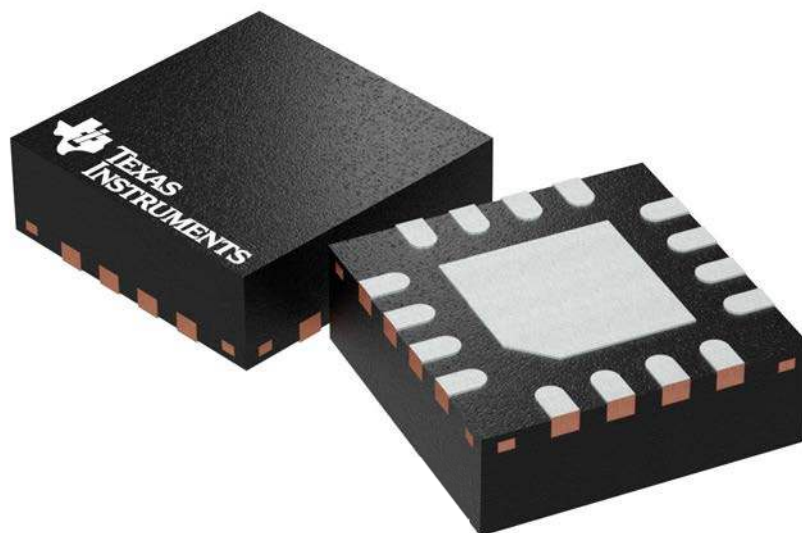
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ONET1191PRGTR | VQFN | RGT | 16 | 3000 | 350.0 | 350.0 | 43.0 |

RGT 16

GENERIC PACKAGE VIEW

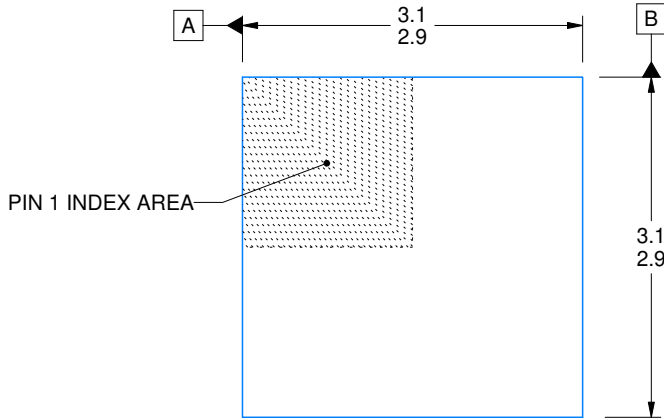
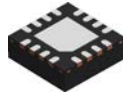
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

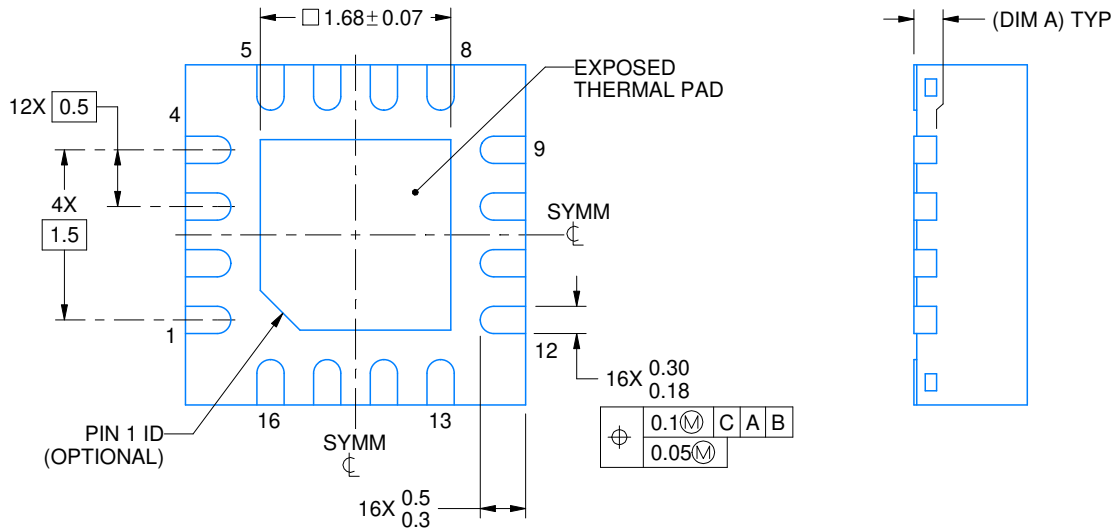
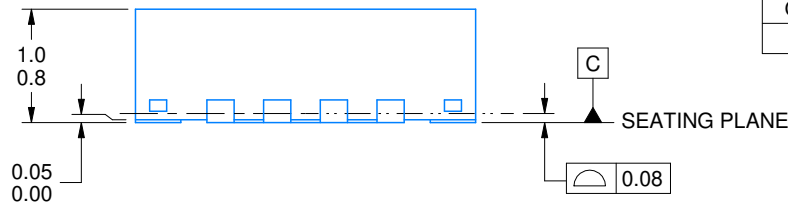


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



| SIDE WALL METAL THICKNESS DIM A | |
|---------------------------------|----------|
| OPTION 1 | OPTION 2 |
| 0.1 | 0.2 |



4222419/D 04/2022

NOTES:

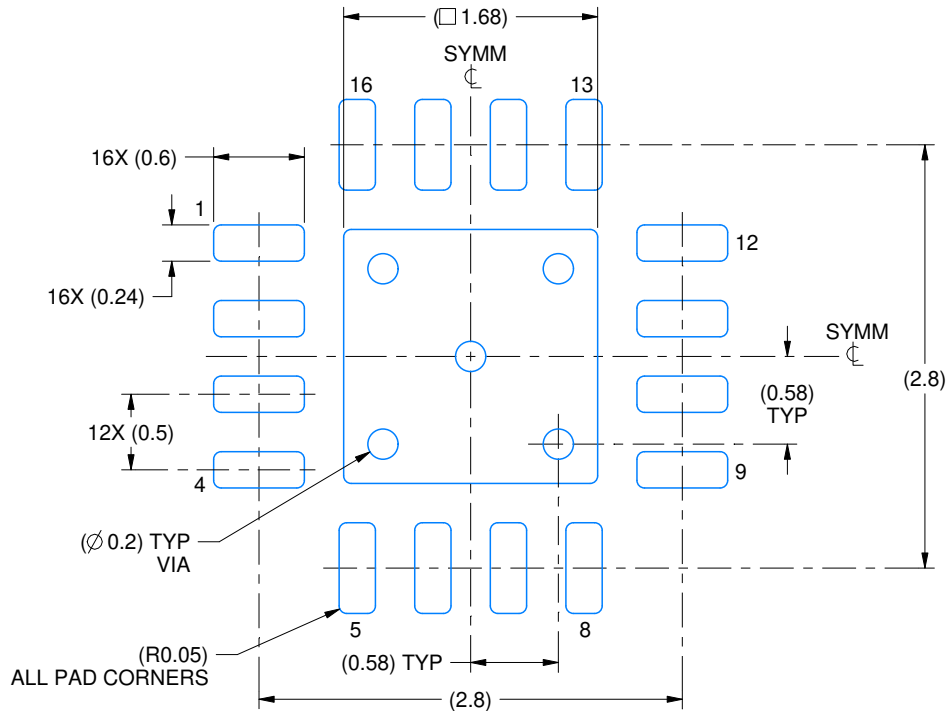
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

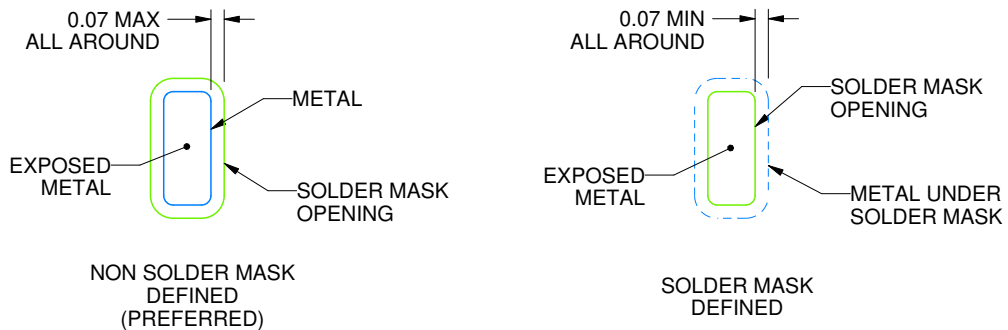
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

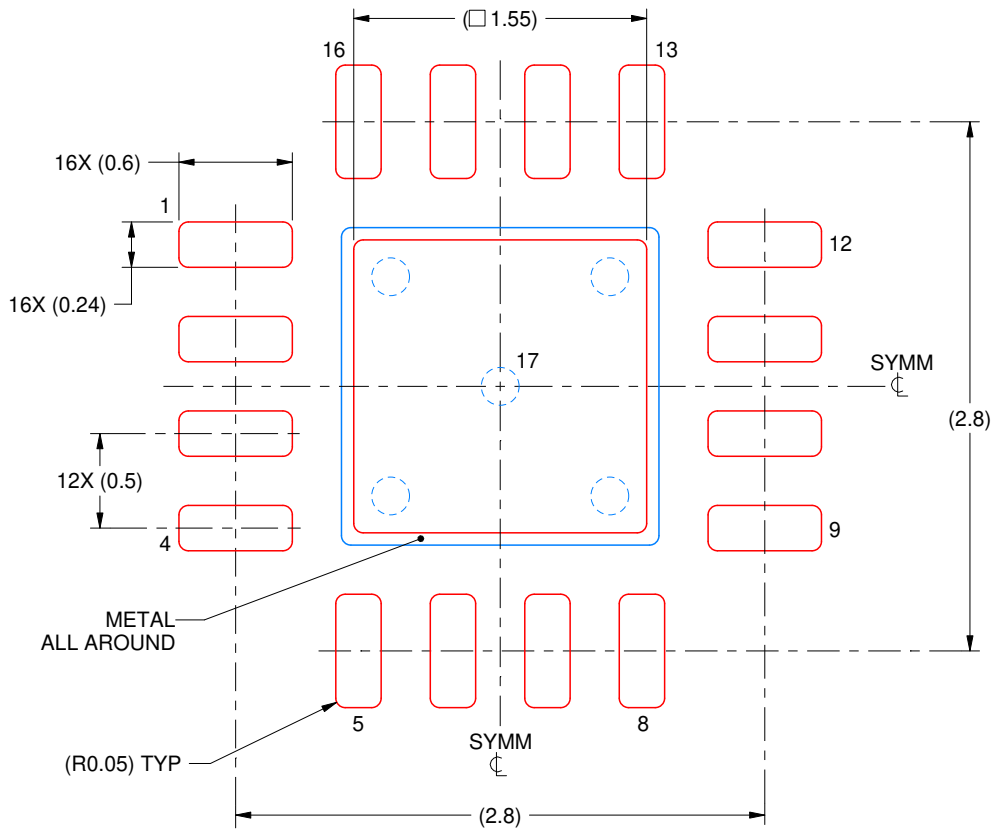
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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