LDI Demonstration Kit User Guide (LVDS Display Interface)

User's Guide

Literature Number: SNLU036A
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LDI Demonstration Kit User Guide (LVDS Display Interface) Introduction

Texas Instruments' LDI demo kit contains a Transmitter (Tx) demo board and a Receiver (Rx) demo board. This kit will demonstrate the chipsets interfacing from a graphics controller using Low Voltage Differential Signaling (LVDS) to a Liquid Crystal Display (LCD) flat panel.

The Transmitter board accepts 3V LVTLL/CMOS RGB signals from a graphics controller along with the clock and control signals. The LVDS Transmitter converts the LVTLL/CMOS parallel lines into serialized LVDS pairs. The serial data streams toggle at 3.5 times the clock speed.

The Receiver board accepts the LVDS serialized data (and clock) and converts them back into parallel LVTLL/CMOS RGB signals for the Panel Timing Controller.

The user needs to provide the proper RGB inputs to the Transmitter and also to provide a proper interface from the Receiver output to the panel timing controller. In some cases, a cable conversion board or harness scramble may be necessary depending on type of cable/connector interface used.

Warnings:

The maximum voltage that should ever be applied to the LDI Transmitter or Receiver Vcc is 4 V. The Transmitter and Receiver power supply pins (Vccs) are **NOT** 5 V tolerant. The Transmitter can however accept a 3.3 V or 5 V LVTLL/CMOS level on the inputs (TxIN). The Transmitter inputs are 5 V tolerant. The maximum voltage that can be applied to any input pin is 5.0 V.

Topic **Page**

1 Contents of Demo Kit

1. One Transmitter board with IDC connectors on Tx input DS90C387MTD - 48 bit Transmitter (http://www.ti.com/lit/ds/symlink/ds90c387.pdf)
2. One Receiver board with IDC connectors on Rx output DS90CF388MTD - 48 bit Receiver (http://www.ti.com/lit/ds/symlink/ds90cf388.pdf)

NOTES:

1. The demo board trace layout is designed for minimum skew between channels. It is not absolutely required in most applications but be aware that the skew margins will be reduced if your board layout is not optimized.
2. The MDR LVDS connector footprint has been set to accept a D26-1 pinout. In order to connect the two boards, use a .050" Mini D Ribbon (MDR) cable assembly, **14526-EZHB-XXX-0QC**. Please refer to: http://www.3m.com/Interconnects.

2 Applications

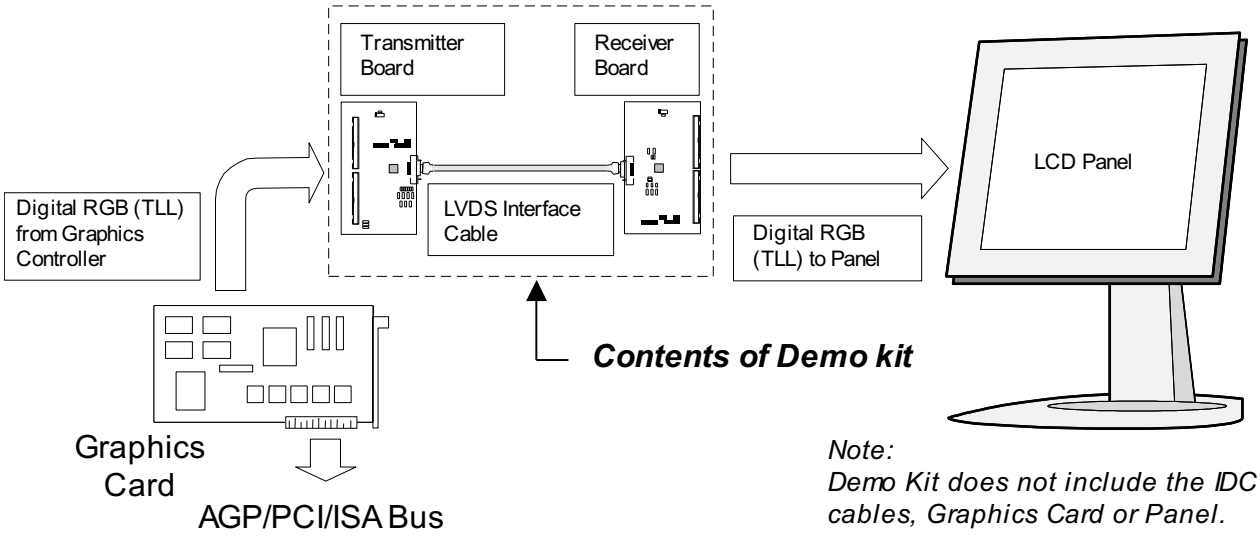


Figure 1. LDI Application

The diagram above illustrates the use of the Chipset (Tx/Rx) in a Host to LCD Panel Interface.

Chipsets support up to 24-bit single pixel or 24-bit dual pixel AM-TFT LCD Panels for any VGA (640X480), SVGA (800X600), XGA (1024X768), SXGA (1280X1024), or UXGA (1600X1200).

Because of the non-periodic nature of STN-DD SHFCLK, the Chipset may not work with all D-STN panels. The PLL CLK input of the Transmitter requires a free running periodic SHFCLK. Most Graphics Controller can provide a separate pin with a free running clock. In this case the STN-DD SHFCLK can be sent as Data while the free running clock can be used as SHFCLK for the PLL ref CLK. For example, C&T's 65550's WEC (Pin102) can be programmed to provide a free running clock using the BMP (Bios Modification Program). Please refer to STN Application using (AN-1056) for more information.

Refer to the proper datasheet information on Chipsets (Tx/Rx) provided on each board for more detailed information.

Note: Refer to AN-1127 for suggested mapping schemes.

3 Features and Explanations

3.1 Transmitter

3.1.1 Pre-Emphasis (PRE - pin 14/JP1):

1. 1. This feature enables you to overcome cable capacitance through the LVDS interface. This function provides additional instantaneous current during switching transitions. NOTE: This function does NOT affect Rx output drive.
2. This function works in “Old Mode” or “New Mode”.
3. This function affects Tx A0-A7 and CLKs LVDS outputs only.
4. To disable this function, pin 14 must be tied LOW. LVDS output drive will then be at its standard value of 3.5mA.
5. The input will be pulled low (0.7 V) if no jumper is used. To adjust the level of pre-emphasis, place a jumper on JP1 to Vcc. R48 will now be connected. R48 is a 2K potentiometer. Use a number 1.4mm jeweler’s screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. Too much pre-emphasis can create an overshoot condition at the rising edge and an undershoot condition on the falling edge. Icc will increase but allows you to drive longer cables. Too little pre-emphasis will not allow you to drive longer cables. Monitor any one of the LVDS lines (A0-A7) or CLK1 for a visual confirmation of its effect. It is recommended that you monitor the LVDS signals with a differential probe. If a differential probe is not used, a single ended probe can be used for a quick check.

3.1.2 PLL range select (PLLSEL - pin 15/JP5):

1. Auto-range is selected by tying pin 15 HIGH.
2. Low-range is selected by tying pin 15 LOW.
3. This function works in “Old Mode” or “New Mode”.

3.1.3 Dual/Single Operation (DUAL - pin 23/JP7):

1. This feature provides three different modes of operation. The modes of operation are:
   1) Dual 112MHz TxIN, Dual 112MHz TxOUT (pin 23 = HIGH; jumper JP7 to Vcc)
   2) Single 170MHz TxIN, Dual 85MHz TxOUT (pin 23 = Vcc/2; no jumper on JP7)
   3) Single 112MHz TxIN, Single 112MHz TxOUT (pin 23 = LOW; jumper JP7 to GND)

2. This function works in “Old Mode” or “New Mode”.

3. In Single to Single mode, TxOUT0 through TxOUT3 and associated Tx inputs are active. TxOUT4 through TxOUT7 and associated inputs are disabled to promote power savings on the part.

3.1.4 DC Balance (BAL - pin 24/JP4):

1. This feature prevents charging of a cable in one state e.g. all “1s” or all “0s” for an extended period of time. The benefit to this is to “open” up the LVDS “eye-pattern” (Reducing the Inter-Symbol Interference).

2. This function works in “New Mode” ONLY.

3. It affects Tx A0-A7 and LVDS CLK outputs only.

4. To disable this function, pin 24 is tied LOW. To enable this function pin 24 is tied HIGH.

5. BAL (pin 6 of the Rx/JP6 on Rx board) must also be tied HIGH to enable this function.

6. In this mode, the part is NOT backward compatible with existing FPD-Link technology. This feature must be turned off to be backward compatible with current FPD-Link chipsets.

NOTE: Refer to the “Application Notes” on back of the data sheet for complete description of each feature.

4 Receiver

4.1 PLL range select (PLLSEL - pin 5/JP5):

1. Auto-range is selected by tying pin 5 HIGH.
2. Low-range is selected by tying pin 5 LOW.

4.2 DESKEW option (pin 4/JP4):

1. This function works in "New Mode" ONLY.
2. In order for the "DESKEW" feature to be operational (DESKEW=HIGH), a minimum of four clock cycles is required during blanking time.
3. To set "DESKEW" feature OFF, set jumper JP4 LOW.

4.3 DC Balance (BAL - pin 6/JP6):

1. This feature prevents charging of a cable in one state e.g. all “1s” or all “0s” for an extended period of time. The benefit to this is to “open” up the LVDS “eye-pattern”.
2. This function works in “New Mode” ONLY.
3. To disable this function, pin 6 is tied LOW. To enable this function pin 6 is tied HIGH.
4. BAL (pin 24 of the Tx/JP4 on Tx board) must also be tied HIGH to enable this function.
5. In this mode, the chipset is NOT backward compatible with existing FPD-Link technology. This feature must be turned off to be backward compatible with current FPD-Link chipsets.

NOTE: Refer to the “Application Notes” section on the back of the datasheet for complete description of each feature.

5 How to Hook up the Demo Boards (Overview)

The Tx demo board TxIN has been laid out to accept data from the Video Graphics card through two 50 pin IDC connectors. The TxOUT/RxIN interface uses the 3M MDR connector and 3M MDR cable with a D26-1 pin out. This combination provides minimal skew between LVDS channels. The receiver board RxOUT is laid out generically and must be mapped correctly to the panel being used.

1. Connect one end of the D26-1 MDR cable to the transmitter board and the other end to the receiver board. This is a standard pinout cable, longer lengths are available for purchase from 3M - see http://www.mmm.com
2. Jumpers have been configured from the factory (Refer to Tx and Rx "Jumper Default Settings" on pages 11 and 17) to run in normal mode with Deskew function OFF and with pre-emphasis ON. Jumpers are also provided on both boards so make sure that they are positioned correctly. See "Jumper Setting Examples" on page 22 and page 25 for different application configurations.
3. From the Graphics card, connect the appropriate IDC cable to the transmitter board and connect two 50-pin IDC cables from the receiver boards to the panel (Note: Refer to AN-1127 for suggested mapping schemes.) Note that pin 1 on the connector should be connected to pin 1 of the cable.
4. Power for the Tx and Rx boards are supplied externally through Test Pad (TP) TP1. Grounds for both boards are connected through TP2.
5. Turn on the PC first then power up the panel.

Warning:

Clock 2 is brought over to the Rx board through the USB pair, which are not matched in length with Clock 1, or LVDS data lines. Also the differential impedance of the USB pair is rated at 90 Ω.

6 Power Connections

The Transmitter and Receiver boards can only be powered by supplying power externally through TP1 (Vcc) and TP2 (GND). The maximum voltage that should ever be applied to the LDI Transmitter or Receiver Vcc is 4V. For the transmitter and the receiver to be operational, /PD must be tied to Vcc which is labeled as “JP3” and "JP1", respectively.

Note: J4 on the Tx and J1 on the Rx provide the interface for LVDS signals.

7 Transmitter Board

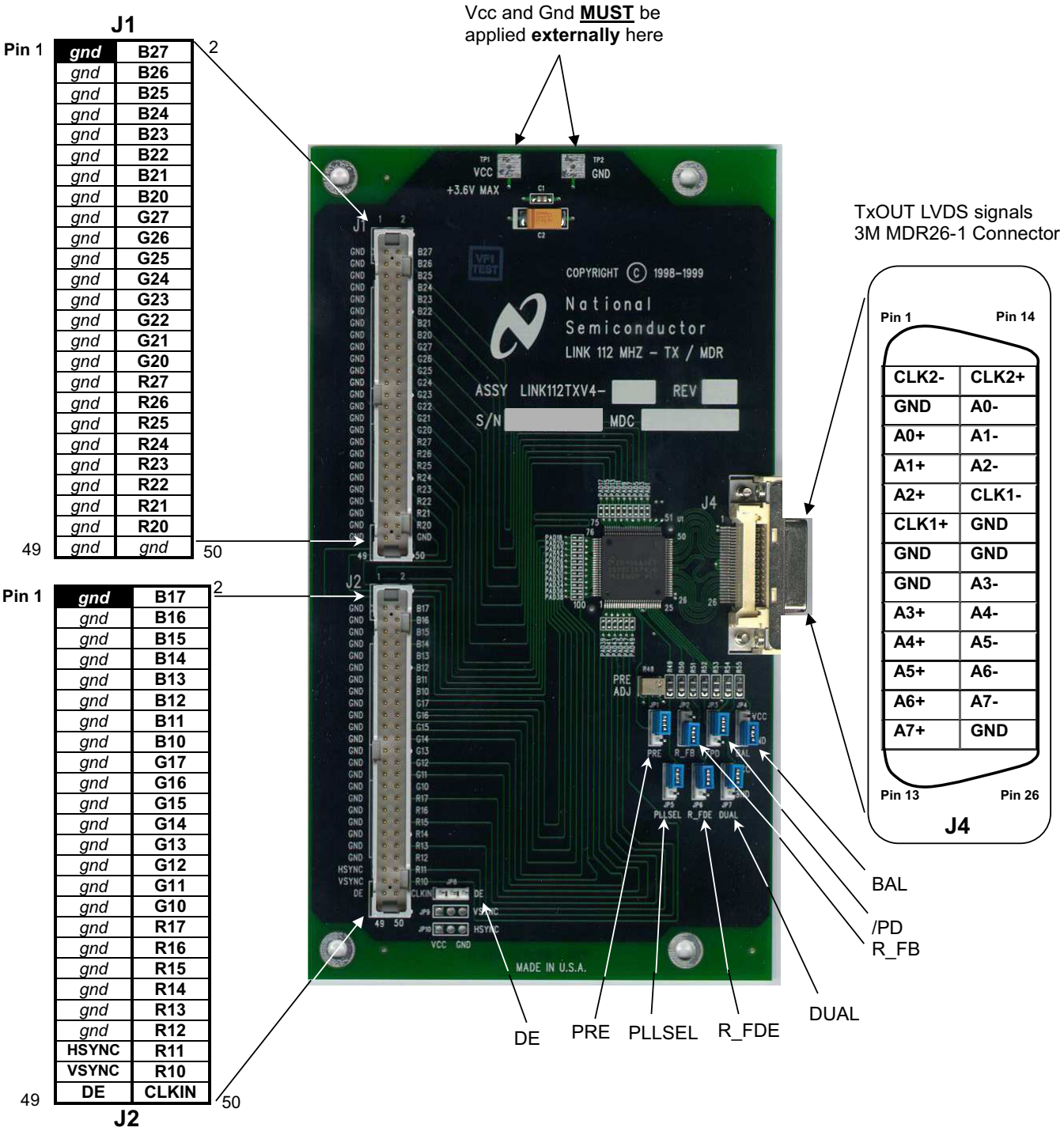
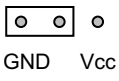
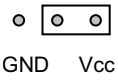
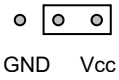
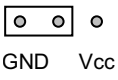
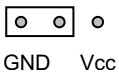
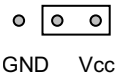
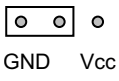
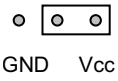
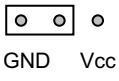
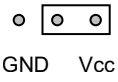
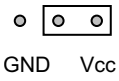
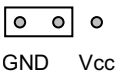
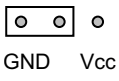
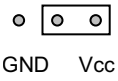


Figure 2. Transmitter Board

8 Tx Board Jumper Definition

Table 1. Tx Board Jumper Definition(1)

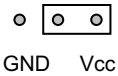
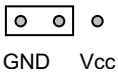
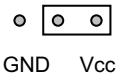
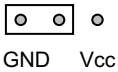
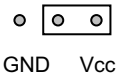
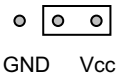
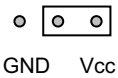
Jumper	Purpose	Settings
PRE (JP1)	**PRE**-emphasis	 = NONE  = ON GND Vcc GND Vcc (NONE: NO pre-emphasis; ON: pre-emphasis is adjusted through R48) When NO jumper is used, pre-emphasis is at 0.7 V value.
R_FB (JP2)	**R**ising or **F**alling Data Strobe	 = Rising  = Falling GND Vcc GND Vcc
/PD (JP3)	**P**ower **D**own	 = OFF  = ON GND Vcc GND Vcc (OFF: Tx powers down; ON: Tx is operational)
BAL (JP4)	DC **BAL**ance	 = OFF  = ON GND Vcc GND Vcc (Old Mode DC Balance OFF; New Mode DC Balance ON)
PLLSEL (JP5)	**PLL SEL**ect (auto-range)	 = LOW  = High GND Vcc GND Vcc (LOW: auto-range OFF; HIGH: auto-range ON)
R_FDE (JP6)	**R**ising or **F**alling **D**ata **E**nable(1)	 = Rising  = Falling GND Vcc GND Vcc
DUAL (JP7)	**DUAL**/single mode	 = Single  = Dual GND Vcc GND Vcc (When NO jumper is used, it is in Single to Dual Mode.)

(1) In Old Mode, the R_FDE pin is ignored by both the Tx and Rx when operating in Single (DUAL=LOW) or DUAL (DUAL=HIGH) mode. When the transmitter is operating in Single-to-Dual Mode (DUAL=1/2 Vcc), the R_FDE pin must be set HIGH if active data when DE signal is HIGH. In New Mode, R_FDE pins of both Tx and Rx boards MUST set to HIGH if DE signal is High during active data. R_FDE pins must set to LOW when DE signal is LOW during active data.

9 Tx Board Jumper Default Settings

The default setting for the Tx board is set to Old Mode, Dual-pixel mode and with pre-emphasis.

Table 2. Tx Board Jumper Default Settings(1)

Jumper Name	Purpose	Settings	Jumper Number
PRE	**PRE**-emphasis(1)	 GND Vcc	JP1
R_FB	**R**ising or **F**alling Data Strobe	 GND Vcc	JP2
/PD	**P**ower **D**own	 GND Vcc	JP3
BAL	DC **BAL**ance (Old Mode)	 GND Vcc	JP4
PLLSEL	**PLL SEL**ect (auto-range)	 GND Vcc	JP5
R_FDE	**R**ising or **F**alling **D**ata **E**nable	 GND Vcc	JP6
DUAL	**DUAL**/single mode	 GND Vcc	JP7

(1) An adjustable potentiometer (2K Ω) is mounted at location R48. This allows pre-emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7 V. See Tx Features and Explanations - Pre-Emphasis for description of feature.

10 LVDS Mapping by IDC Connector

The following two figures show how the Tx inputs are mapped to the IDC connector (It is also printed on the demo boards.) and to each of the eight LVDS channels. Note: Refer to AN-1127 for suggested mapping schemes.

Mapping for Old Mode (Transmitter Board)

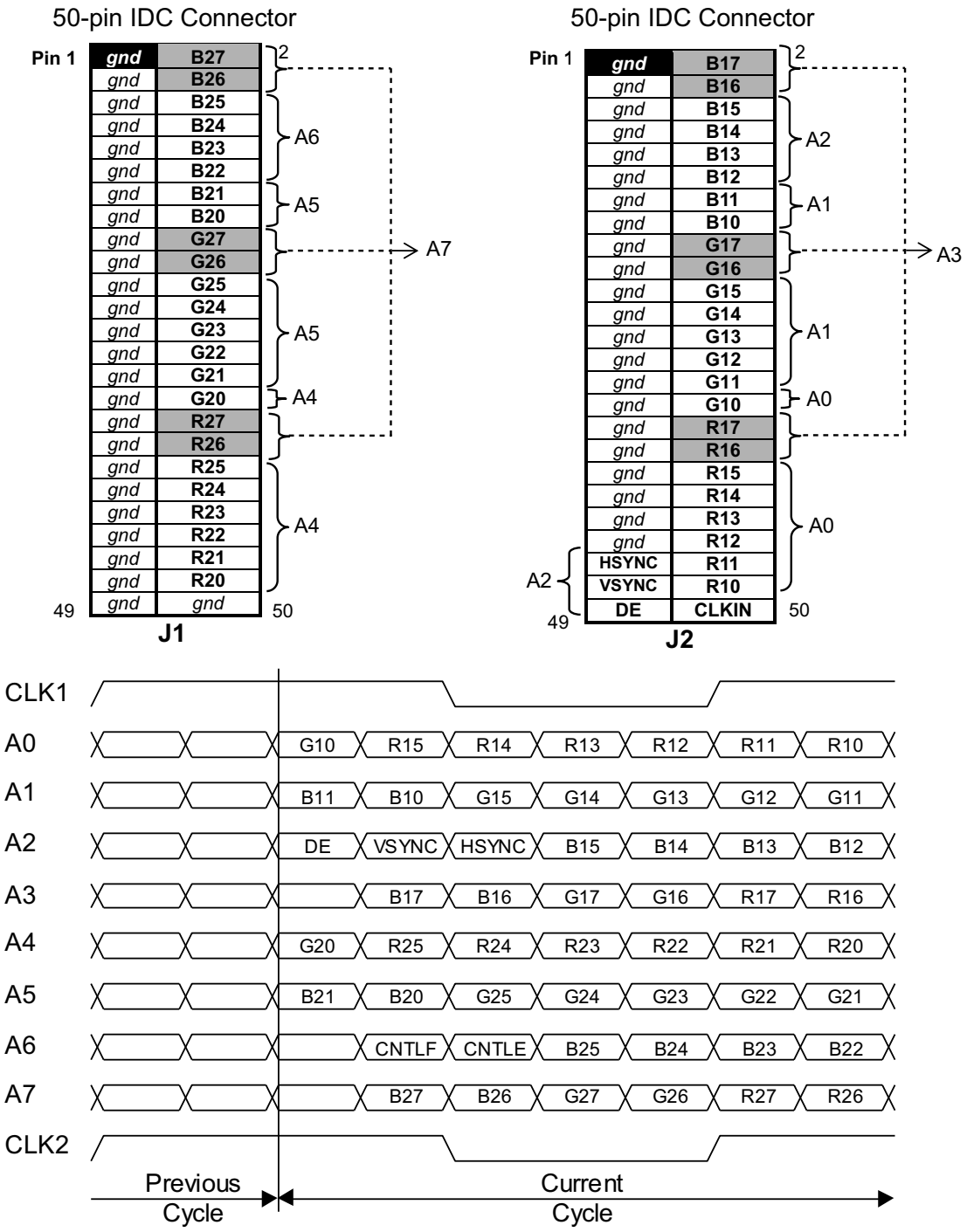
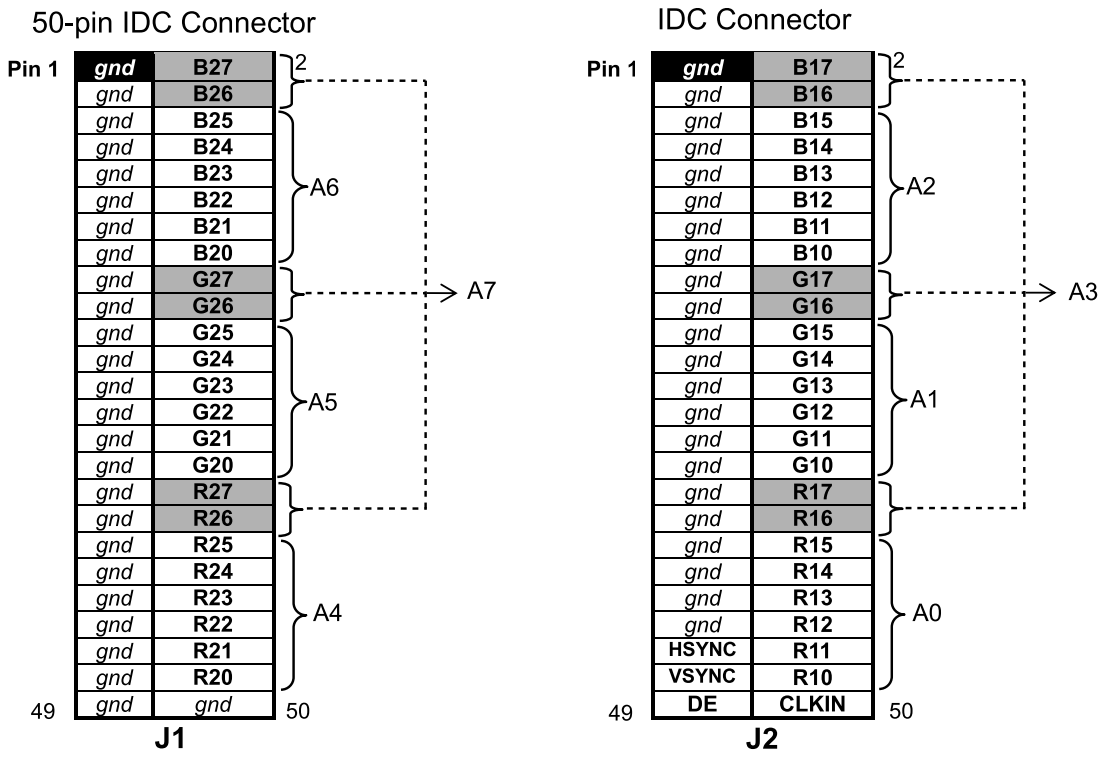


Figure 3. Mapping for Old Mode (Transmitter Board)

Figure 4. Mapping for New Mode (Transmitter Board)



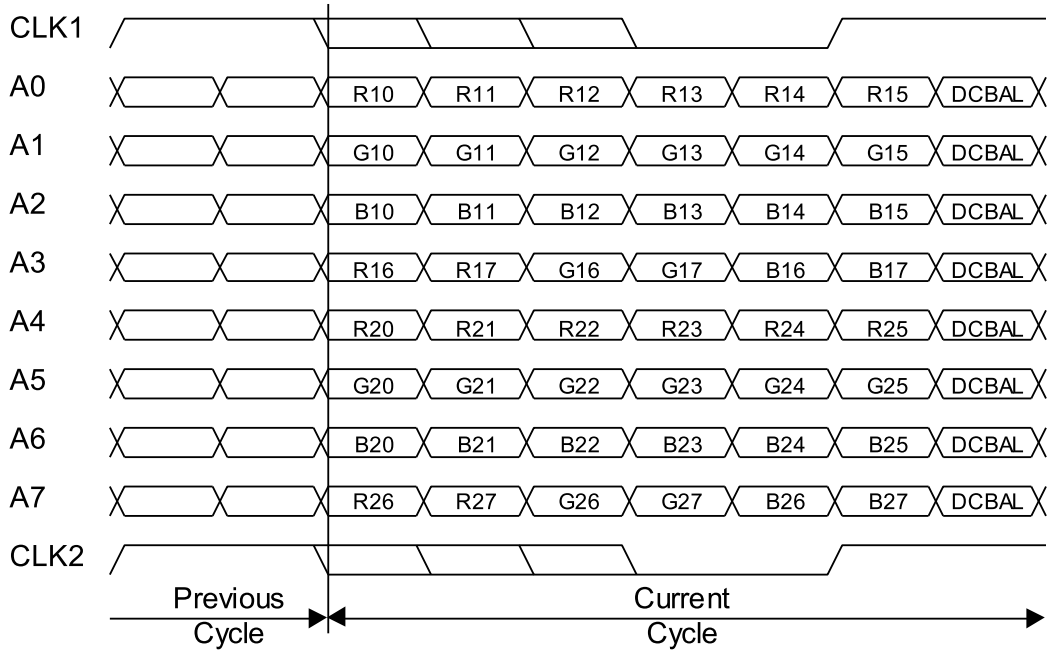


Figure 5. Mapping for New Mode (Transmitter Board)

11 Tx Optional: Parallel Termination for TxIN

On the Tx demo board, there are 50 inputs that have an 0402 pad on one side and the other side tied to ground. These pads are unpopulated from the factory but are provided if the user needs to adjust the input termination to match the impedance of the input signal. PAD1 TO PAD48 and PAD50 to PAD52 are associated with the Tx data input lines. PAD49 is associated with CLKIN.

Mapping for Transmitter Inputs for the Optional Parallel Termination Resistors:

Mapping for Transmitter Inputs for the Optional Parallel Termination Resistors

Tx Pin Names	Tx Pin Number	Parallel Termination Resistor		Tx Pin Names	Tx Pin Number	Parallel Termination Resistor
R10	10	PAD48		R22	80	PAD22
R11	9	PAD47		R23	79	PAD21
R12	8	PAD46		R24	78	PAD20
R13	7	PAD45		R25	77	PAD19
R14	6	PAD44		R26	76	PAD18
R15	5	PAD43		R27	75	PAD17
R16	4	PAD42		G20	74	PAD16
R17	3	PAD41		G21	73	PAD15
G10	2	PAD40		G22	72	PAD14
G11	1	PAD39		G23	71	PAD13
G12	100	PAD38		G24	70	PAD12
G13	99	PAD37		G25	69	PAD11
G14	96	PAD36		G26	66	PAD10
G15	95	PAD35		G27	65	PAD9
G16	94	PAD34		B20	64	PAD8
G17	93	PAD33		B21	63	PAD7
B10	92	PAD32		B22	62	PAD6
B11	91	PAD31		B23	61	PAD5
B12	90	PAD30		B24	60	PAD4
B13	89	PAD29		B25	59	PAD3
B14	88	PAD28		B26	58	PAD2
B15	87	PAD27		B27	57	PAD1
B16	86	PAD26		DE	56	PAD50
B17	85	PAD25		VSYNC	55	PAD51
R20	84	PAD24		HSYNC	54	PAD52
R21	81	PAD23		CLKIN	11	PAD49

BOM (Bill of Materials)

LDI3V8BT-112 TX BOM

Type	Pattern	Value	Designators
3M_MDR_D26-1 Qty = 1			J4
3_PIN_HEADER Qty = 10	.1" spacing		JP1 JP2 JP3 JP4 JP5 JP6 JP7 JP8 JP9 JP10
25X2_IDC_CONN Qty = 2			J1 J2
PAD Qty = 52	0402 (See previous page)	Optional	PAD1 PAD2 PAD3 PAD4 PAD5 PAD6 PAD7 PAD8 PAD9 PAD10 PAD11 PAD12 PAD13 PAD14 PAD15 PAD16 PAD17 PAD18 PAD19 PAD20 PAD21 PAD22 PAD23 PAD24 PAD25 PAD26 PAD27 PAD28 PAD29 PAD30 PAD31 PAD32 PAD33 PAD34 PAD35 PAD36 PAD37 PAD38 PAD39 PAD40 PAD41 PAD42 PAD43 PAD44 PAD45 PAD46 PAD47 PAD48 PAD49 PAD50 PAD51 PAD52
CAP Qty = 2	CC0805	.001uF	C4 C10
CAP Qty = 4	CC0805	.01uF	C5 C6 C8 C11
CAP Qty = 5	CC0805	.1uF	C1 C3 C7 C9 C12
DS90C387 Qty = 1			U1
POT Qty = 1		10 KΩ	R48
RES Qty = 7		10 Ω	R49 R50 R51 R52 R53 R54 R55
TESTPAD_.2"X.2" Qty = 2			TP1 TP2
CAP100P Qty = 4	CAP100P	10uF	C2 C13 C14 C15

12 Receiver Board

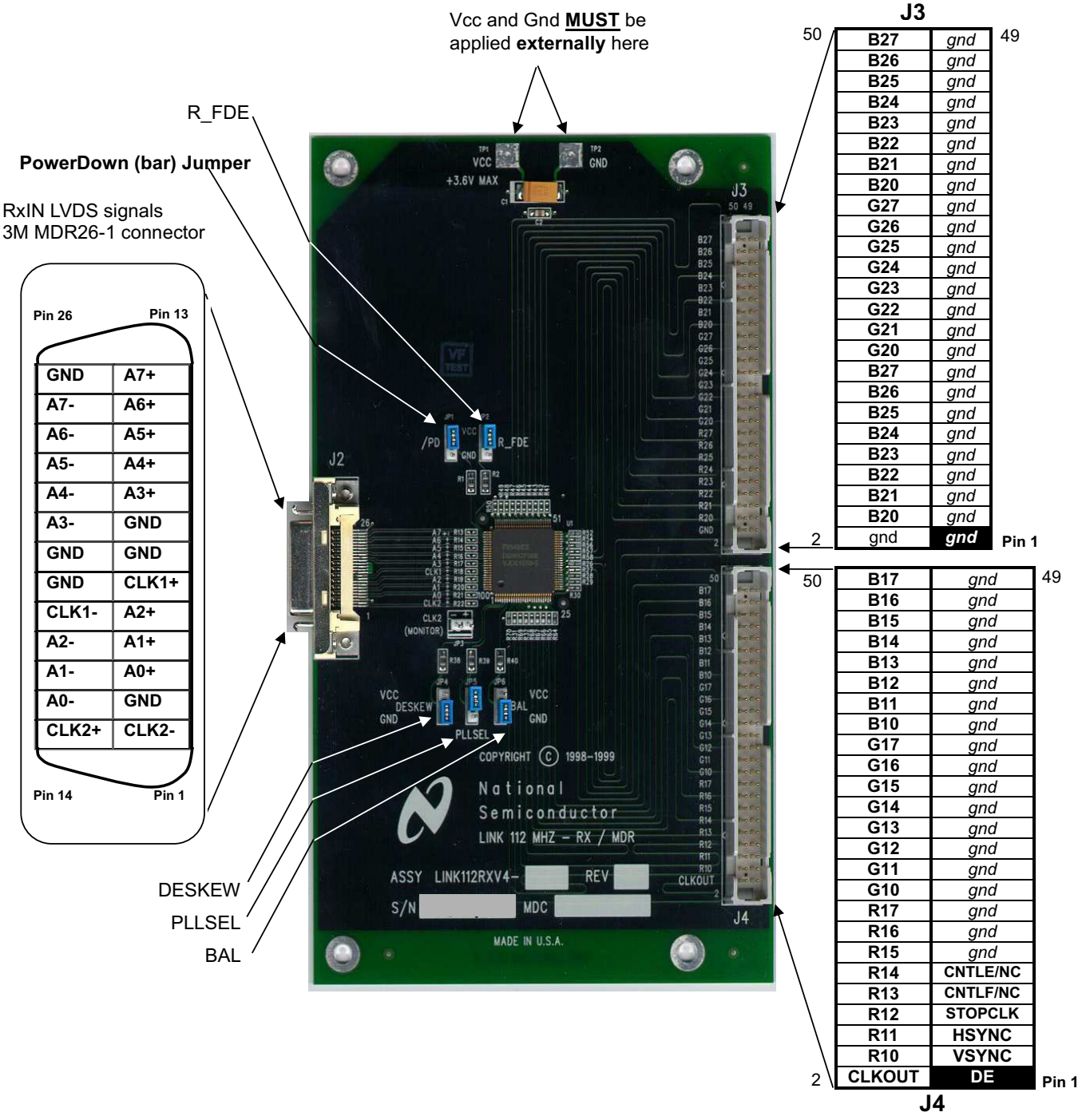
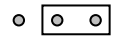
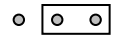
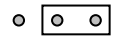


Figure 6. Receiver Board

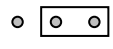
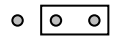
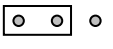
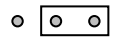
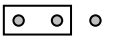
13 Rx Board Jumper Definition

Table 3.

Jumper	Purpose	Settings
/PD (JP1)	**P**ower**D**own	 = OFF GND Vcc  = ON GND Vcc (OFF Tx powers down; ON Tx is operational)
R_FDE (JP2)	**R**ising or **F**alling **D**ata **E**nable	 = Falling GND Vcc  = Rising GND Vcc
DESKEW (JP4)	**DESKEW**	 = OFF GND Vcc  = ON GND Vcc
PLLSEL (JP5)	**PLL SEL**ect (auto range)	 = OFF GND Vcc  = ON GND Vcc
BAL (JP6)	DC **BAL**ance	 = OFF GND Vcc  = ON GND Vcc (Old Mode DC Balance OFF; New Mode DC Balance ON)

14 Rx Board Jumper Default Settings

Table 4.

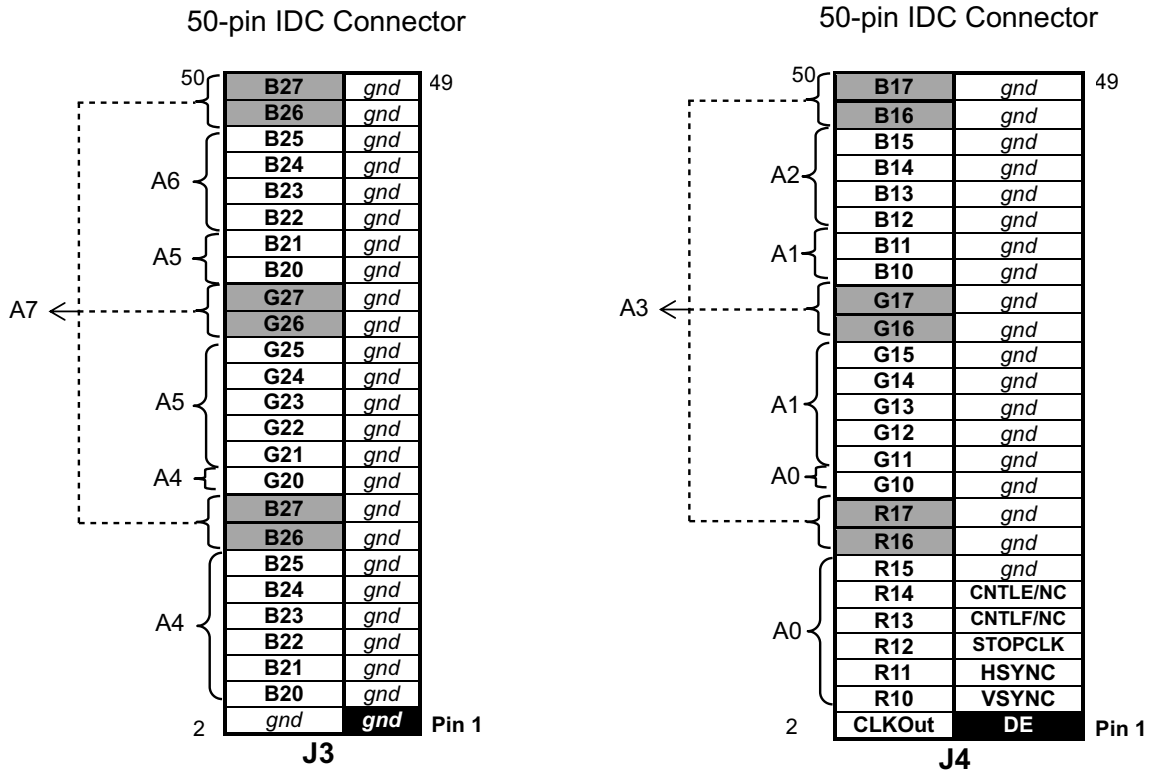
Jumper	Purpose	Settings	Jumper Number
/PD	**P**ower**D**own -- ON (Part is enabled)	 GND Vcc	JP1
R_FDE	**R**ising or **F**alling **D**ata **E**nable	 GND Vcc	JP2
DESKEW	**DESKEW**	 GND Vcc	JP4
PLLSEL	**PLL SEL**ect (auto range)	 GND Vcc	JP5
BAL	DC **BAL**ance	 GND Vcc	JP6

15 LVDS Mapping by IDC Connector

The following two figures show how the Rx outputs are mapped to the IDC connector and to each of the eight LVDS channels.

Note: Refer to AN-1127 for suggested mapping schemes.

Figure 7. Mapping for Old Mode (Receiver Board)



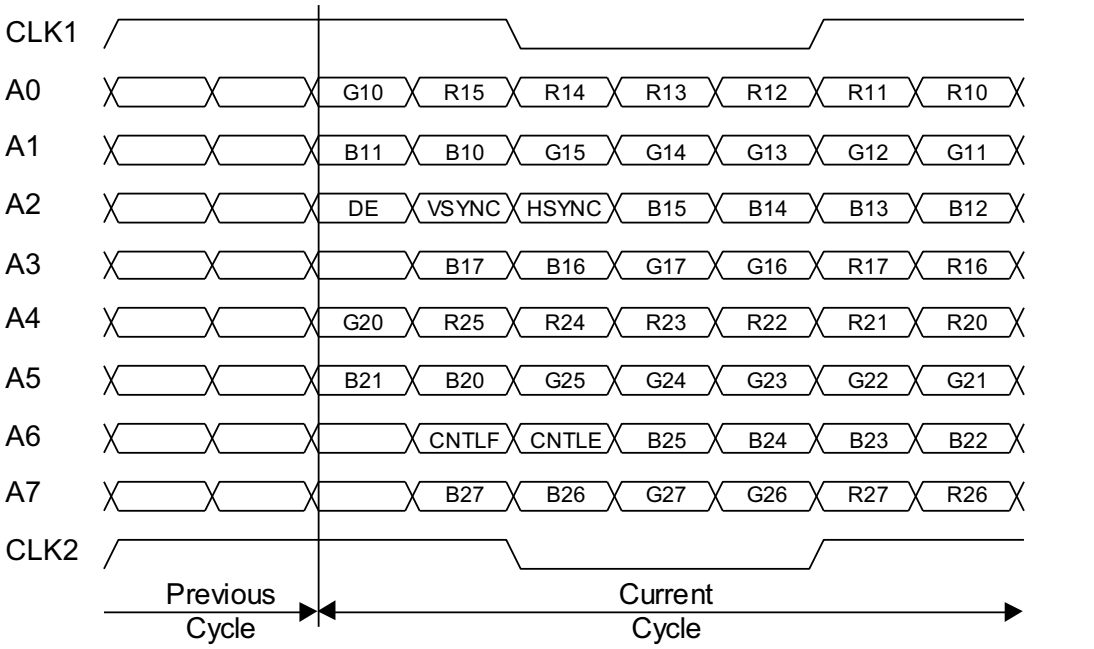
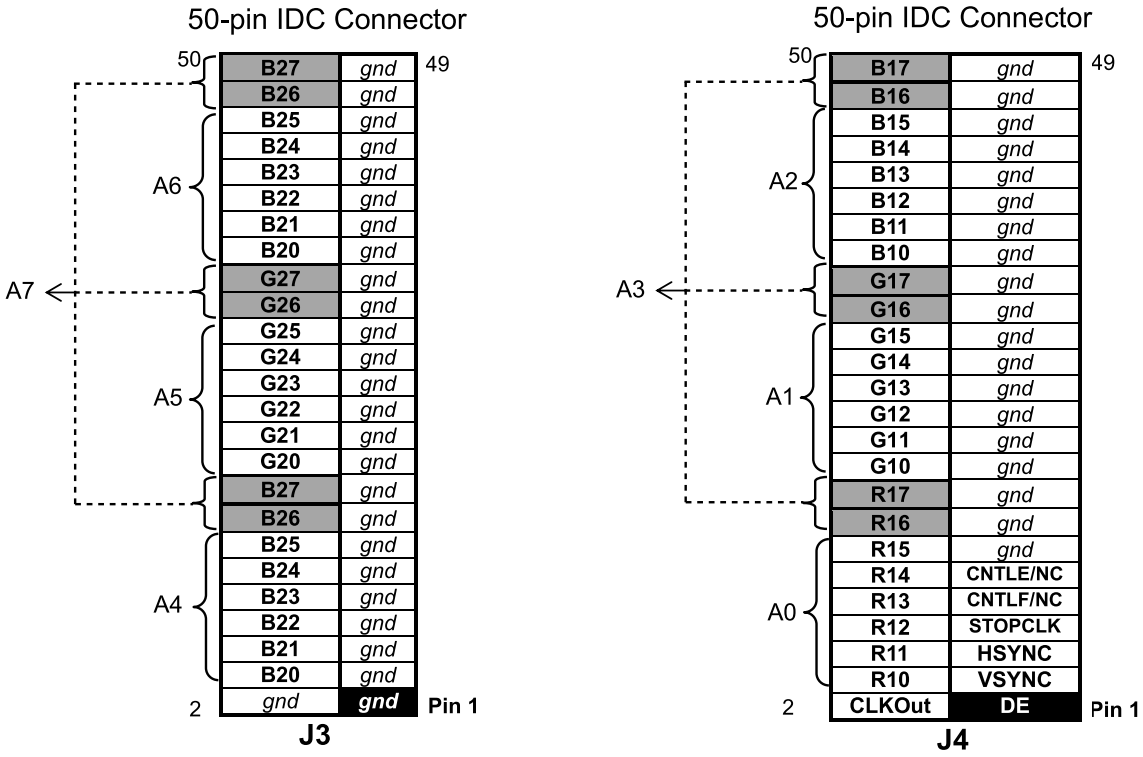


Figure 8. Mapping for Old Mode (Receiver Board)

Mapping for New Mode (Receiver Board)



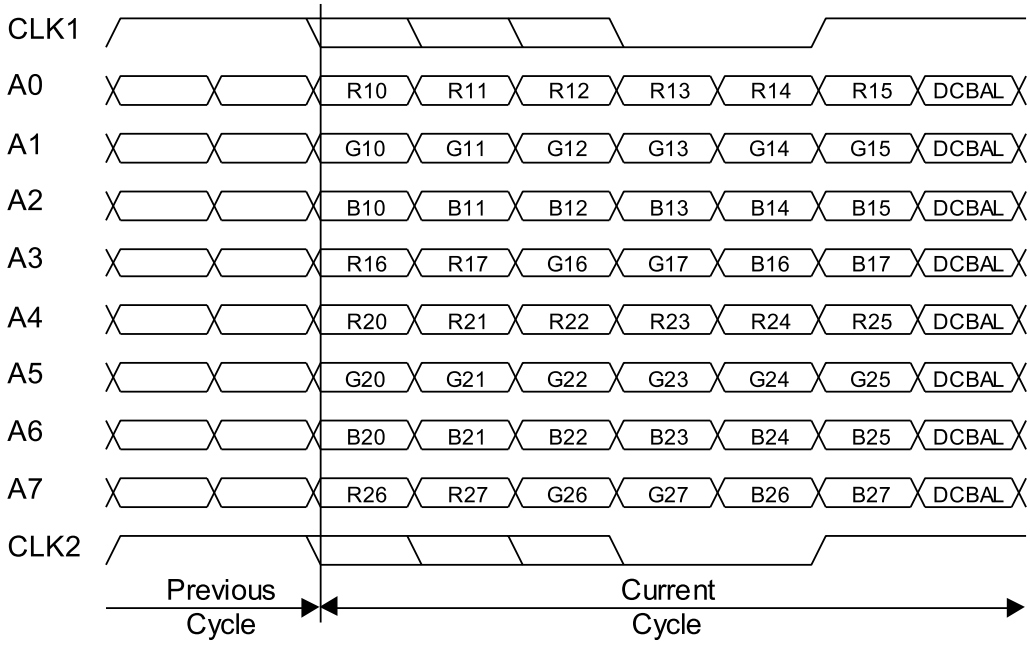


Figure 9.

Rx Optional: Series Termination for RxOut

On the Rx demo board there are 49 outputs that have an 0402 pad in series (but shorted). These pads are unpopulated from the factory but are provided if the user needs to adjust the output series termination to match the impedance of an input line the user must cut the short out before mounting a series resistor. R6-R12, R24-R37, R41-R70 are associated with the DATA input lines. R23 is associated with CLKOUT.

Rx Pin Names	Rx Pin Number	Parallel Termination Resistor		Rx Pin Names	Rx Pin Number	Parallel Termination Resistor
R10	8	R70		R24	43	R56
R11	9	R31		R25	46	R55
R12	10	R69		R26	47	R54
R13	11	R32		R27	48	R53
R14	12	R68		G20	49	R52
R15	14	R33		G21	50	R51
R16	15	R67		G22	51	R41
R17	17	R34		G23	52	R12
G10	18	R66		G24	53	R42
G11	19	R35		G25	55	R11
G12	20	R65		G26	57	R43
G13	21	R36		G27	58	R10
G14	22	R64		B20	59	R44
G15	24	R37		B21	60	R9
G16	26	R30		B22	61	R45
G17	27	R63		B23	62	R8
B10	28	R29		B24	64	R46
B11	29	R62		B25	65	R7
B12	30	R28		B26	67	R47
B13	31	R61		B27	68	R6
B14	32	R27		DE	69	R48
B15	34	R60		VSYNC	70	R5
B16	36	R26		HSYNC	71	R49
B17	37	R59		STOPCLK	73	R4
R20	38	R58		CNTLF/NC	74	R50
R21	39	R25		CNTLE/NC	75	R3
R22	40	R57				
R23	41	R24		CLKOUT	42	R23

BOM (Bill of Materials)

LDI3V8BT-112 RX BOM

Type	Pattern	Value	Designators
2_PIN_HEADER Qty = 1	.1" spacing		JP3
3M_MDR_D26--1 Qty = 1			J2
3_PIN_HEADER Qty = 5	.1" spacing		JP1 JP2 JP4 JP5 JP6
25X2_IDC_R Qty = 2			J3 J4
PAD Qty = 6	402	Shorted	PAD1 PAD2 PAD3 PAD4 PAD5 PAD6
CAP Qty = 2	CC0805	.001 uF	C4 C10
Qty = 4	CC0805	.01 uF	C5 C6 C8 C11
Qty = 5	CC0805	.1 uF	C2 C3 C7 C9 C12
DS90CF388 Qty = 1			U1
R0402 Qty = 55	Optional (See previous page)		R3 R4 R5 R6 R7 R8 R9 R10 R11 R12 R23 R24 R25 R26 R27 R28 R29 R30 R31 R32 R33 R34 R35 R36 R37 R41 R42 R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R55 R56 R57 R58 R59 R60 R61 R62 R63 R64 R65 R66 R67 R68 R69 R70
RES Qty = 10		100 Ω	R13 R14 R15 R16 R17 R18 R19 R20 R21 R22
Qty = 5		10 Ω	R1 R2 R38 R39 R40
TESTPAD_.2"X.2" Qty = 2			TP1 TP2
CAP100P Qty = 4	CAP100P	10 uF	C1 C13 C14 C15

Jumper Setting Examples 1 (Old Mode)

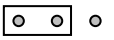
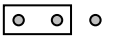
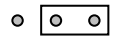
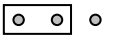
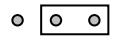
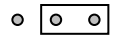
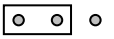
The LDI chipset supports up to 24-bit single pixel and 24-bit dual pixel formats. The following examples show how to set the jumpers for a specific pixel format in Old Mode.

18-bit or 24-bit Single Pixel (Old Mode)

The jumper settings below are for Old Mode, Single to Single pixel application.

For Tx board: (**For Rx board** jumper settings in this application, see Rx Board Jumper Default Settings)

Tx Board settings[1][2]

Jumper	Purpose	Settings	Jumper Number
PRE	**PRE**-Emphasis[3]	 GND Vcc	JP1
R_FB	**R**ising or **F**alling data strobe	 GND Vcc	JP2
/PD	**P**ower**D**own	 GND Vcc	JP3
BAL	DC **BAL**ance	 GND Vcc	JP4
PLLSEL	**PLL SEL**ect (auto range)	 GND Vcc	JP5
R_FDE	**R**ising or **F**alling **D**ata **E**nable[4]	 GND Vcc	JP6
DUAL	**DUAL**/single mode	 GND Vcc	JP7

(1) In the single pixel mode, only TxOUT0 through TxOUT3 (LVDS channels A0-A3) and their associated inputs are active. TxOUT4 through TxOUT7 and their associated inputs and CLK2 are disabled for power savings.

(2) "Old Mode" is backward compatible to existing FPD-Link technology.

(3) An adjustable potentiometer (2K ohm) is mounted at location R48. This allows pre- emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7 V. See Section 3.1.1 for description of feature.

(4) In Old Mode, R_FDE can be set HIGH or LOW.

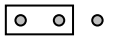
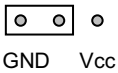
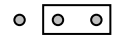
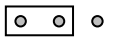
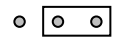
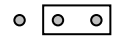
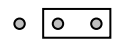
18-bit or 24-bit Dual Pixel (Old Mode)

(Default Setting from the factory)

The jumper settings below are for Old Mode, Dual to Dual pixel application.

For Tx board: (**For Rx board** jumper settings in this application, see Rx Board Jumper Settings).

18-bit or 24-bit Dual Pixel (Old Mode)

Jumper	Purpose	Settings	Jumper Number
PRE	**PRE**-Emphasis[1]	 GND Vcc	JP1
R_FB	**R**ising or **F**alling data strobe	 GND Vcc	JP2
/PD	**P**ower**D**own	 GND Vcc	JP3
BAL	DC **BAL**ance	 GND Vcc	JP4
PLLSEL	**PLL SEL**ect (auto range)	 GND Vcc	JP5
R_FDE	**R**ising or **F**alling **D**ata **E**nable[2]	 GND Vcc	JP6
DUAL	**DUAL**/single mode	 GND Vcc	JP7

(1) An adjustable potentiometer (2K ohm) is mounted at location R48. This allows pre- emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7V. See Section 3.1.1 for description of feature.

(2) In Old Mode, R_FDE can be set HIGH or LOW.

Jumper Setting Example 2 (New Mode)

The LDI chipset supports up to 24-bit single pixel and 24-bit dual pixel formats. The following examples show how to set the jumper for a specific pixel format in New Mode.

18-bit or 24-bit Single Pixel (New Mode)

The jumper settings below are for New Mode, Single to Single pixel application.

For Tx board: (**The Rx board** jumper settings in this application is the same as Rx Board Jumper Default Settings except the BAL pin(JP6), which must be set to Vcc.)

Table 5. 18-bit or 24-bit Single Pixel (New Mode)(1)

Jumper	Purpose	Settings	Jumper Number
PRE	**PRE**-Emphasis(2)	GND Vcc	JP1
R_FB	**R**ising or **F**alling data strobe	GND Vcc	JP2
/PD	**P**ower**D**own	GND Vcc	JP3
BAL	DC **BAL**ance	GND Vcc	JP4
PLLSEL	**PLL SEL**ect (auto range)	GND Vcc	JP5
R_FDE	**R**ising or **F**alling **D**ata **E**nable(3)	GND Vcc	JP6
DUAL	**DUAL**/single mode	GND Vcc	JP7

(1) In the single pixel mode, only TxOUT0 through TxOUT3 (LVDS channels A0-A3) and their associated inputs are active. TxOUT4 through TxOUT7 and their associated inputs and CLK2 are disabled for power savings.

(2) An adjustable potentiometer (2K Ω) is mounted at location R48. This allows pre- emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7 V.

(3) In Balanced Mode (New Mode), R_FDE pin (pin 21) MUST be set to HIGH if DE signal (pin 56) is HIGH during active data. R_FDE pin must set to LOW when DE signal is LOW during active data.

16 18-bit or 24-bit Dual Pixel (New Mode)

The jumper settings below are for New Mode, Dual to Dual pixel application.

For Tx Board: (**The Rx board** jumper settings in this application is the same as the Rx Board Jumper Default Settings on page 17 except the BAL pin(JP6), which must be set to Vcc.)

Table 6. 18-bit or 24-bit Dual Pixel (New Mode)

Jumper	Purpose	Settings	Jumper Number
PRE	**PRE**-Emphasis[1]	GND Vcc	JP1
R_FB	**R**ising or **F**alling data strobe	GND Vcc	JP2
/PD	**P**ower**D**own	GND Vcc	JP3
BAL	DC **BAL**ance (New Mode)	GND Vcc	JP4
PLLSEL	**PLL SEL**ect (auto range)	GND Vcc	JP5
R_FDE	**R**ising or **F**alling **D**ata **E**nable[2]	GND Vcc	JP6
DUAL	**DUAL**/single mode	GND Vcc	JP7

(1) An adjustable potentiometer (2K ohm) is mounted at location R48. This allows pre-emphasis to be adjusted (only if JP1 has a jumper to VCC). Use a number 1.4mm jewelers screwdriver to adjust R48. Turning clockwise will increase the pre-emphasis value. Turning counterclockwise will decrease the pre-emphasis value. R48 should be adjusted to reduce overshoot. If no jumper is used, the pre-emphasis value will be 0.7V. See Tx Features and Explanations - Pre-Emphasis for description of feature.

(2) In Balanced Mode (New Mode), R_FDE pin (pin 21) MUST be set to HIGH if DE signal (pin 56) is HIGH during active data. R_FDE pin must set to LOW when DE signal is LOW during active data.

17 Troubleshooting

If the demo boards are not performing properly, use the following as a guide for quick solutions to common problems. If the problem persists, contact the hotline number listed under Additional Information section of this document.

Check the following:

1. Power and Ground are connected to both Tx AND Rx boards
2. Supply voltage (typical 3.3 V) and current (It's around 200 mA with clock and one data bit at 66 MHz.) are correct.
3. Input clock and input data (It's best to start with one data bit.) to the Tx board.
4. Jumpers are set correctly or to default settings.
5. The 2 meter cable is connecting the Tx and Rx boards.
6. Make sure all of the connections are good.
7. Start with a low clock frequency (40 or 66 MHz) and work from there.

Trouble shooting chart:

Table 7. Troubleshooting Chart

Problem	Solution
There is only the output clock. There is no output data.	Make sure the data scramble/mapping is correct. Make sure there is data input.
No output data and clock.	Make sure Power is on. Input data and clock are active and connected correctly. Make sure that the 2 meter cable is secured to both demo boards.
Power, ground, input data and input clock are connected correctly, but no outputs.	Check the Power Down pins of both boards and make sure the devices are enabled (/PD=ON) for operation.
The devices are pulling more than 1A of current.	Check for shorts on the demo boards.
After powering up the demo boards, the power supply reads less than 3 V when it is set to 3.3 V.	Use a larger power supply that will provide enough current for the demo boards.

18 Additional Information

For more information on FPD-Link Transmitters/Receivers and other Interface products, refer to the Texas Instruments URL: http://www.ti.com/lsds/ti/analog/interface/interface.page

18.1 Application Notes

- AN-971 An Overview of LVDS technology
- AN-1032 An Introduction to FPD-Link
- AN-1127 LVDS Display Interface TFT Data Mapping for Interoperability with FPD-Link
- AN-1163 TFT Data Mapping for Dual Pixel LDI Application - Alternate A - Color Map
- AN-1085 FPD-Link PCB and Interconnect Design-In Guidelines
- AN-977 LVDS Signal Quality: Jitter measurement using Eye pattern
- AN-977 LVDS Signal Quality: Jitter measurement using Eye pattern
- AN-1059 High Speed Transmission with LVDS Devices

SID'99 LDI Paper:

http://www.ti.com/lit/an/snla168/snla168.pdf

19 3M 26-Mini D Ribbon Cable and Connector

The next few pages provide a full description of the cable and connector. For product request please contact 3M.

3M Cable and Connector Data is available at: http://www.mmm.com/Interconnects

Revision History

DATE	CHANGES
April 2014	Converted to TI User Guide format.
January 2014	• Removed cables from parts included with the kit. • Updated 3M datasheet information. • Updated contact info and links to reflect TI references.
2001	Included EVK schematic with documentation.
1999	• Updated 3M datasheet information. • Updated Transmitter/Receiver Rev 4 demo board schematics.
1999	The first version of the LDI3V8BT 112MHz evaluation boards documentation.

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3. User agrees that EVMs shall not be used as, or incorporated into, all or any part of a finished product.
4. User agrees and acknowledges that certain EVMs may not be designed or manufactured by TI.
5. User must read the user's guide and all other documentation accompanying EVMs, including without limitation any warning or restriction notices, prior to handling and/or using EVMs. Such notices contain important safety information related to, for example, temperatures and voltages. For additional information on TI's environmental and/or safety programs, please visit www.ti.com/esh or contact TI.
6. User assumes all responsibility, obligation, and any corresponding liability for proper and safe handling and use of EVMs.
7. Should any EVM not meet the specifications indicated in the user's guide or other documentation accompanying such EVM, the EVM may be returned to TI within 30 days from the date of delivery for a full refund. THE FOREGOING LIMITED WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY TI TO USER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE. TI SHALL NOT BE LIABLE TO USER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES RELATED TO THE HANDLING OR USE OF ANY EVM.
8. No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which EVMs might be or are used. TI currently deals with a variety of customers, and therefore TI's arrangement with the user is not exclusive. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services with respect to the handling or use of EVMs.
9. User assumes sole responsibility to determine whether EVMs may be subject to any applicable federal, state, or local laws and regulatory requirements (including but not limited to U.S. Food and Drug Administration regulations, if applicable) related to its handling and use of EVMs and, if applicable, compliance in all respects with such laws and regulations.
10. User has sole responsibility to ensure the safety of any activities to be conducted by it and its employees, affiliates, contractors or designees, with respect to handling and using EVMs. Further, user is responsible to ensure that any interfaces (electronic and/or mechanical) between EVMs and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
11. User shall employ reasonable safeguards to ensure that user's use of EVMs will not result in any property damage, injury or death, even if EVMs should fail to perform as described or expected.
12. User shall be solely responsible for proper disposal and recycling of EVMs consistent with all applicable federal, state, and local requirements.

Certain Instructions. User shall operate EVMs within TI's recommended specifications and environmental considerations per the user's guide, accompanying documentation, and any other applicable requirements. Exceeding the specified ratings (including but not limited to input and output voltage, current, power, and environmental ranges) for EVMs may cause property damage, personal injury or death. If there are questions concerning these ratings, user should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the applicable EVM user's guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using EVMs' schematics located in the applicable EVM user's guide. When placing measurement probes near EVMs during normal operation, please be aware that EVMs may become very warm. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use EVMs.

Agreement to Defend, Indemnify and Hold Harmless. User agrees to defend, indemnify, and hold TI, its directors, officers, employees, agents, representatives, affiliates, licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of, or in connection with, any handling and/or use of EVMs. User's indemnity shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if EVMs fail to perform as described or expected.

Safety-Critical or Life-Critical Applications. If user intends to use EVMs in evaluations of safety critical applications (such as life support), and a failure of a TI product considered for purchase by user for use in user's product would reasonably be expected to cause severe personal injury or death such as devices which are classified as FDA Class III or similar classification, then user must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

RADIO FREQUENCY REGULATORY COMPLIANCE INFORMATION FOR EVALUATION MODULES

Texas Instruments Incorporated (TI) evaluation boards, kits, and/or modules (EVMs) and/or accompanying hardware that is marketed, sold, or loaned to users may or may not be subject to radio frequency regulations in specific countries.

General Statement for EVMs Not Including a Radio

For EVMs not including a radio and not subject to the U.S. Federal Communications Commission (FCC) or Industry Canada (IC) regulations, TI intends EVMs to be used only for engineering development, demonstration, or evaluation purposes. EVMs are not finished products typically fit for general consumer use. EVMs may nonetheless generate, use, or radiate radio frequency energy, but have not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or the ICES-003 rules. Operation of such EVMs may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: For EVMs including a radio, the radio included in such EVMs is intended for development and/or professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability in such EVMs and their development application(s) must comply with local laws governing radio spectrum allocation and power limits for such EVMs. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by TI unless user has obtained appropriate experimental and/or development licenses from local regulatory authorities, which is the sole responsibility of the user, including its acceptable authorization.

U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Important Notice for Users of EVMs Considered "Radio Frequency Products" in Japan

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

http://www.tij.co.jp

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In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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