12 + 1 Gamma/V_{COM} Reference with Regulator

ADD8707

FEATURES

Integrated voltage regulator
Mask programmable gamma resistors: 0.2% resolution
Upper/lower buffers swing to V_{DD}/GND
Single-supply operation: 7.5 V to 16 V
Continuous gamma current drive: 15 mA
High peak V_{COM} output current: 250 mA
Low offset voltage: 15 mV max
Output voltage stable under transient load conditions
48-lead Pb-free LFCSP package

APPLICATIONS

TFT LCD monitor panels
TFT LCD TV panels

FUNCTIONAL BLOCK DIAGRAM

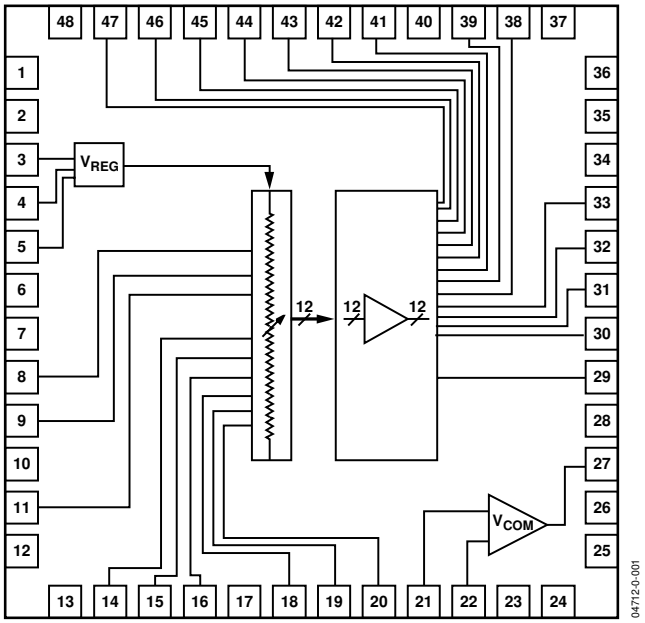

Figure 1. 48-Lead LFCSP

PRODUCT OVERVIEW

The ADD8707 is a 12-channel, integrated gamma reference with V_{COM} for use in high resolution TFT LCD monitor and TV panels. The output buffers feature low offset voltage and high current drive under transient load conditions to provide an accurate and stable gamma curve. Two channels swing to VDD and two channels swing to GND, increasing the overall range of the curve. A novel approach is used to reduce the external component count while increasing accuracy by integrating the gamma setup resistors. To accommodate multiple column drivers and panel architectures, the internal resistor string is mask-programmable, and the tap points are externally accessible. An on-board voltage regulator minimizes supply ripple to provide a fixed point for the resistor string. Here again, external component costs are reduced and the quality of the gray scale is increased.

The ADD8707 is specified over the temperature range of –40°C to +100°C and comes in a robust, low cost, lead frame chip scale package.

Rev. 0

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REVISION HISTORY

7/04—Revision 0: Initial Version

ELECTRICAL CHARACTERISTICS

V_{DD} = 16 V, T_A @ +25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
POWER SUPPLY						
Supply Voltage	V_{DD}		7.5		16	V
Supply Current	I_{SYS}	No load		8.3	13	mA
		−20°C ≤ T_A ≤ +105°C			15	mA
Power Supply Rejection Ratio	PSRR	V_{DD} = 7 V to 17 V, −20°C ≤ T_A ≤ +105°C	68	90		dB
VOLTAGE REGULATOR						
Dropout Voltage	ΔV_{DO}	I_L = 100 µA		100	150	mV
		I_L = 5 mA		310	350	mV
Line Regulation	REG_{LINE}	V_{IN} = 8.5 V to 16.5 V, V_{OUT} = 8V		0.01	0.20	%/V
Load Regulation	REG_{LOAD}	I_O = 100 µA to 10 mA		0.02	0.10	%/mA
Load Current	I_O			5		mA
Thermal Regulation	$Reg_{THERMAL}$			0.005		%/W
MASK-PROGRAMMABLE RESISTOR STRING						
Total Resistor String	R_{TOTAL}	# of segments = 500		15		kΩ
OUTPUT ACCURACY						
System Error[1, 2]	V_{SY} Error	−20°C ≤ T_A ≤ +105°C			3	%
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			5	15	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−20°C ≤ T_A ≤ +105°C		20		µV/°C
Input Bias Current	I_B			0.5	1.1	µA
		−20°C ≤ T_A ≤ +105°C			1.5	µA
Input Voltage Range			0		V_{DD}	V
Input Impedance	Z_{IN}			400		kΩ
Input Capacitance	C_{IN}			1		pF
BUFFER OUTPUT CHARACTERISTICS						
Output Performance (V1, V6, V7, V12)	ΔV	I_L = 20 mA, V_{DD} = 16 V		15		mV
Output Performance (V2 to V5, V8 to V11)	ΔV	I_L = 5 mA, V_{DD} = 16 V		5		mV
V_{COM} OUTPUT CHARACTERISTICS						
Output Performance	ΔV	I_L = 30 mA, V_{DD} = 16 V		10		mV
Continuous Output Current	I_{OUT}	V_{DD} = 16 V		50		mA
Peak Output Current	I_{PK}	V_{DD} = 16 V		250		mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, CL = 200 pF	4	6		V/µs
Bandwidth	BW	−3dB, R_L = 10 Ω, CL = 200 pF		4.5		MHz
Settling Time to 0.1%	t_S	1V, R_L = 10 kΩ, CL = 200 pF		1.1		µs
Phase Margin	ϕo	R_L = 10 kΩ, CL = 200 pF		55		Degrees

[1] System error is defined as the difference between the designed and actual output voltage divided by the regulator output voltage.
[2] System error includes regulator error, resistor string error, bias current effects, and buffer offset voltage.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{DD})	18 V
Input Voltage	-0.5 V to V_{DD}
Differential Input Voltage	V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range[1]	−40°C to +100°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C
ESD Tolerance (HBM)	±3000 V
ESD Tolerance (MM)	±100 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Thermal Resistance

Package Type	θ_{JA}[2]	θ_{JA}[3]	Unit
48-Lead LFCSP (CP)	28.3	47.7	°C/W

[1] See the Applications Information section.
[2] θ_{JA} for DAP soldered to JEDEC 4-layer board.
[3] θ_{JA} for DAP not soldered down.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

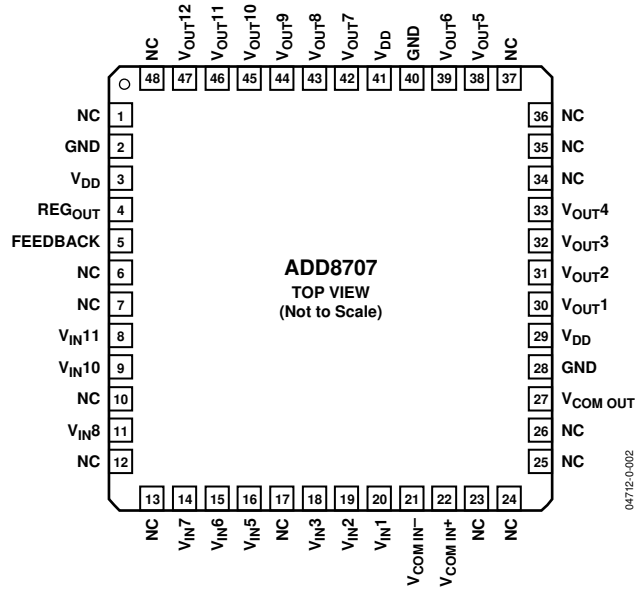

Figure 2. 48-Lead LFCSP

Table 4. Pin Function Descriptions

Pin No.	Name	Description
1	NC	
2	GND	Ground. Nominally 0 V.
3	V_{DD}	Supply voltage. Nominally 16 V.
4	REG_{OUT}	Provides reference voltage to resistor string.
5	FB	Compares a percentage of the regulator output to the internal voltage reference. Internal resistors are used to program the desired regulator output voltage.
6	NC	
7	NC	
8	$V_{IN}11$	Nominally floating. External resistors can be added to modify the internal resistor string to change the gamma voltage.
9	$V_{IN}10$	
10	NC	
11	$V_{IN}8$	Nominally floating. External resistors can be added to modify the internal resistor string to change the gamma voltage.
12	NC	
13	NC	
14	$V_{IN}7$	Nominally floating. External resistors can be added to modify the internal resistor string to change the gamma voltage.
15	$V_{IN}6$	
16	$V_{IN}5$	
17	NC	
18	$V_{IN}3$	Nominally floating. External resistors can be added to modify the internal resistor string to change the gamma voltage.
19	$V_{IN}2$	
20	$V_{IN}1$	
21	$V_{COM\ IN}-$	Negative input for the common voltage node.
22	$V_{COM\ IN}+$	Positive input for the common voltage node.
23	NC	
24	NC	
25	NC	
26	NC	
27	$V_{COM\ OUT}$	Output for the common node. Typical V_{OL} = 1.4 V. V_{OH} = 14.6 V.
28	GND	Ground. Nominally 0 V.

Pin No.	Name	Description
29	V_{DD}	Supply voltage. Nominally 16 V.
30	$V_{OUT}1$	Buffer output. Swings to negative rail.
31	$V_{OUT}2$	
32	$V_{OUT}3$	
33	$V_{OUT}4$	
34	NC	
35	NC	
36	NC	
37	NC	
38	$V_{OUT}5$	Buffer output. Swings to negative rail.
39	$V_{OUT}6$	
40	GND	Ground. Nominally 0 V.
41	V_{DD}	Supply voltage. Nominally 16 V.
42	$V_{OUT}7$	Buffer output. Swings to negative rail.
43	$V_{OUT}8$	
44	$V_{OUT}9$	
45	$V_{OUT}10$	
46	$V_{OUT}11$	Buffer output. Swings to positive rail.
47	$V_{OUT}12$	
48	NC	

TYPICAL PERFORMANCE CHARACTERISTICS

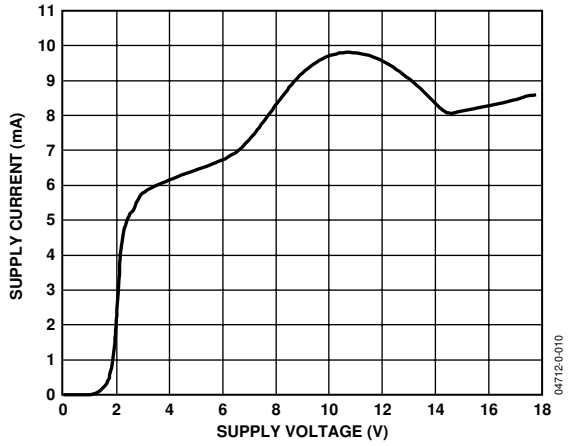

Figure 3. Supply Current vs. Supply Voltage

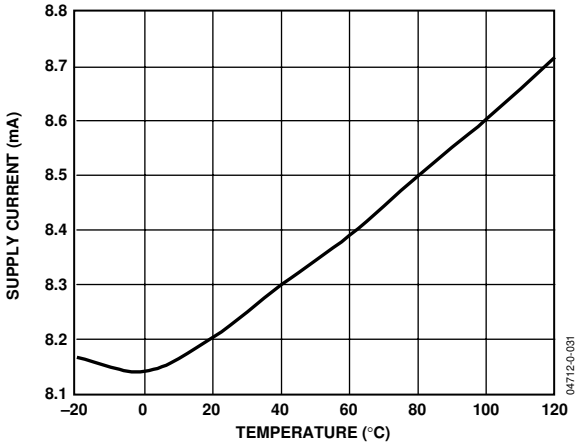

Figure 4. Supply Current vs. Temperature

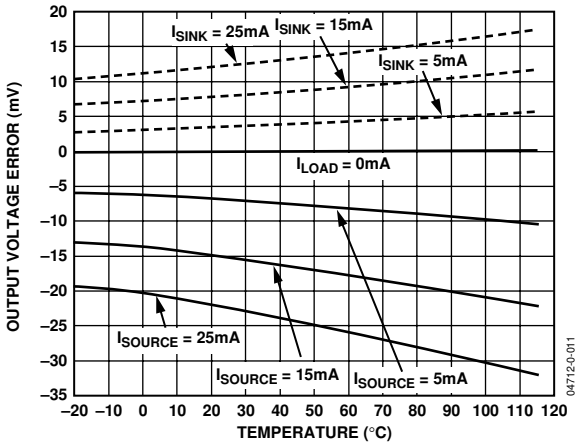

Figure 5. Output Voltage Error vs. Temperature

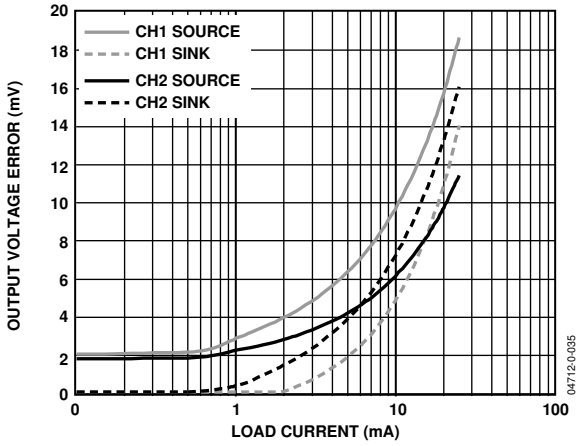

Figure 6. Output Voltage Error vs. Load Current

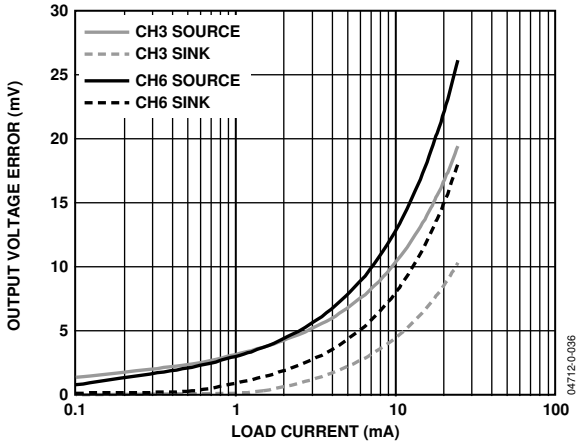

Figure 7. Output Voltage Error vs. Load Current

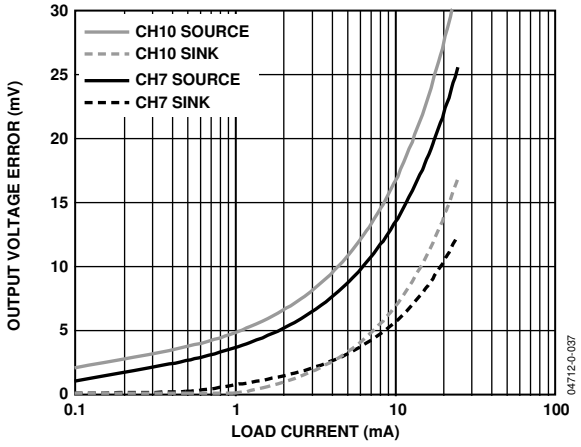

Figure 8. Output Voltage Error vs. Load Current

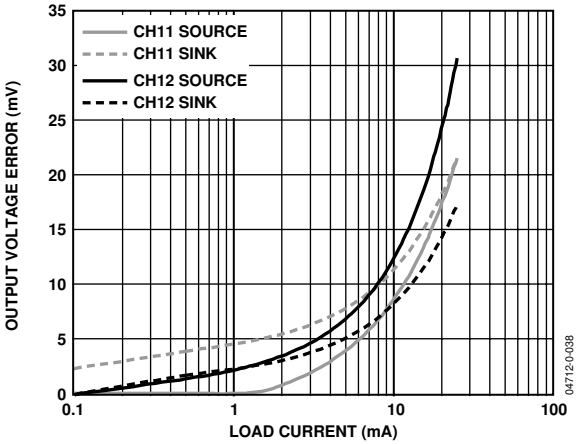

Figure 9. Output Voltage Error vs. Load Current

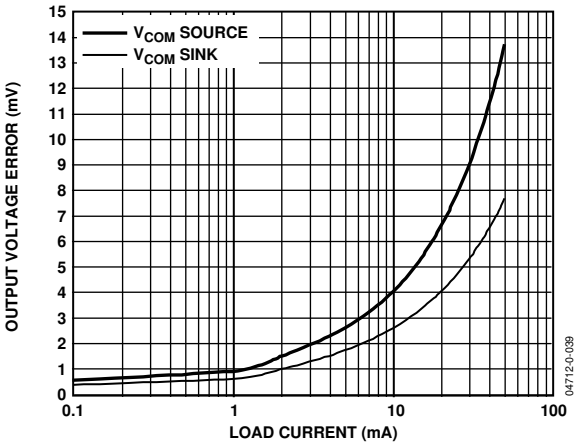

Figure 10. Output Voltage Error vs. Load Current

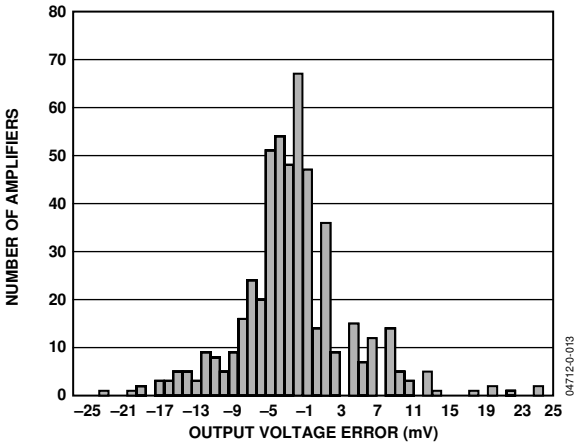

Figure 11. Output Voltage Error/Gamma 1 and 2

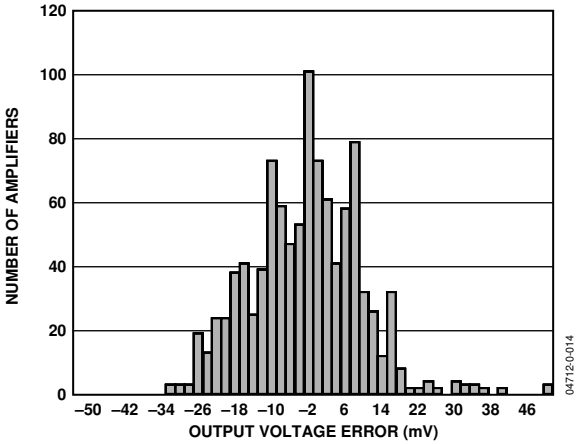

Figure 12. Output Voltage Error/Gamma 3 to 6

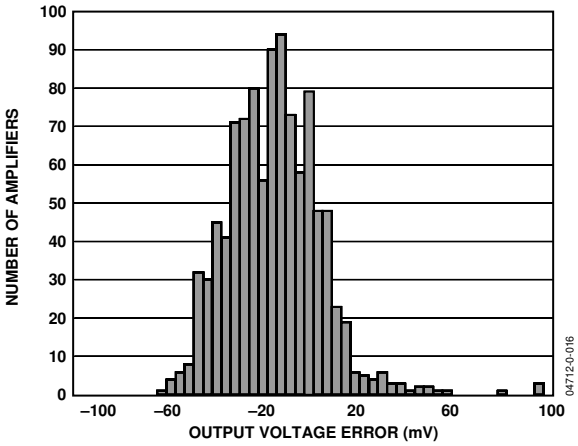

Figure 13. Output Voltage Error/Gamma 7 to 10

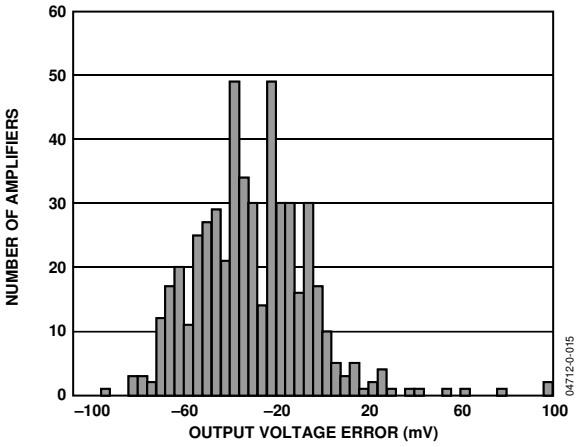

Figure 14. Output Voltage Error/Gamma 11 and 12

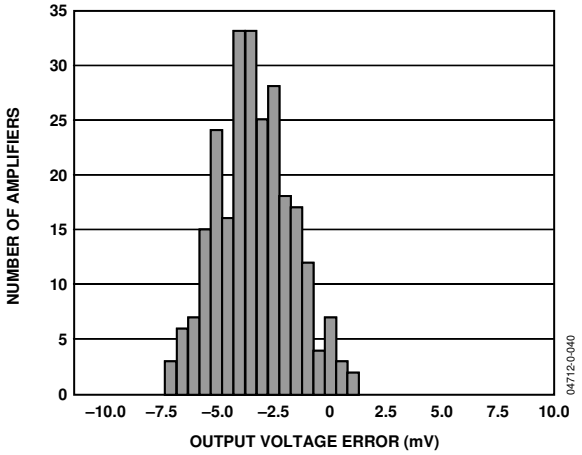

Figure 15. Output Voltage Error/Gamma V_{COM}

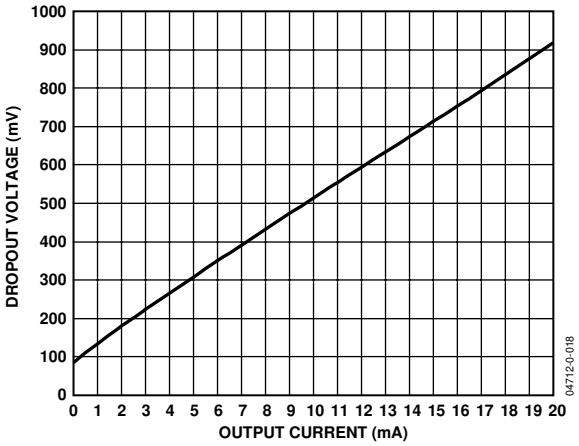

Figure 18. Dropout Voltage vs. Output Current

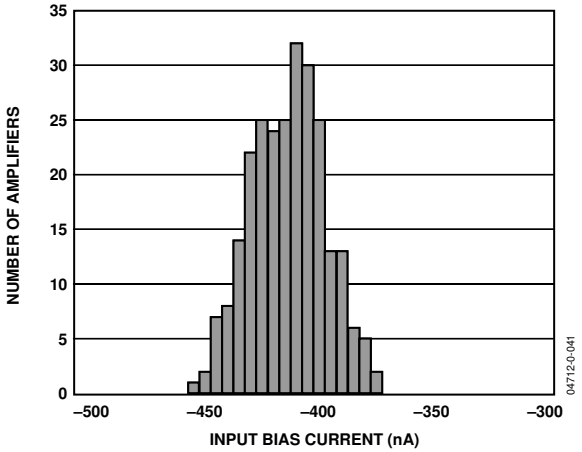

Figure 16. V_{COM} Input Bias Current Distribution

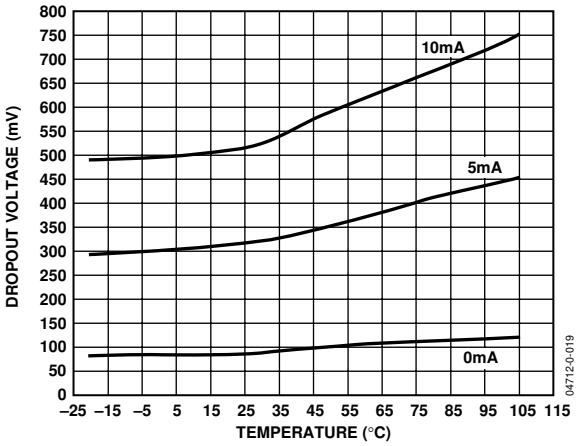

Figure 19. Dropout Voltage vs. Temperature

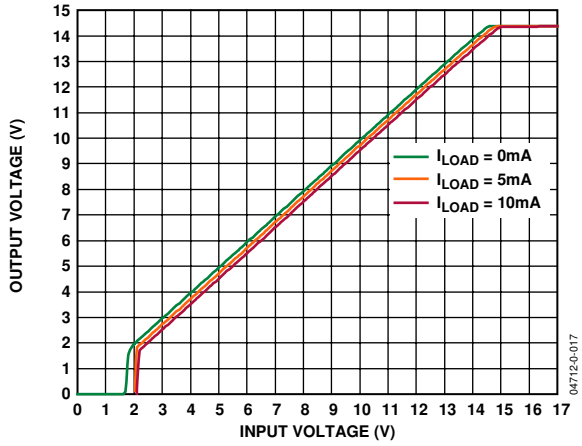

Figure 17. Dropout Characteristics

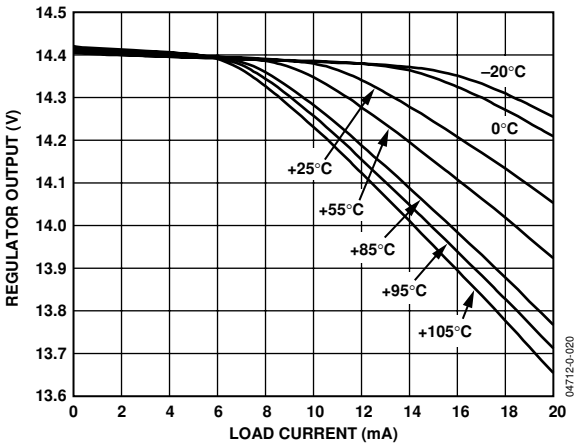

Figure 20. Regulator Output vs. I_{LOAD} over Temperature

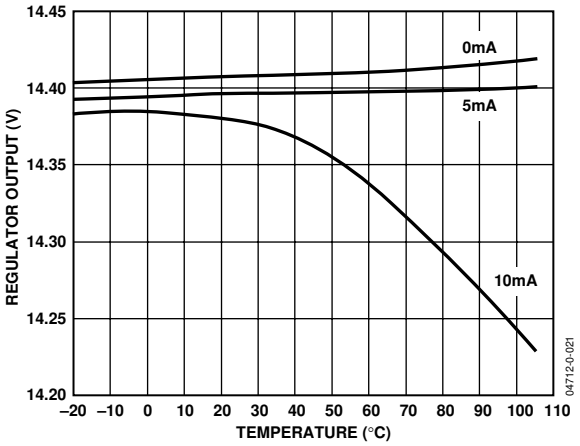

Figure 21. Regulator Output vs. Temperature

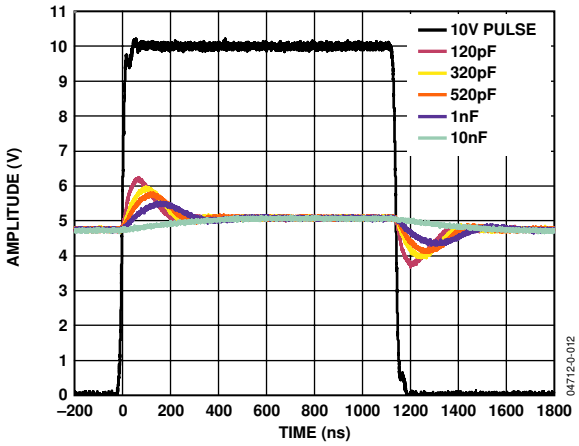

Figure 24. Transient Load Response vs. Capacitive Loading

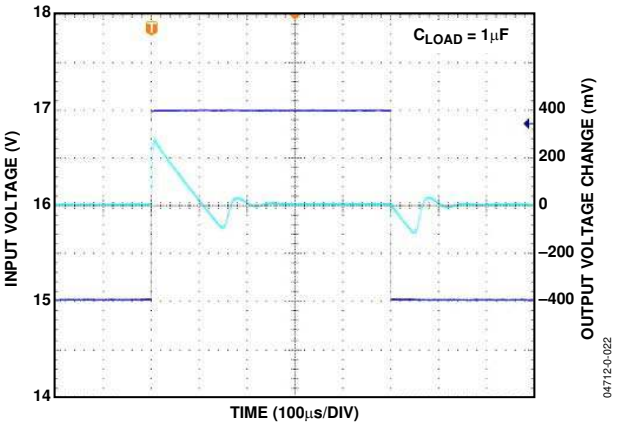

Figure 22. Regulator Line Transient Response

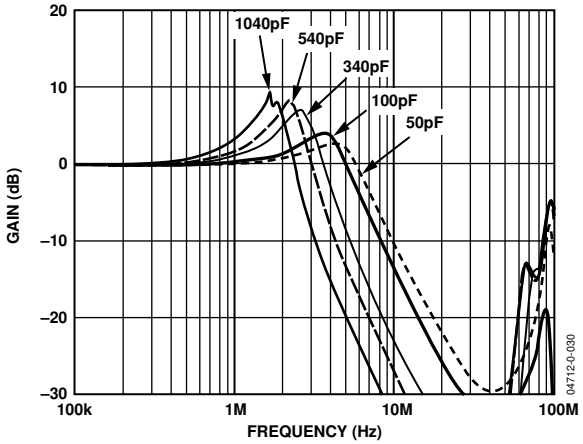

Figure 25. Frequency Response vs. Capacitive Loading

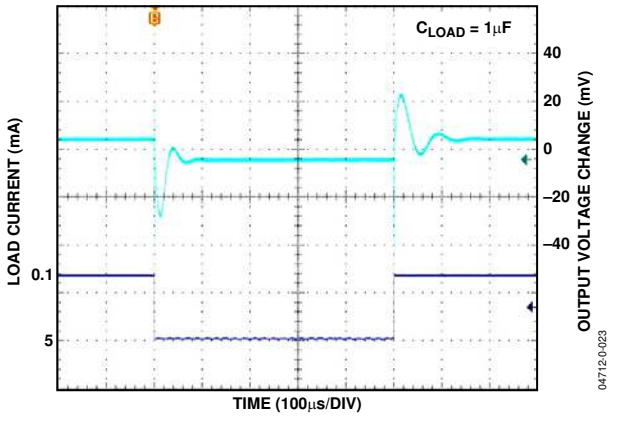

Figure 23. Regulator Load Transient Response

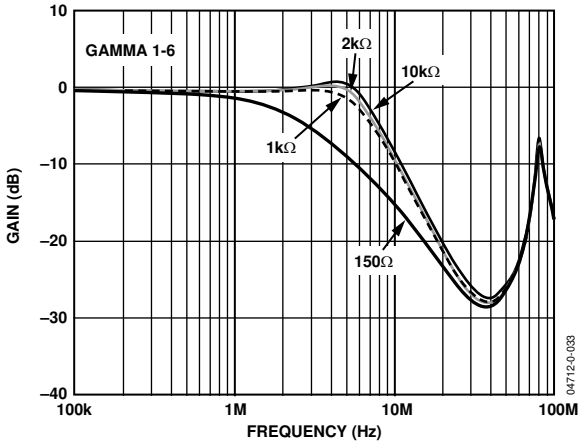

Figure 26. Frequency Response vs. Resistive Loading

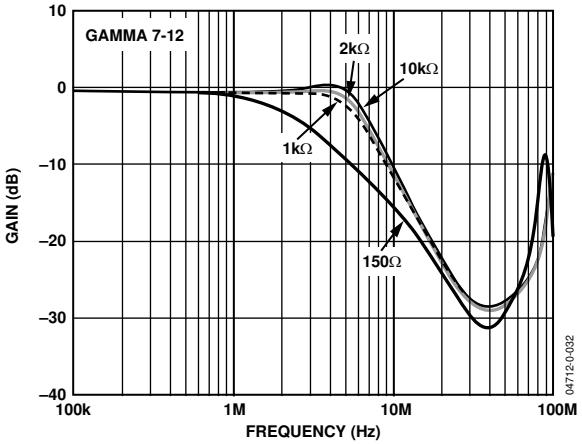

Figure 27. Frequency Response vs. Resistive Loading

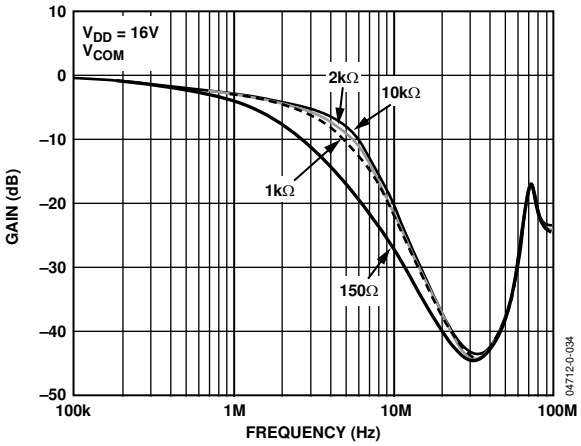

Figure 28. Frequency Response vs. Resistive Loading

APPLICATION NOTES

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the ADD8707 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADD8707. Exceeding a junction temperature of 175°C for an extended period can result in changes in the silicon devices, potentially causing failure.

LAND PATTERN

The LFCSP package comes with a thermal pad. Soldering down this thermal pad dramatically improves the heat dissipation of the package. It is necessary to attach vias that connect the soldered thermal pad to another layer on the board. This provides an avenue to dissipate the heat away from the part. Without vias, the heat is isolated directly under the part.

Subdivide the solder paste, or stencil layer, for the thermal pad. This reduces solder balling and splatter. It is not critical how the subdivisions are arranged, as long as the total coverage of the solder paste for the thermal pad is greater than 50%. The land pattern is critical to heat dissipation. A suggested land pattern is shown in Figure 29.

The thermal pad is attached to the substrate. In the ADD8707, the substrate is connected to V_{DD}. To be electrically safe, the thermal pad should be soldered to an area on the board that is electrically isolated or connected to V_{DD}. Attaching the thermal pad to ground adversely affects the performance of the part.

OPERATING TEMPERATURE RANGE

The maximum junction temperature is as follows:

$$T_J = T_{AMB\,MAX} + \theta_{JA} \times W_{MAX}$$

where:
$T_{AMB\,MAX}$ = maximum ambient temperature specified on the data sheet.
θ_{JA} = junction-to-ambient thermal resistance, in °C/watt.
W_{MAX} = maximum power dissipated in the device, in watts.

For the ADD8708, W_{MAX} can be calculated by this equation:

$$W_{MAX} = V_{DD} \times I_{SYS} + V_{OUT} \times I_{OUT} + V_{DO} \times I_O$$

where:
$V_{DD} \times I_{SYS}$ = nominal system power requirements
$V_{OUT} \times I_{OUT}$ = amplifier load power dissipation
$V_{DO} \times I_O$ = regulator load power dissipation

In a reasonable application, $T_{AMB\,MAX}$ = 95°C. To calculate W_{MAX}, assume:

$V_{DD} \times I_{SYS}$ = 15 V × 15 mA
$V_{OUT} \times I_{OUT}$ = (8 V × 5 mA/channel) × 13 channels
$V_{DO} \times I_O$ = 0.6 V × 5 mA
W_{MAX} = (15 V × 15 mA) + (8 V × 5 mA/channel × 13 channel) + (0.6 V × 5 mA) = 0.748 W

Example 1

DAP soldered down with via θ_{JA} = 28.3°C/W.

$$T_J = 95°C + (28.3°C/W) \times (0.748\ W) = 116°C$$

The maximum junction temperature that is guaranteed before the part breaks down is 150°C. is The maximum process limit is 125°C. Because T_J is < 150°C and < 125°C, this example demonstrates a condition where the part should perform within process limits.

Example 2

DAP not soldered down θ_{JA} = 47.7°C/W

$$T_J = 95°C + (47.7°C/W) \times (0.748\ W) = 131°C$$

In this example, T_J is < 150°C but > 125°C. Although the part should not exhibit any damage in this situation, the process limits have been exceeded. The part may no longer operate as intended.

Conclusion

These examples show that soldering down the DAP is important for proper heat dissipation. Under the same power-up and loading conditions, the unsoldered part has a 22.5% higher temperature than the soldered part. Therefore, it is strongly advised that the DAP be soldered down.

OUTPUT FILTERING

The amplifiers in the ADD8707 are extremely stable devices. Therefore it is not necessary to attach low-pass filters on the output to provide stability. In fact it is can be detrimental to gamma applications to have a series resistor on the output of the amplifiers.

In a typical application these amplifiers provide nearly 20 mA of current. Even a small output resistance in series with the source driver load produces voltage drops that adversely affect the overall system accuracy.

While not needed for stability, it is acceptable to place a low-pass filter to ground on the gamma outputs to remove any high frequency noise from the switch mode power supply. Make sure this filter is out of the signal path between the ADD8707 outputs to source driver inputs. See Figure 30.

The nature of the V_{COM} circuit demands high peak currents and fast switching. This makes a capacitor to ground on the V_{COM} output essential.

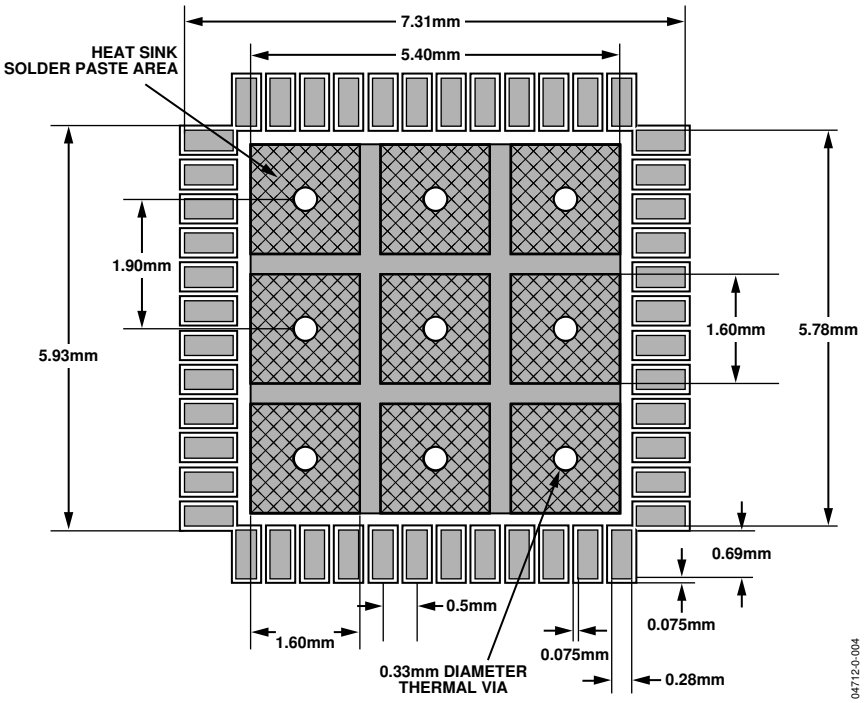

Figure 29. 48-Pin LFCSP (CP-48) Land Pattern—Dimensions shown in millimeters

Notes:

1. Gray area represents the board metallization.
2. White area represents the solder mask and vias.
3. Hatched area is for the heat sink solder paste.
4. The thermal pad is electrically active. The solder mask opening should be 0.150 mm larger than the pad size, resulting in 0.075 mm of clearance between the copper pad and solder mask.

TYPICAL APPLICATIONS CIRCUIT

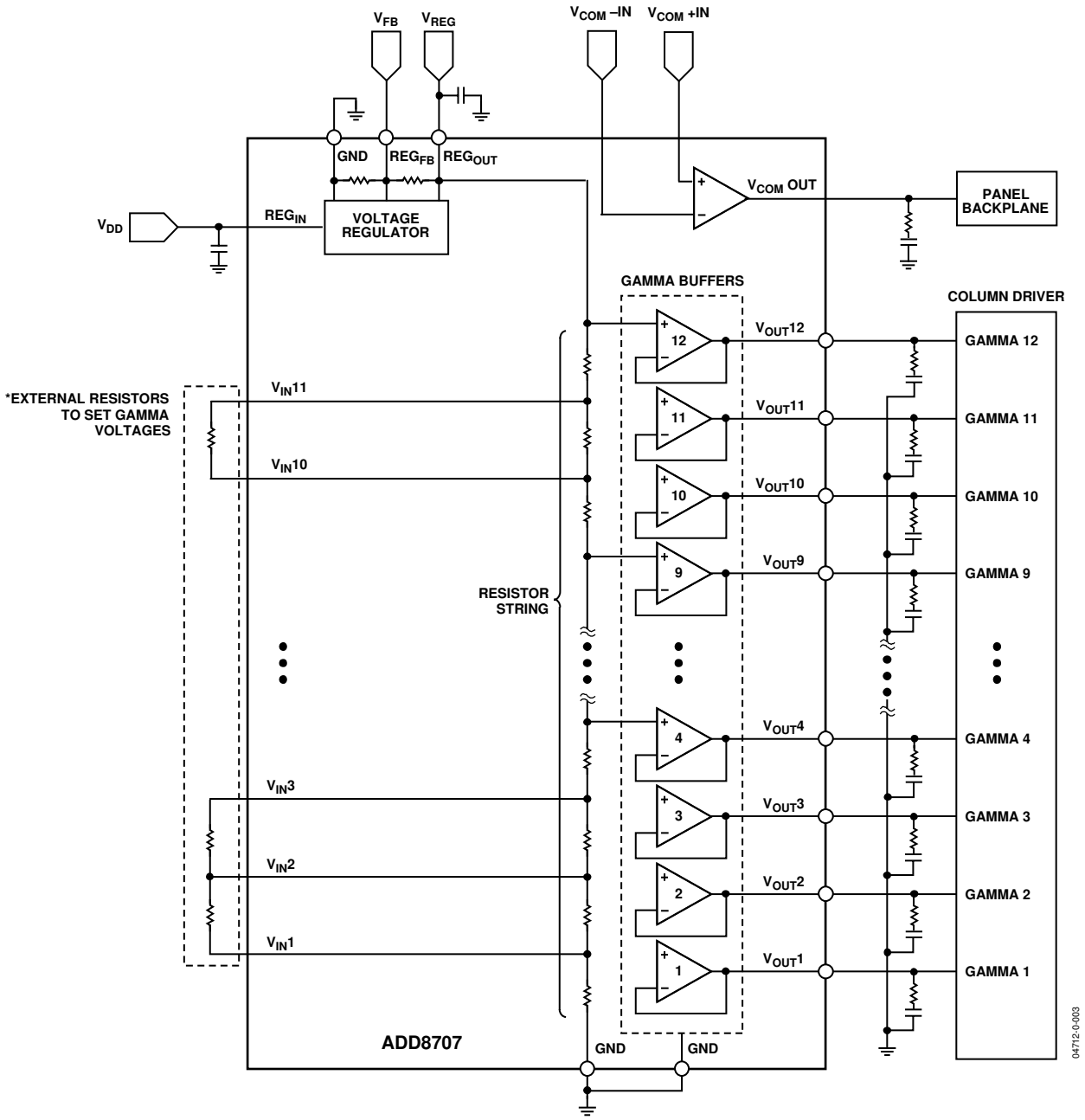

Figure 30. Typical Applications Circuit

OUTLINE DIMENSIONS

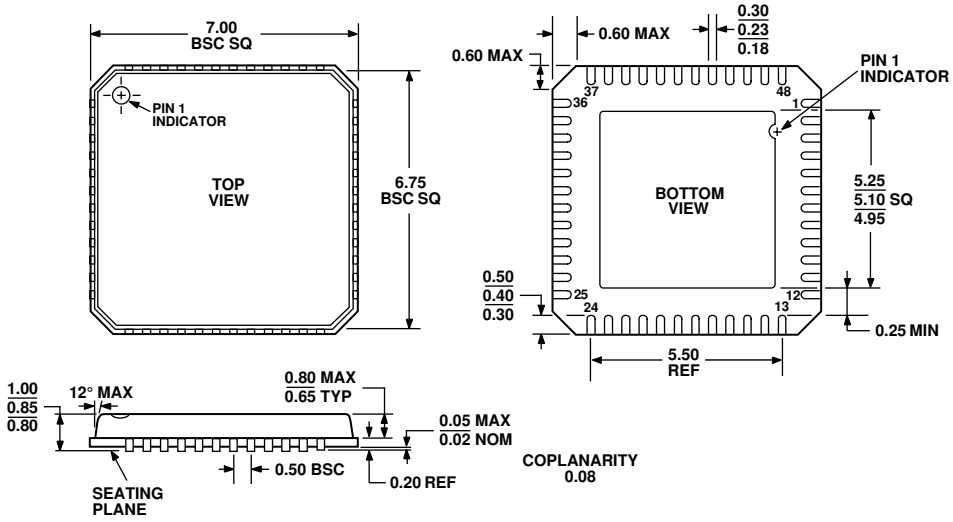

Figure 31. 48-Lead Frame Chip Scale Package [LFCSP]
(CP-48)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Package	Package Description	Package Outline
ADD8707ACPZ-REEL7[2]	–40°C to +100°C	48-Terminal Leadless Frame Chip Scale Package	CP-48

[1] Available in reels only.
[2] Z = Pb-free part.

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