ANALOG DEVICES

EVAL-ADuM4122EBZ User Guide
UG-1440

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Evaluating the ADuM4122 Single Gate Adjustable Slew Rate Isolated Gate Driver, 3 A Short Circuit (<3 Ω)

FEATURES

3 A short-circuit output capability
Output power device resistance: <3 Ω
Output voltage range to 35 V
Output and input undervoltage lockout (UVLO)
Pad placement for multiple switch types
Pad placement for external series gate resistors
Screw terminals for easy connectivity
Placement for capacitive load testing
Jumpers for easy slew rate setting

EVALUATION KIT CONTENTS

EVAL-ADuM4122EBZ evaluation board

EQUIPMENT NEEDED

Suggested test equipment
Primary side power supply: 0 V to 6 V at 100 mA
Secondary side supply: 0 V to 35 V at 250 mA
Square wave generator: 0 V to 5 V

DOCUMENTS NEEDED

ADuM4122 data sheet

GENERAL DESCRIPTION

The EVAL-ADuM4122EBZ evaluation board supports the ADuM4122 isolated gate driver with slew rate control. *i*Coupler® technology provides isolation between the ADuM4122 input signal and the output gate driver. The evaluation board supplies jumpers and screw terminals to configure different drive conditions. The EVAL-ADuM4122EBZ board operates with square waves and dc values on the V_{IN+} and $\overline{SRC}$ pins.

The ADuM4122 is operational with voltages of up to 35 V. Logic level voltages at the V_{IN+} pin control the V_{OUT} output. The $\overline{SRC}$ pin controls whether the V_{OUT_SRC} pin is either set to high-Z or follows the logic of the user supplied pulse-width modulation (PWM) input at V_{IN+}. When the external series gate resistors combine the outputs from the V_{OUT} and V_{OUT_SRC} pins, one isolated gate driver is then able to have two easily selectable slew rates.

The EVAL-ADuM4122EBZ board tests the propagation delay, drive strength, slew rate selection, and input logic of the device.

Refer to the ADuM4122 data sheet for complete information about the ADuM4122, and consult the data sheet in conjunction with this user guide when using the evaluation board.

EVALUATION BOARD PHOTOGRAPH

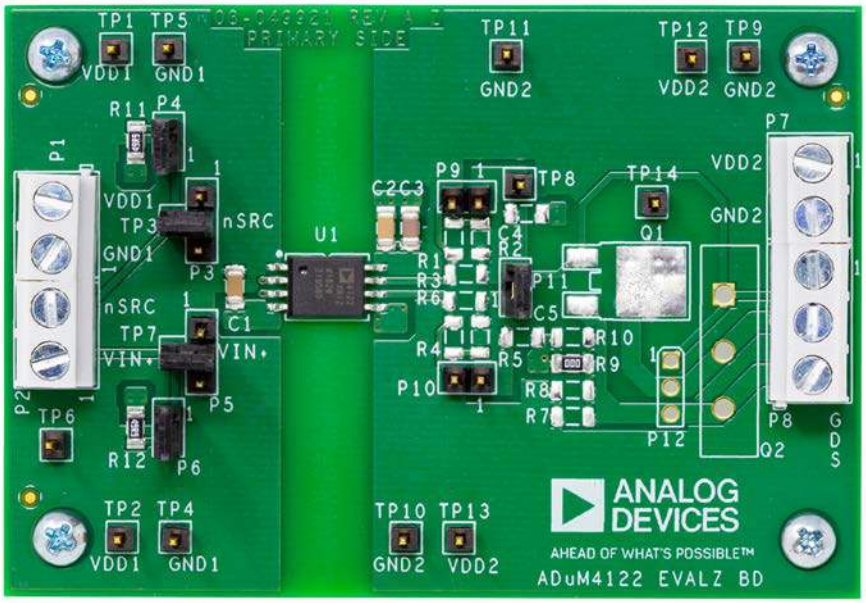

Figure 1.

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REVISION HISTORY

4/2019—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

INITIAL CONFIGURATION

In the stock configuration (see Figure 1), the R1 to R6 resistors are not placed on the board. The series external resistors for the charging and discharging paths of the driven device are located in the R1 to R6 pad locations-.

PAD LAYOUT FOR THE DEVICE UNDER TEST (DUT)

The EVAL-ADuM4122EBZ board provides placement for supporting components to facilitate evaluation of the gate driver. The Pad Layout for the Device Under Test (DUT) section provides descriptions of the available pad placements.

The EVAL-ADuM4122EBZ board includes the following available pad placements:

- U1 is the footprint for the ADuM4122.
- C1 and C2 are 0.1 µF bypass capacitors. C3 is a 10 µF bypass capacitor.
- TO-247, TO-252, or TO-220 metal-oxide semiconductor field effect transistors (MOSFETs) or insulated gate bipolar transistors (IGBTs) (see Figure 2 for the transistor footprint) populate the Q1, Q2, and P12 pad placements. TO-252 is placed on Q1, TO-247 is placed on Q2, and TO-220 is placed on P12.
- R1 to R6 are gate resistors that control the output edges. No resistors are installed by default and users are recommended to populate the resistors with low value 1206 resistors in the 1 Ω to 10 Ω range.

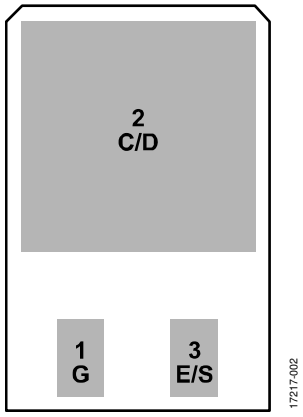

Figure 2. IGBT/MOSFET Footprint

SETTING UP THE EVAL-ADUM4122EBZ EVALUATION BOARD

Complete the following steps before initial use to prepare the evaluation board for operation:

1. Depending on the load being driven, use the 1206 surface-mount resistors pads to select the appropriate drive strength. The recommended values are approximately between 1 Ω and 10 Ω.
2. The R1 to R3 resistors are between the P11 jumper pins and the V_{OUT} pin. R4 to R6 are between P11 and the V_{OUT_SRC} pin. Place a jumper in P11 to combine the two outputs pins, V_{OUT} and V_{OUT_SRC}, at the gate of the user supplied power device. If the jumper at P11 is removed, the C4 and C5 capacitor pad placements provide land patterns for placing a capacitor load to simulate gate capacitance.
3. The R7 to R10 resistors enable bipolar voltage configurations. Populate R9 and/or R10 with a 0 Ω resistor when the source or emitter of the driven power device is referenced to GND2, a unipolar configuration. If a bipolar voltage configuration is desired, construct Zener networks in R7 to R10 according to the directions from the Analog Dialogue article, Driving a Unipolar Gate Driver in a Bipolar Way.
4. Either place an IGBT or MOSFET in the provided Q1, Q2, or P12 landing patterns to evaluate gate driver performance on the given power device. P9 and P10 allow shorting across the external resistors of the series to observe overshoot and to probe the voltage to quantify peak currents.
5. The R11 and R12 resistors terminate the inputs, V_{IN+} and $\overline{SRC}$ with 50 Ω loads. The P4 jumper pin and the P6 jumper pin connect R11 and R12, but when R11 and R12 are not connected, the evaluation board accepts high impedance, input generator signals from an external source (see Figure 3).

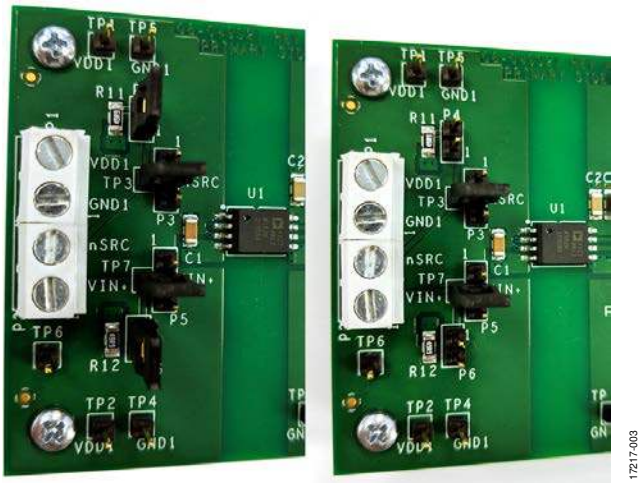

Figure 3. 50 Ω Terminated (Left) and High Impedance (Right)

6. Either pins or screw terminals are viable as connection mechanisms. The screw terminals connect wires for long-term measurements, but are not recommended for connecting driven devices.

7. P3 and P5 tie the V_{IN+} and $\overline{SRC}$ pins to V_{DD1} or GND1 for faster dc evaluation setups (see Figure 4, Figure 5, and Figure 6). If using P3 or P5, do not drive the pin that is connected by a jumper to an external signal generator.

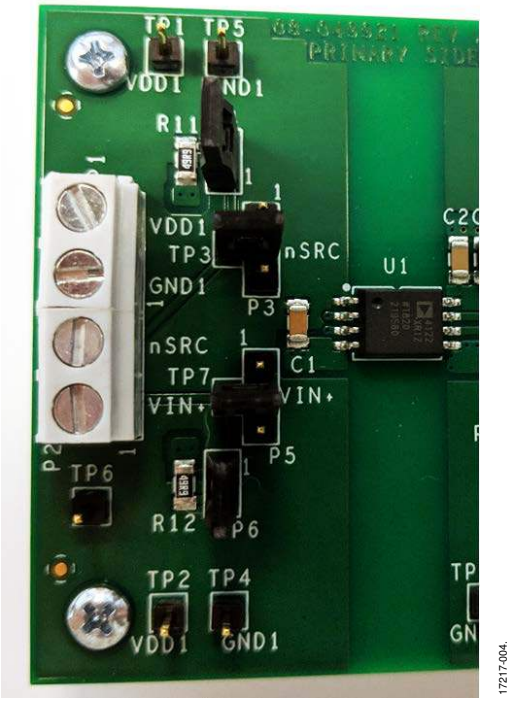

Figure 4. P3 and P5 Configured for Screw Terminal Input

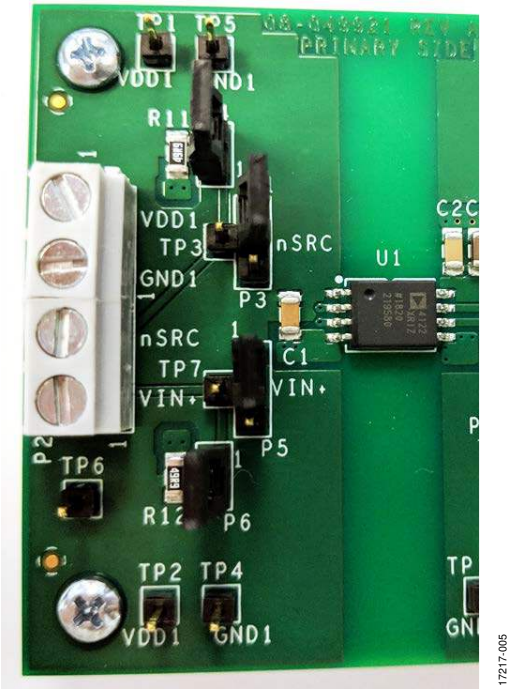

Figure 5. P3 and P5 Configured to Connect Inputs to V_{DD1}

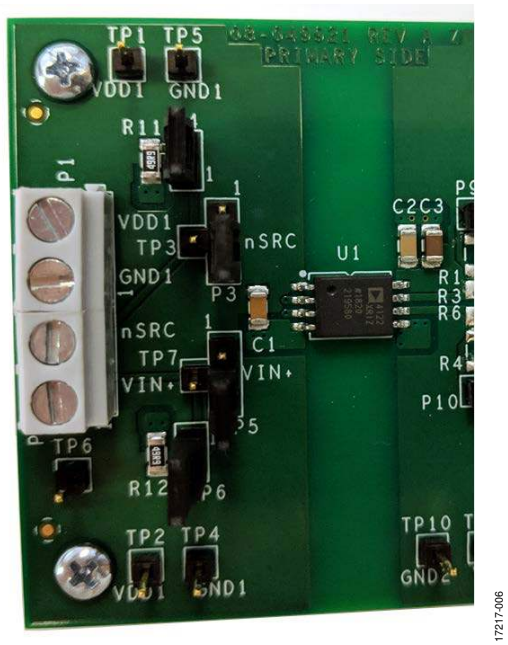

Figure 6. P3 and P5 Configured to Connect Inputs to GND1

POWER SUPPLIES

Adhere to the following steps to connect the EVAL-ADuM4122EBZ board to a power supply:

1. Connect the input V_{DD1} supply (3.3 V to 5.5 V) to the V_{DD1} and GND1 pins (see Figure 7).
2. Connect the input V_{DD2} supply (4.5 V to 35 V) to the V_{DD2} and GND2 pins (see Figure 7).

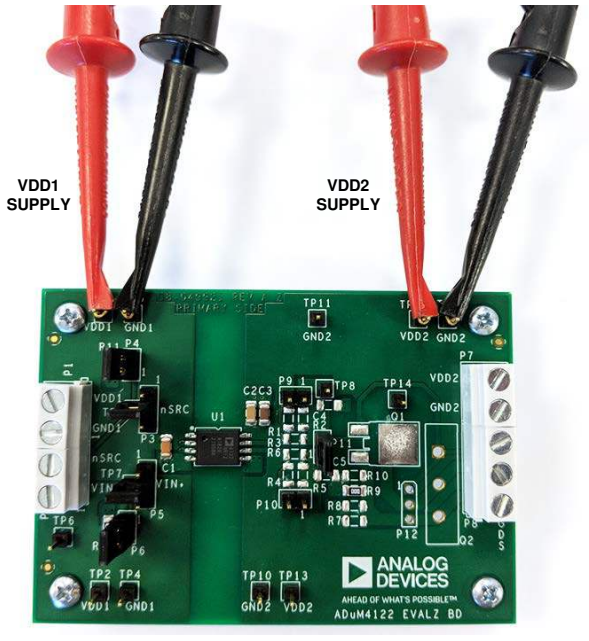

Figure 7. Power Supply Connections

GND1 and GND2 are isolated from each other. The emitter or source of the IGBT and MOSFET is connected to GND2.

INPUT AND OUTPUT CONNECTIONS

The V_{IN+} and $\overline{SRC}$ pins are complementary metal-oxide semiconductor (CMOS) inputs. The $\overline{SRC}$ pin chooses whether the extra drive power provided by the V_{OUT_SRC} pin is available at the output. $\overline{SRC}$ is active low, and an extra boost on the output is available when $\overline{SRC}$ is held low.

The EVAL-ADuM4122EBZ board comes with screw terminals for both the input and output connections. The screw terminals facilitate connection options (soldering vs. hook clamps) but are not recommended for high performance transient testing. The most accurate measurements conducted on the load, whether through the IGBT, MOSFET, or load capacitor, come from small loop measurements performed on the load. When conducting measurements on the load, whether through the IGBT, MOSFET, or load capacitor, small loop measurements are recommended for the best results. Using the screw terminals as either the sensing node or load connection often results in measurement overshoot.

EVALUATION BOARD SCHEMATIC AND ARTWORK

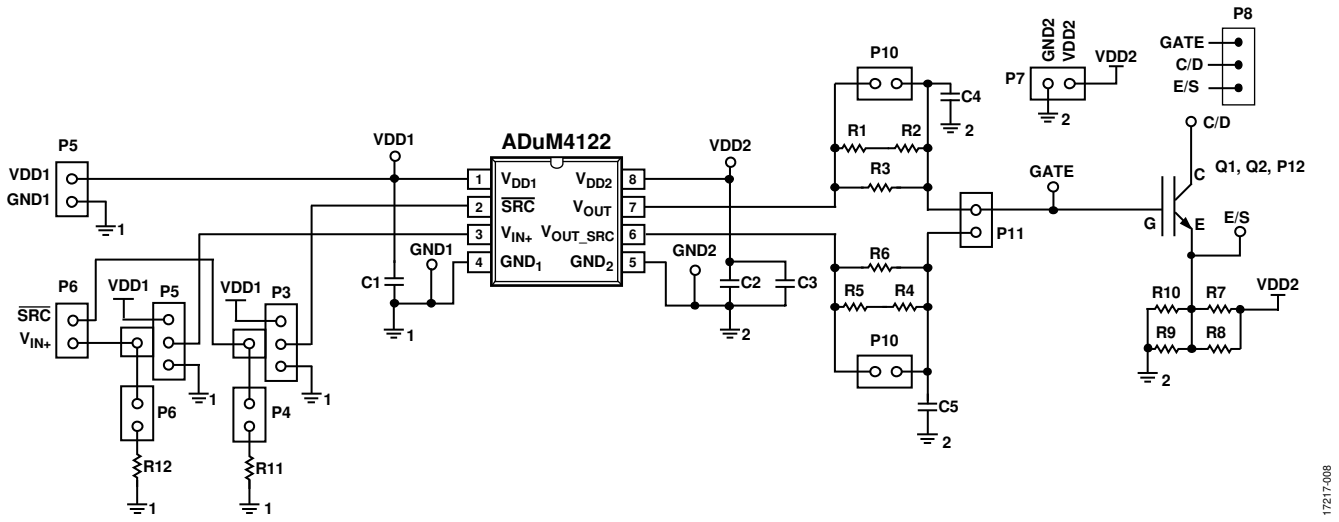

Figure 8. Schematic of the EVAL-ADuM4122EBZ Evaluation Board

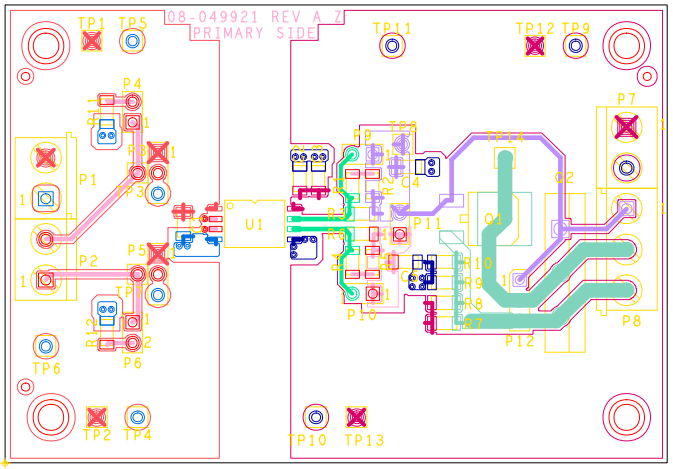

Figure 9. EVAL-ADuM4122EBZ Evaluation Board Top Layer

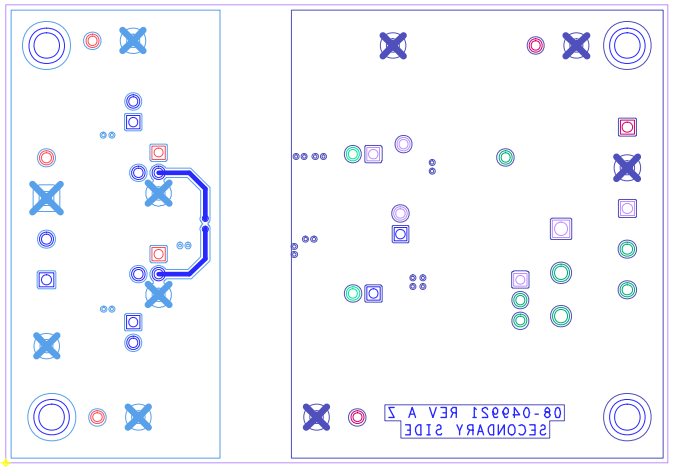

Figure 10. EVAL-ADuM4122EBZ Evaluation Board Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 1.

Reference Designator	Description/Value	Manufacturer	Part Number
U1	ADuM4122	Analog Devices, Inc.	ADuM4122ARIZ
R9	Resistor, 0 Ω, 1206	Not applicable	Not applicable
R11, R12	Resistor, 49.9 Ω, 1206	Not applicable	Not applicable
C1, C2	Capacitor, 0.1 µF, 25 V, 10%, 1206	Not applicable	Not applicable
C3	Capacitor, 10 µF, 50 V, 10%, 1206	Not applicable	Not applicable
R1 to R8, R10, Q1, Q2, P12, C4, C5	Not installed	Not applicable	Not applicable

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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