TPD5E003 Five-Channel Space-Saving ESD Protection Device

1 Features

- Provides System-Level ESD Protection for Low-Voltage I/O Interface
- IEC 61000-4-2 Level 4
  - ±15 kV (Contact Discharge)
  - ±15 kV (Air-Gap Discharge)
- Typical I/O Capacitance 7 pF (V_{IO} = 2.5 V)
- DC Breakdown Voltage: 6 V (Minimum)
- Low Leakage Current: 100 nA (Maximum)
- Low ESD Clamping Voltage
- Industrial Temperature Range: –40°C to 125°C
- IEC 61000-4-5 (Surge): 40 W (8/20-µs Pulse)
- Small, Easy-to-Route DPF Package

2 Applications

- End Equipment:
  - Cell Phones
  - Tablets
  - Remote Controllers
  - Wearables
- Interfaces:
  - SIM Cards
  - Audio Lines
  - Push-Buttons
  - General-Purpose Input and Output (GPIO)

3 Description

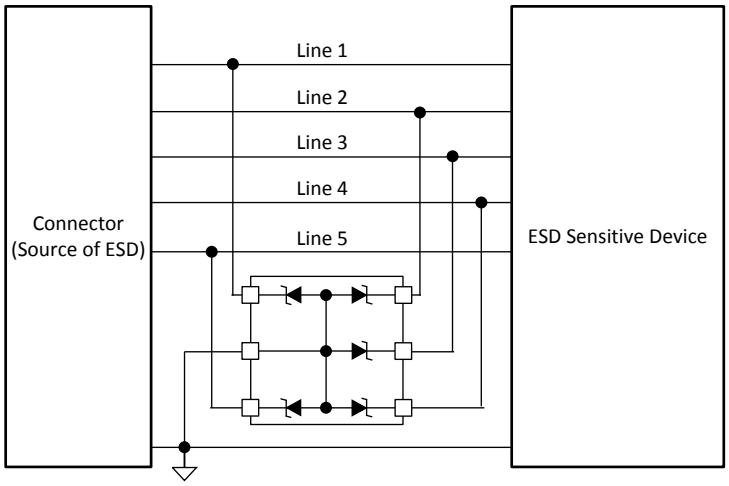
The TPD5E003 is a five-channel electrostatic discharge (ESD) transient voltage suppression (TVS) device. This device offers ±15-kV IEC contact and ±15-kV air-gap (level 4) ESD protection, and features five identical ESD clamping diodes that can be used to protect either five unidirectional (0 V to 5 V) I/O lines or four bidirectional (–5 V to 5 V) I/O lines. The compact DPF package is an industry standard and is convenient for component placement in space-constrained applications. Typical application interfaces include SIM card interfaces, audio lines (mics, earphones, and speakerphones), SD interfaces, and keypads, or other buttons. Typical end equipment includes cell phones, tablets, remote controllers, and wearables.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD5E003	X2SON (6)	1.00 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2013) to Revision B — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Original (December 2012) to Revision A — **Page**

- Added IO voltage tolerance to the ABSOLUTE MAXIMUM RATINGS table. ... 3
- Added MAX values to parameters in the ELECTRICAL CHARACTERISTICS table ... 4

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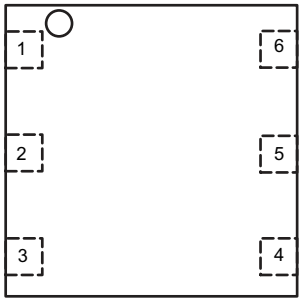
5 Pin Configuration and Functions

DPF Package
6-Pin X2SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
I/O	1	I/O	ESD Protected channel
	3		
	4		
	5		
	6		
GND	2	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

	MIN	MAX	UNIT
I/O voltage tolerance		5.5	V
Peak pulse current (tp = 8/20 µs), I_{PP}		3	A
Peak pulse power (tp = 8/20 µs), P_{PP}		40	W
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings: JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings: IEC 61000-4-2

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±15000	V
		IEC 61000-4-2 air-gap discharge	±15000	

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6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Operating free-air temperature, T_A		–40		125	°C
Operating voltage	Pin 1, 3, 4, 5, 6 to Pin 2	0		5	V

6.5 Thermal Information

THERMAL METRIC[1]		TPD5E003 DPF (X2SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	246.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	187.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	198	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	32	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_I = 0.1 µA			5	V
I_{LEAK}	Leakage Current	Pin 1, 3, 4, 5, or 6 = 5 V, Pin 2 = 0 V		10	100	nA
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 6 A, TLP, Dx pin to GND, T_A = 25 °C		13	15.6	V
		I_{PP} = 10 A, TLP, Dx pin to GND, T_A = 25 °C		16.3	19.5	V
R_{DYN}	Dynamic resistance	I_{TLP} = 6 A to 10 A, Dx pin to GND, T_A = 25 °C		0.8	1	Ω
		I_{TLP} = 6 A to 10 A, GND to Dx pin, T_A = 25 °C		0.3	0.4	Ω
C_{IO}	IO capacitance	V_{IO} = 2.5 V, 1 MHz, T_A = 25 °C	5.6	7	8.4	pF
		V_{IO} = 0 V, 1 MHz, T_A = 25 °C	8	10	12	pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA	6	7	8.5	V

6.7 Typical Characteristics

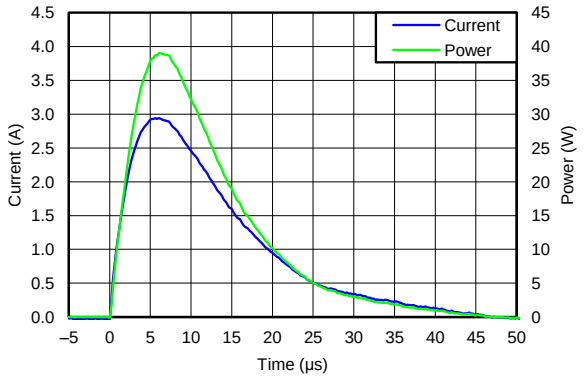

Figure 1. Surge Plot (tp = 8/20 µs), Pin Dx to GND

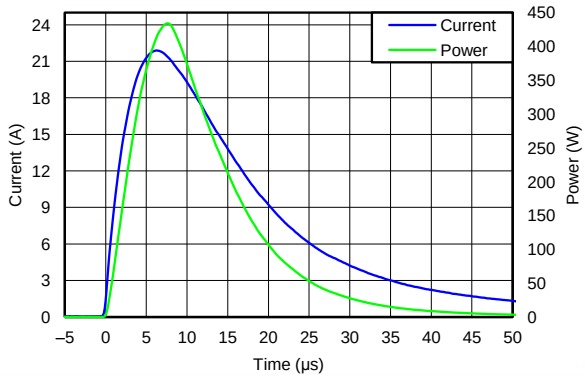

Figure 2. Surge Plot (tp = 8/20 µs), Pin GND to Dx

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Typical Characteristics (continued)

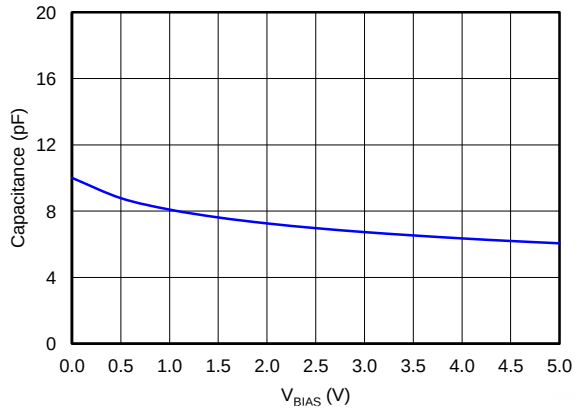

Figure 3. Capacitance vs DC Bias Voltage

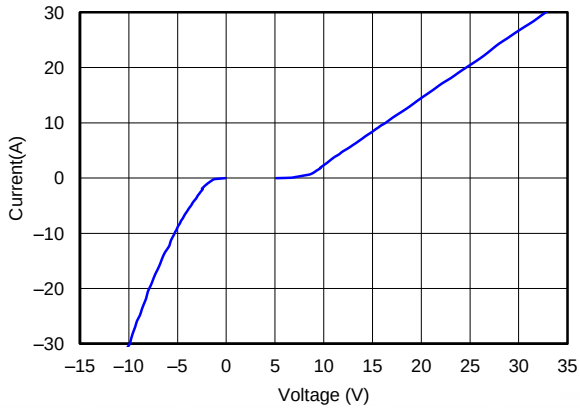

Figure 4. 30 A TLP Plot

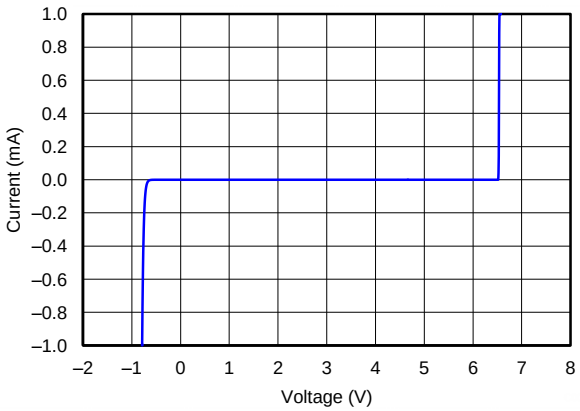

Figure 5. DC SWEEP V-I Curve

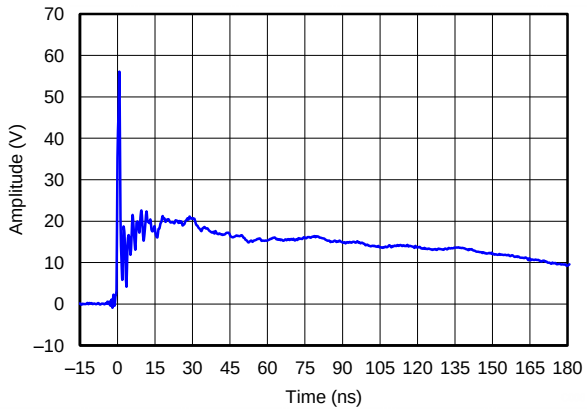

Figure 6. IEC 61000-4-2 Clamping Voltage, 8-kV Contact

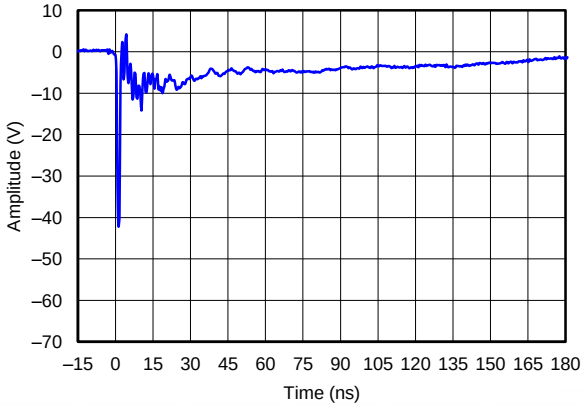

Figure 7. IEC 61000-4-2 Clamping Voltage, –8-kV Contact

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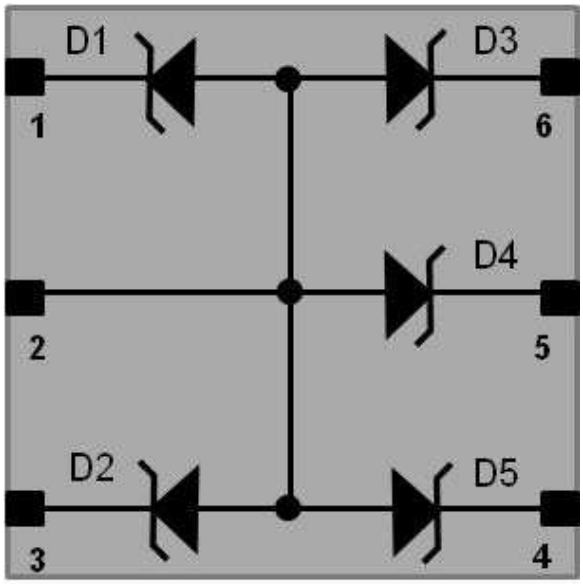
7 Detailed Description

7.1 Overview

The TPD5E003 is a five-channel ESD protection device. Each channel has ±15 kV contact and ±15 kV air-gap IEC ESD performance. When TPD5E003 is used in the unidirectional clamping configuration, it stays inactive from 0 V to 5 V and has low leakage. When the voltages on the I/O lines exceed the breakdown voltage, it starts to clamp and thus, keep the I/O line voltages low. Same mechanism applies to the bidirectional configuration where one of the channels is used as the ground pin and the other four are connected to I/O. The low leakage inactive range in bidirectional configuration is from –5 V to 5 V. The compact DPF package helps save board area. Typical application interfaces include SIM card interfaces, audio lines (mics, earphones, and speakerphones), SD interfaces, and keypads, or other buttons. Typical end equipment includes cell phones, tablets, remote controllers, and wearables.

7.2 Functional Block Diagram



7.3 Feature Description

TPD5E003 is a robust ESD protection device. Each of the five channels has ±15 kV contact and ±15 kV air-gap IEC ESD performance. This and the low dynamic resistance ensure the circuits protected by it only see a low residual transient pulse during the ESD. A typical I/O capacitance of 7 pF makes sure that this device is suitable to be used in a wide frequency range of the applications. The capacitance is even smaller when used in the bidirectional configuration, thus can be used for even higher frequencies. Low leakage current can keep the unnecessary power dissipation low during the normal operation. The industrial temperature range of –40°C to 125°C makes this device suitable for a wide applications range including consumer electronics, industrial and automotive. With the robust design, TPD5E003 is able to take 3 A of 8/20 µs surge current (40 W). The small package saves the board area and the pinout makes it easy to route.

7.4 Device Functional Modes

Each channel of TPD5E003 is a passive clamp that has low leakage during normal operation when the voltage between I/O pin and GND is below V_{RWM} and activates when it goes above V_{BR}. During IEC ESD events (contact and air-gap), transient voltages as high as ±15 kV can be clamped. When the voltages on the protected lines fall below the trigger voltage, the device reverts back to the low leakage passive state.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When a system contains a human interface, it becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these interfaces. The TPD5E003 is a five-channel unidirectional TVS device, which is typically used to provide paths to ground for dissipating ESD events on signal or power lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

The TPD5E003 offers five identical unidirectional ESD protection channels. The device can also be used as four identical bidirectional ESD protection channels. To do so, pin 5 would be connected to ground, with pin 1, 3, 4, and 6 connected to the I/O to be protected. In the bidirectional configuration, I/O capacitance is reduced by half and dynamic resistance increases.

For this design example, the TPD5E003 will be used to protect the SIM card in the bidirectional configuration.

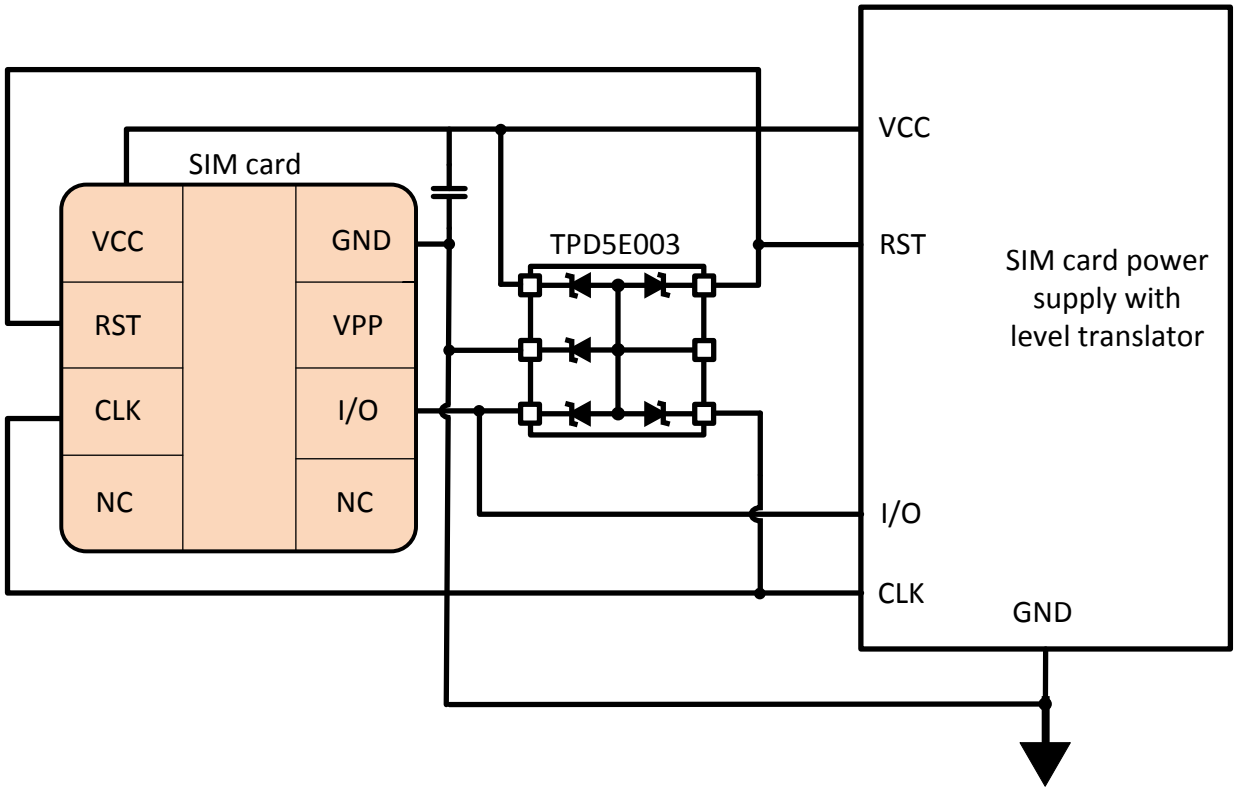

Figure 8. Application Diagram

Typical Application (continued)

8.2.1 Design Requirements

For this application, the system parameters in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
SIM card power supply voltage (Vcc)	3.3 V or 5 V
Signal pins voltage range	0 V to Vcc
Signal pins data rate	1 Mbps to 20 Mbps
Required IEC 61000-4-2 ESD Protection	±8-kV Contact or ±15-kV Air-Gap

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer should make sure:

- Voltage range on the protected line must not exceed the reverse standoff voltage of the TVS diode(s) (V_{RWM}).
- Operating frequency is supported by the I/O capacitance C_{IO} of the TVS diode.
- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, the power supply and signal voltage range is 0 to 3.3 V or to 5 V. When used in bidirectional configuration, at ±5 V the channel has very low leakage current; therefore, the bidirectional TVS will not break down during normal operation, and therefore normal operation of the power supply and signal pins will not be affected.

Next, consider the data rate of the signal. The SIM card clock frequency that the signals run off is from 1 MHz to 20 MHz; ensure that the TVS I/O capacitance will not distort this signal by filtering it with the inherent capacitance. Either a unidirectional or bidirectional ESD clamping device is good for this application, but bidirectional configuration has a smaller capacitance and thus each channel has sufficient bandwidth to pass the signal without distorting it, thus this configuration is used here.

Finally, the human interface in this application requires the Level 4 IEC 61000-4-2 system-level ESD protection (±8-kV Contact or ±15-kV Air-Gap). The TPD5E003 can survive at least ±15-kV Contact or ±15-kV Air-Gap. Therefore, the device can provide sufficient ESD protection for the interface. For any TVS diode to provide its full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, it is crucial that a system designer uses proper board layout of their TVS ESD protection diodes. See *Layout Example* for instructions on properly laying out TPD5E003.

8.2.3 Application Curves

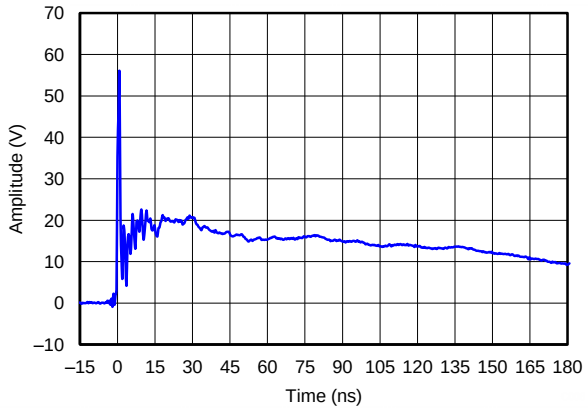

Figure 9. IEC 61000-4-2 Clamping Voltage, 8-kV Contact

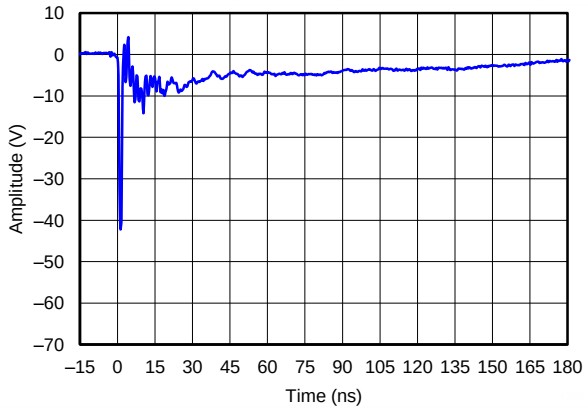

Figure 10. IEC 61000-4-2 Clamping Voltage, –8-kV Contact

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9 Power Supply Recommendations

This device is a passive TVS diode-based ESD protection device, so there is no need to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the interface as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the interface.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Use a thick and short trace for the power supply and ground paths.

10.2 Layout Example

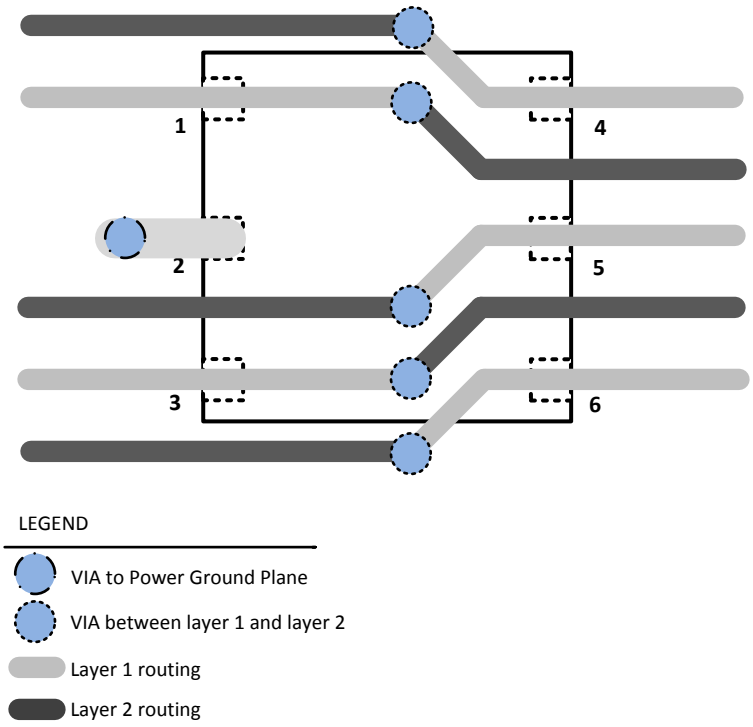

Figure 11. Board Layout Recommendation

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11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD5E003DPFR	ACTIVE	X2SON	DPF	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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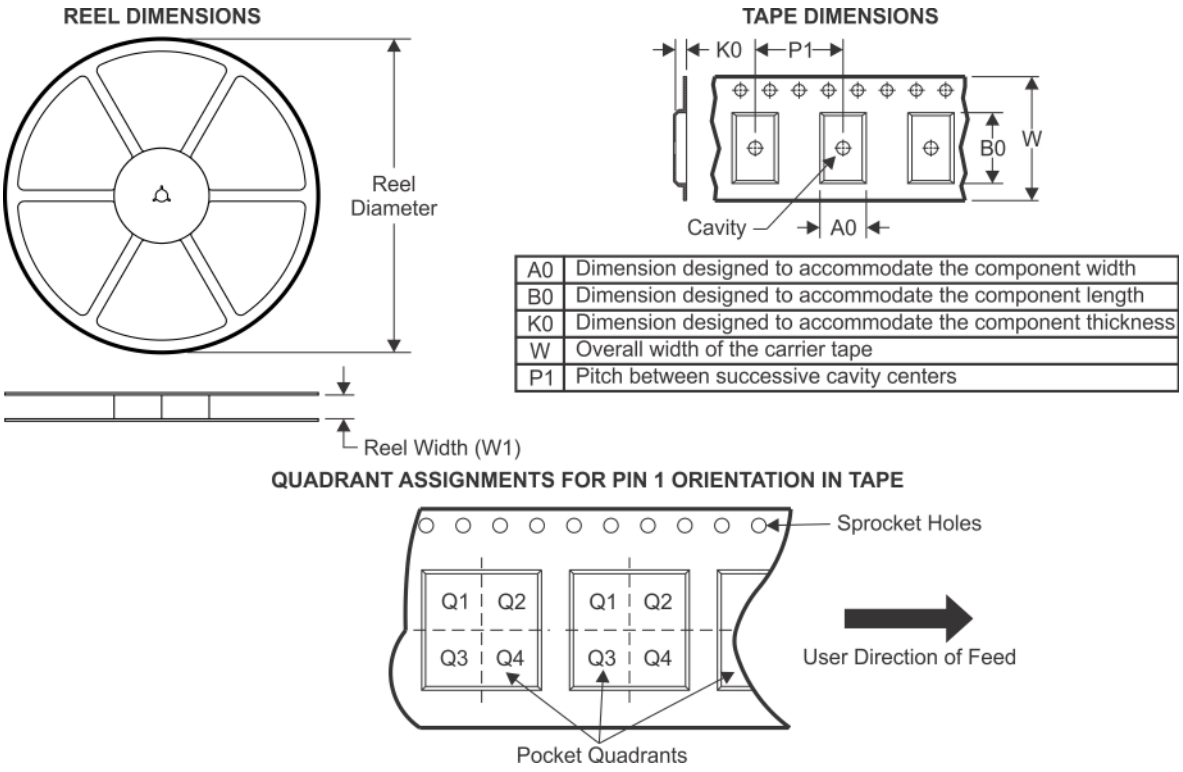
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

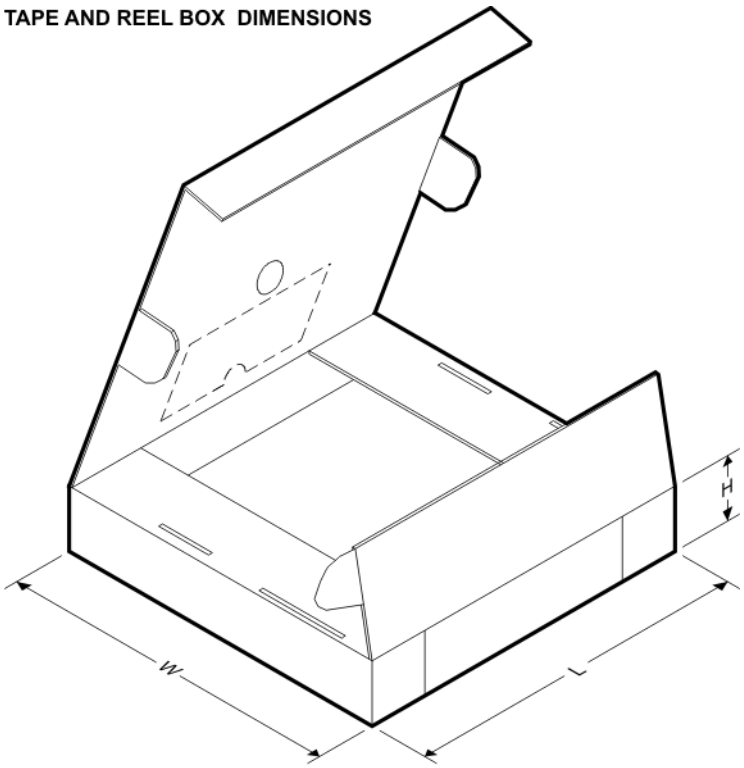


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

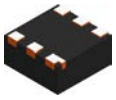
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD5E003DPFR	X2SON	DPF	6	5000	180.0	9.5	1.16	1.16	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD5E003DPFR	X2SON	DPF	6	5000	184.0	184.0	19.0

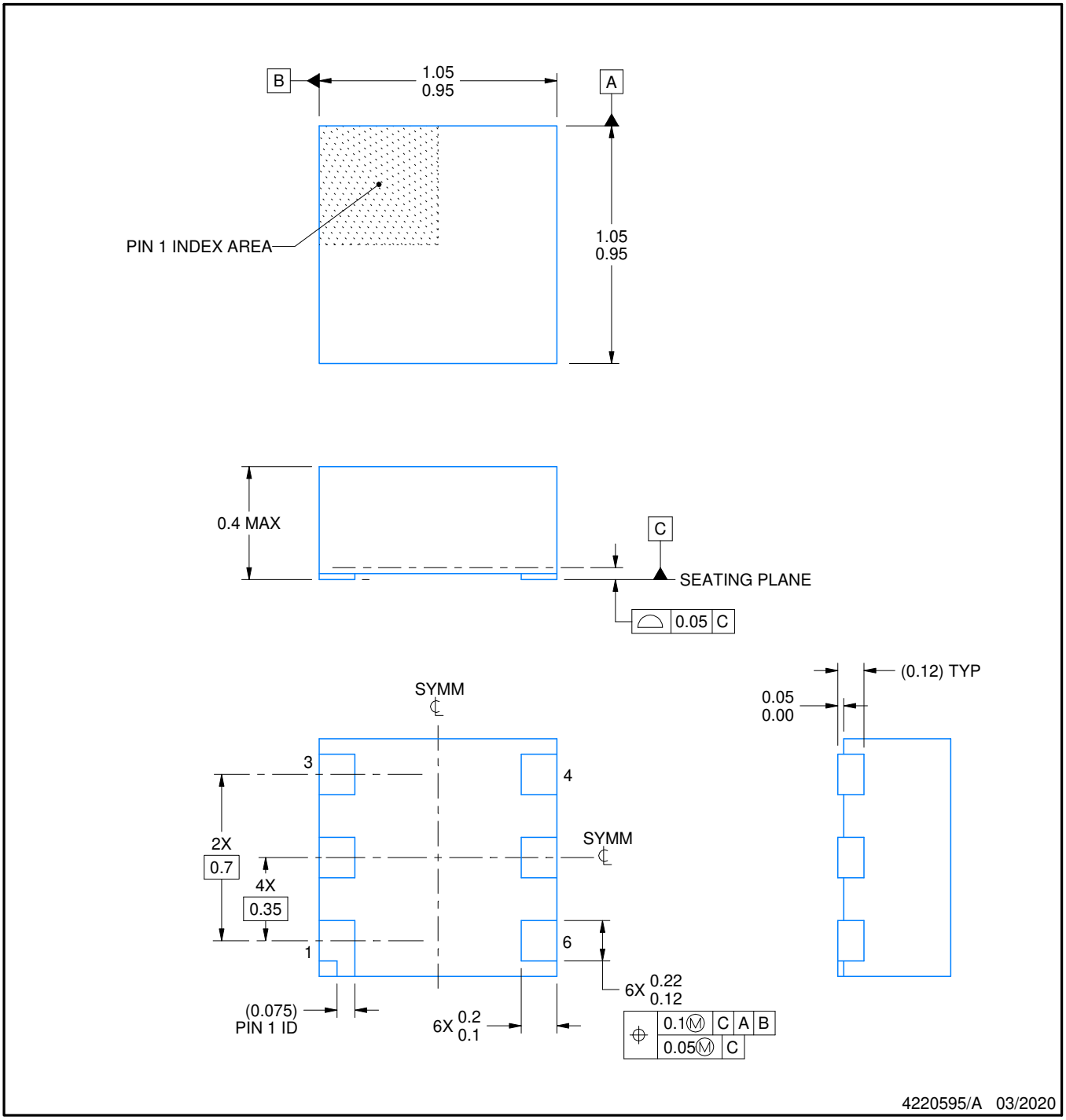


PACKAGE OUTLINE

DPF0006A

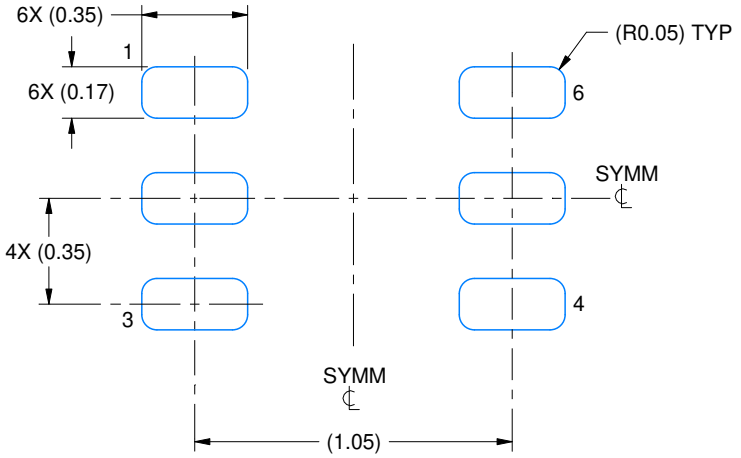
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

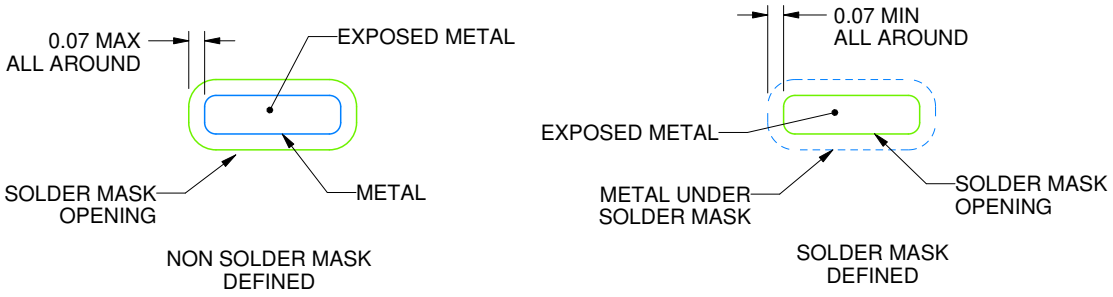


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X



SOLDER MASK DETAILS

4220595/A 03/2020

NOTES: (continued)

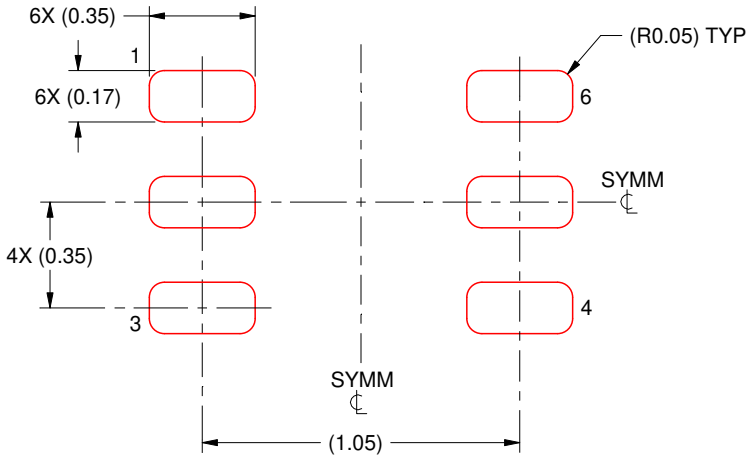
4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SCALE:40X

4220595/A 03/2020

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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