General Description

BDE-BLEM301 is one of the most cost-efficient Bluetooth 5.1 Low Energy Module in the field. Based on Dialog ultra-low power DA14531 SoC, it comprises a Cortex® M0+ MCU, 1Mbit on board Flash memory, a Bluetooth 5.1 Low Energy radio and a high efficiency PCB antenna in a single module. The module can be used with or without an external MCU. It also offers flexible hardware interfaces for sensor applications.

BDE-BLEM301 is compatible with Dialog DA14531 TINY™ Bluetooth Module - DA14531MOD. The same software tools and hardware kits can be used for BDE-BLEM301. Empowered by Dialog BT5.1 qualified BLE stack and SDK with a rich set of software functions & examples, BDE-BLEM301 is dedicated to help you build an ultra-low-power and ultra-low-cost device with minimum time to market.

Key Features

- Bluetooth
  - Compatible with Bluetooth v5.1, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US)
  - Supports up to 3 BLE connections
- Processing and memories
  - 16 MHz 32-bit Arm® Cortex® M0+ with SWD interface
  - 128 Kbytes internal FLASH
  - 48 Kbytes RAM
  - 144 Kbytes ROM
  - 32 Kbytes OTP
- Current Consumption
  - 2 mA RX at VBAT=3V
  - 4 mA TX at VBAT=3V and 0 dBm
  - 1.8 uA at sleep with all RAM retained
- Radio
  - Programmable RF transmit power from -19 to +2.2 dBm
  - -93 dBm receiver sensitivity
- Interfaces
  - Quadrature decoder with 3 channels
  - 4 channel 11-bit ENOB ADC
  - 2 general purpose timers with PWM capabilities
  - 9 GPIOs
  - SPI
  - 2 x UART, 1wire UART support
  - I2C
- Power Management
  - Operating range (1.8V - 3.3V)
  - Inrush current control
- Other
  - Real Time Clock
- Packaging
  - 12.5 mm x 14.5 mm x 2.1 mm package
- Module Software Development Kit
  - Configurable DSPS
  - Codeless v2.0
  - SDK6 support
- Module Software Tools
  - Flash/OTP programmer
  - SUOTA support
  - Battery Life Estimation
  - Data Rate Monitoring
  - Real-Time Power Profiling
  - Production Line Testing
- Standards Conformance
  - BQB
  - ETSI EN 300 328 and EN 300 440 Class 2 (Europe)
  - FCC CFR47 Part 15 (US)
- Compatible with Dialog DA14531MOD
- Commissioning/Provisioning

Applications

- Beacons
- Remote Controls
- Proximity tags
- Low Power Sensors
- Toys
- Serial port transmission
- Smart home
- Smart meters
- Smart medical devices

Contents

1. References

[1] DA14531, Datasheet, Revision 3.0, Dialog Semiconductor.

[2] DA14531 TINY™ Module DA14531MOD, Datasheet, Revision 1.0, Dialog Semiconductor.

[2] DA14585/DA14531 SW Platform Reference Manual (https://www.dialog-semiconductor.com/products/connectivity/bluetooth-low-energy/products/da14531)

2. Block Diagram

BLEM301 module is based on the Dialog Semiconductor DA14531 SoC configured in buck mode. With an integrated 128Kbytes flash, 32MHz XTAL and a on board PCB antenna, it allows faster time to market at reduced development cost.
The module, as seen in Figure 1, comprises of:

- 128kBytes (1 Mbit) SPI FLASH
- 32MHz XTAL
- 2 decoupling capacitors
- a power inductor
- a CLC filter and matching components for the printed antenna

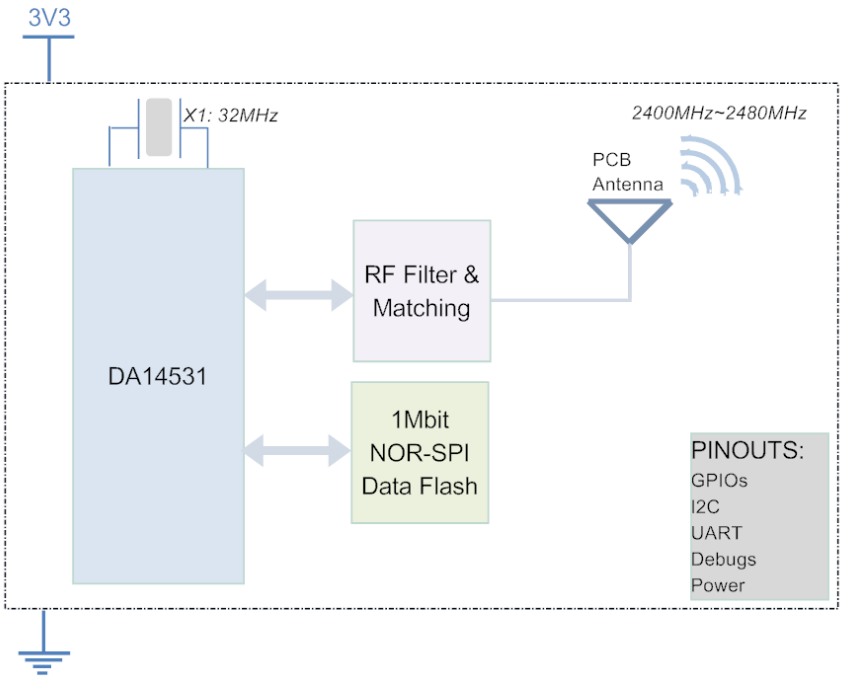


Figure 1: BLEM301 Module Block Diagram

3. Pinout

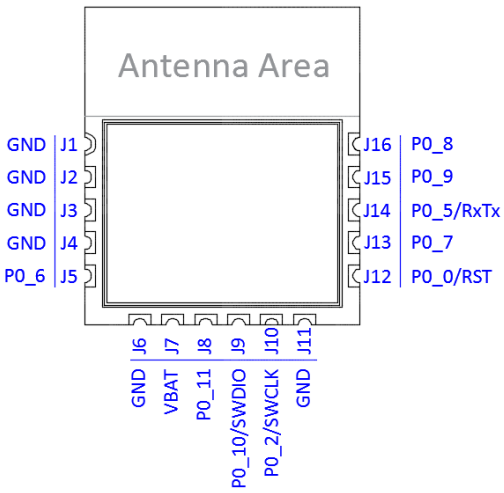


Figure 2: Pinout Diagram Top View

Note that, J1 has no internal connection and for this reason presents a difference pad shape. It was used ONLY for providing RF signal for certification purposes.

Table 1: Pin Description

Pin #	Pin Name	Type	Reset State	Description
J1	GND	GND		Ground
J2	GND	GND		Ground
J3	GND	GND		Ground
J4	GND	GND		Ground
J5	P0_6	DIO (Type A) Note[1]	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J6	GND	GND		Ground
J7	VBAT	PWR		INPUT. Battery connection. IO supply.
J8	P0_11	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.

[1] There are two types of pads, namely Type A and Type B. Type A is a normal IO pad with a Schmitt trigger on input while Type B has an extra RC Filter with a cutoff frequency of 100 kHz.

Pin #	Pin Name	Type	Reset State	Description
J9	P0_10	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
	SWDIO			INPUT/OUTPUT. JTAG Data input/output. Bidirectional data and control communication (by default).
J10	P0_2	DIO (Type B)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power-down.
	SWCLK			INPUT JTAG clock signal (by default).
J11	GND	GND		Ground
J12	P0_0	DIO (Type B) Note [2]	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power-down
	RST			RST active high hardware reset (default).
J13	P0_7	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J14	P0_5	DIO (Type B)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J15	P0_9	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.
J16	P0_8	DIO (Type A)	I-PD	INPUT/OUTPUT with selectable pull up/down resistors. Pull-down enabled during and after reset. General purpose I/O port bit or alternate function nodes. Contains state retention mechanism during power down.

I-PD stands for Input-Pulled Down while I-PU stands for Input-Pulled Up.
DIO stands for Digital Input-Output, PWR stands for power and GND stands for Ground.

[2] This pin is also used for the communication to the internal SPI FLASH

4. Characteristics

All MIN/MAX specification limits are guaranteed by design, production testing and/or statistical characterization. Typical values are based on characterization results at default measurement conditions and are informative only.
Default measurement conditions (unless otherwise specified): VBAT= 3.0 V, TA = 25 ℃. All radio measurements are performed with standard RF measurement equipment.

4.1. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 2: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
V_{BAT_LIM}	Limiting battery supply voltage		-0.1	3.6	V
T_{STG}	Storage temperature		-40	125	°C

4.2. Recommended Operating Conditions

Table 3: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{BAT}	Battery supply voltage	Allowing FLASH programming	1.65		3.3	V
V_{PIN}	Voltage on a pin		-0.1		3.3	V
T			-40		85	°C
V_{IH}	HIGH level input voltage	VDD=0.9V	0.7*VDD			V
V_{IL}	LOW level input voltage	VDD=0.9V			0.3*VDD	V

4.3. Device Characteristics

Table 4: DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{BAT_ACTIVE}	Battery supply current with CPU running CoreMark from RAM at 16MHz			0.42		mA
$I_{BAT\_BLE\_ADV\_100ms}$	Average battery supply current with system in Advertising state (3 channels) every 100ms and extended sleep with all RAM retained. TX output power at 2dBm. FLASH is off.			90		uA

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{BAT\_BLE\_CONN\_30ms}$	Average battery supply current with system in a connection state with 30ms connection interval and extended sleep with all RAM retained. TX output power at 2dBm. FLASH is off.			100		uA
I_{BAT_FLASH}	Battery supply current with CPU fetching code from serial FLASH. RF is off.			0.24		mA
I_{BAT_HIBERN}	Battery supply current with system shut down (Hibernation or shipping mode). FLASH is off.			0.48		uA
I_{BAT_IDLE}	Battery supply current with CPU in Wait for Interrupt Mode. FLASH is off.			0.24		mA
$I_{BAT\_SLP\_20KB}$	Battery supply current with system in extended sleep mode and 20KB RAM retained			1.5		µA
$I_{BAT\_SLP\_48KB}$	Battery supply current with system in extended sleep mode and all RAM retained			1.8		µA
$I_{BAT\_RF\_RX}$	Battery supply current	Continuous RX; VBAT=3V; FLASH in sleep mode; DCDC converter is on; TA = 25 °C		2		mA
$I_{BAT\_RF\_TX\_0dBm}$	Battery supply current	Continuous TX; VBAT=3V; FLASH in sleep mode; DCDC converter is on; Output power at 0 dBm; TA = 25 °C		4		uA
$I_{BAT\_RF\_TX\_+3dBm}$	Battery supply current	Continuous TX; VBAT=3V; FLASH in sleep mode; DCDC converter is on; Output power at 3 dBm; TA = 25 °C		5		uA
$I_{BAT\_RF\_TX\_-3dBm}$	Battery supply current	Continuous TX; VBAT=3V; FLASH in sleep mode; DCDC converter is on; Output power at-3 dBm; TA = 25 °C		3		mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
$I_{BAT\_RF\_TX\_-6dBm}$	Battery supply current	Continuous TX;VBAT=3V; FLASH in sleep mode; DCDC converter is on; Output power at-6 dBm; TA = 25 °C		2.3		uA
$I_{BAT\_RF\_TX\_-12dBm}$	Battery supply current	Continuous TX; VBAT=3V; FLASH in sleep mode; DCDC converter is on; Output power at-12 dBm; TA = 25 °C		1.8		mA
$I_{BAT\_RF\_TX\_-18dBm}$	Battery supply current	Continuous TX; VBAT=3V; FLASH in sleep mode; DCDC converter is on; Output power at-18 dBm; TA = 25 °C		1.5		µA

Table 5: XTAL32MHz - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{XTAL_32M}	Crystal oscillator frequency			32		MHz
Δf_{XTAL}	Crystal frequency tolerance	After trimming; Including aging and temperature drift	-25		25	ppm

Table 6: Digital IO - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH level input voltage	VDD=0.9V	0.52			V
V_{IL}	LOW level input voltage	VDD=0.9V			0.27	V

Table 7: Digital IO - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{IH}	HIGH level input current	$V_I=V_{BAT\_HIGH}$=3.0V	-10		10	uA
I_{IL}	LOW level input current	V_I=Vss=0V	-10		10	uA
I_{IH}	HIGH level input current	$V_I=V_{BAT}$=3.0V	60		180	uA
I_{IL}	LOW level input current	V_I=Vss=0V, V_{BAT}=3.0V	-180		-60	uA
I_{IH}	HIGH level output voltage	I_O=3.5mA, V_{BAT}=1.8V	0.8*VBAT			V
I_{IL}	LOW level output voltage	I_O=3.5mA, V_{BAT}=1.8V			0.2*VBAT	V
I_{IH}	HIGH level output voltage	I_O=0.3mA, V_{BAT}=1.8V	0.8*VBAT			V
I_{IL}	LOW level output voltage	I_O=0.3mA, V_{BAT}=1.8V			0.2*VBAT	V
I_{IH}	input capacitance			TBD		pF

Table 8: Radio 1Mbps - Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{OPER}	Pperating frequency		2400		2483.5	MHz
N_{CH}	Number of channels			40		1
F_{CH}	Channel frequency	K = 0 to 39		2402=K*2		MHz

Table 9: Radio 1Mbps - AC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{SENS_EPKT}	Sensitivity level	Extended packet size (255 octets)		-91		dBm

5. Mechanical Specifications

5.1. Dimensions

The module dimensions are presented in the following figure:

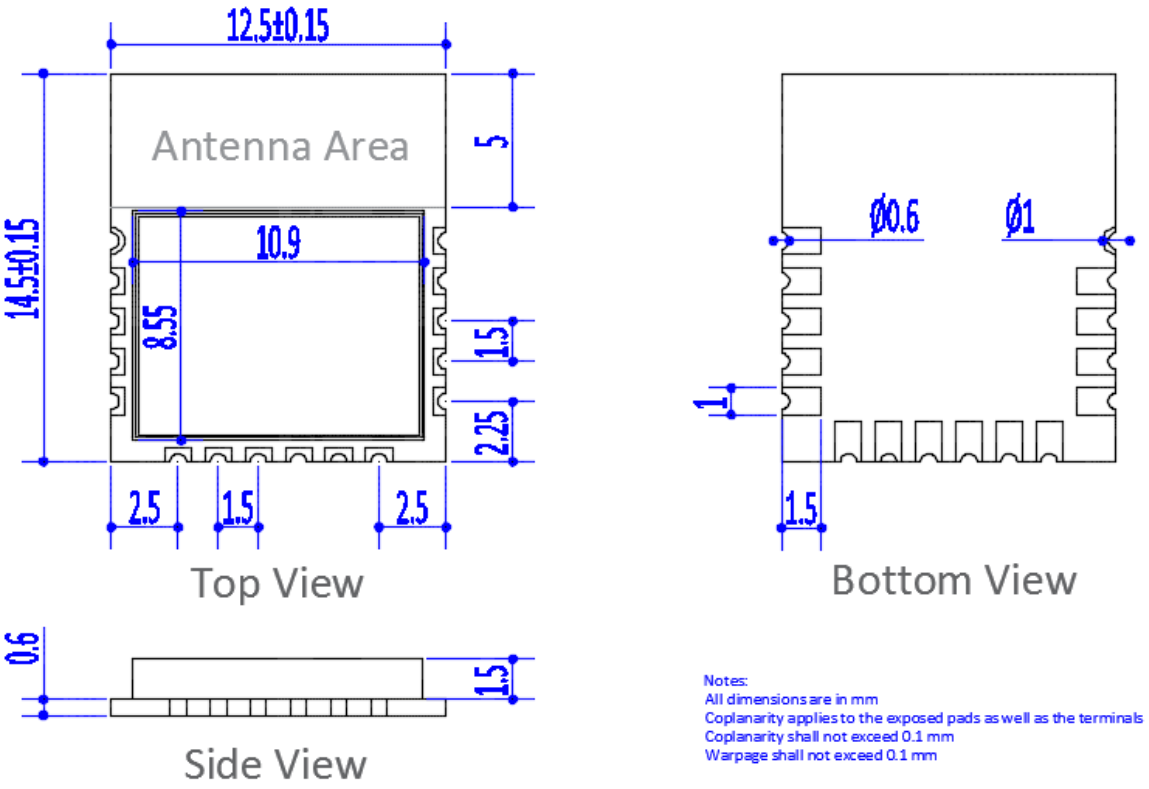


Figure 3: Mechanical Drawing

5.2. PCB Footprint

The footprint for the PCB is presented in the following figure:

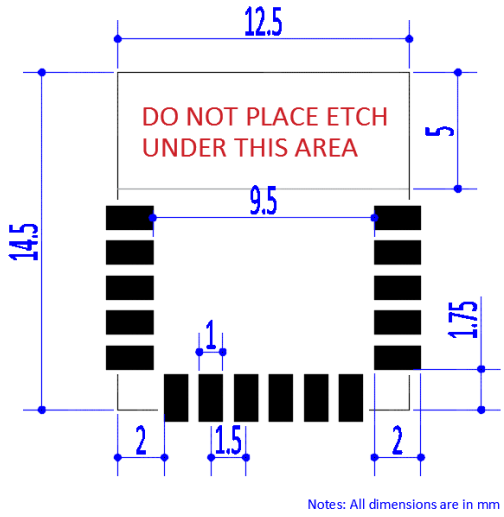


Figure 4: Module Footprint Top View

5.3. Marking

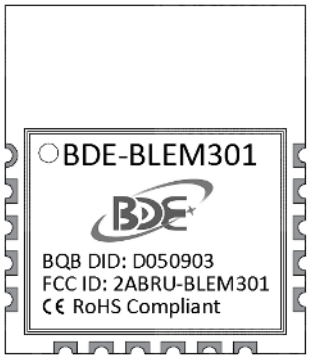


Figure 5: Indicative Module Shield Marking

6. Packaging Information

6.1. Tape & Reel

Tape & Reel or Tray, 1K MPQ.

6.2. Labeling

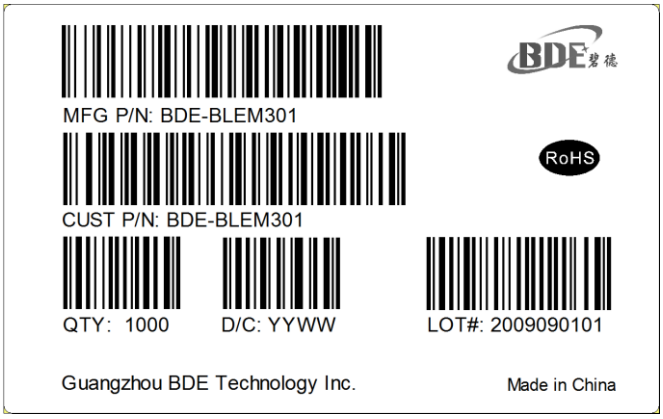


Figure 6: Reel Label

7. Application Information

A typical reference diagram of BDE-BLEM301 is presented in the following figure:

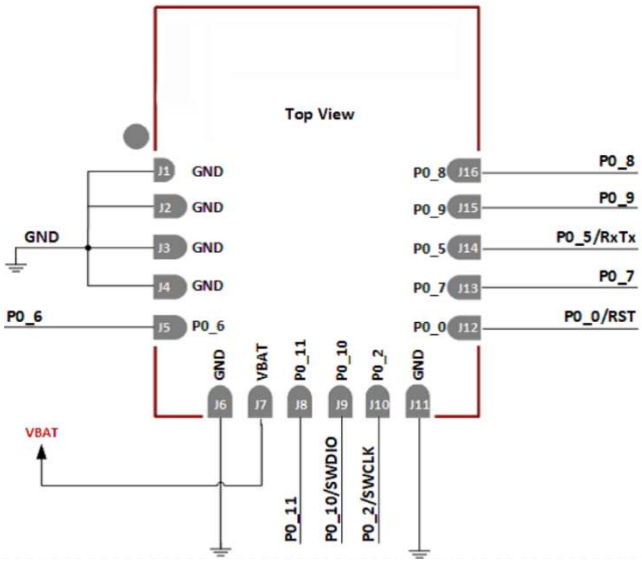


Figure 7: Reference Diagram

There are some special considerations regarding using this module, namely:

- RST signal is shared with the MOSI input of the NOR flash. For this reason, RST must not be driven to GND. When internal Flash is in use, reset functionality is not available.
- The SPI Bus of DA14531 is used for the communication of the BLE SoC with the NOR Flash at boot time. Three of the four signals are not driven to external module pins. For this reason, a sensor that utilizes the SPI bus must be assigned (by software) on to the module pins to communicate with after booting and when NOR Flash is no longer in use. An example is presented in the following figure.

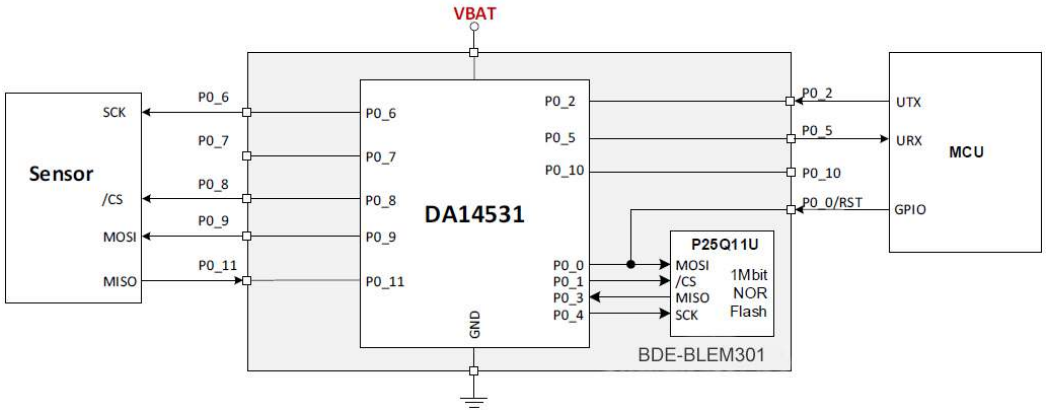


Figure 8: Example of Connecting a Sensor to the SPI Bus and an MCU to RST and UART

Note that P0_0/RST pin should not be driven while the module is booting from its internal SPI FLASH.

8. Design Guidelines

BDE-BLEM301 comes with an integrated PCB trace antenna. Antenna area is 12.5 x 5 mm. The antenna is characterized in terms of Voltage Standing Wave Ratio (VSWR) and efficiency.

The PCB trace antenna radiated performance depends on the host PCB layout. The Antenna gain is better than -1 dBi when mounted on a 50 x 50 mm reference board. Radiation pattern is omnidirectional. The RF front end has been optimized to achieve the maximum possible efficiency for various mounting positions of the module on a host PCB. To obtain similar performance, guidelines described in the following sections should be followed.

8.1. Placement

For optimum performance, the module should be placed at the edge of a host PCB with the antenna edge facing out. The module can be located on either of the outer corners or the middle of the host PCB with equivalent performance.

Proximity with copper or laminate next to the PCB trace antenna affects the efficiency of the antenna. The antenna should have 4 mm free space in all directions. Laminate or copper under the antenna should be avoided as it severely affects the performance of the antenna. Antenna keep-out area can be seen in Figure 9.

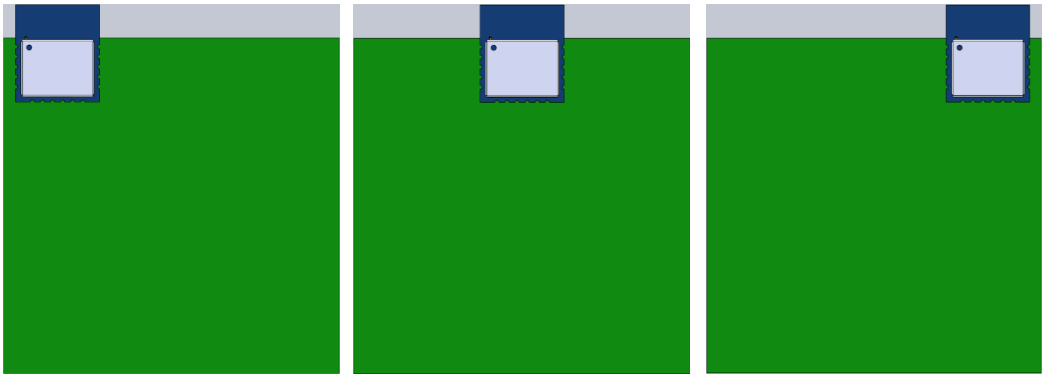
Metals close to the antenna will cause degradation on antenna performance. The amount of

degradation depends on the host system characteristics.

Following table summarizes antenna efficiency for different placements on a host PCB as indicated in Figure 9.

Table 10: Antenna gain and efficiency vs module positions

Frequency	Position #1		Position #2		Position #3	
	Gain (dBi)	Efficiency	Gain (dBi)	Efficiency	Gain (dBi)	Efficiency
2400 MHz	2.68	51.02%	-0.35	34.12%	1.75	46.40%
2410 MHz	2.67	51.60%	-0.18	35.87%	1.89	47.22%
2420 MHz	2.73	51.24%	-0.12	36.90%	1.96	46.88%
2430 MHz	2.90	51.52%	0.03	38.32%	2.00	47.11%
2440 MHz	3.15	54.14%	0.57	42.08%	2.23	50.00%
2450 MHz	3.26	56.49%	0.98	45.56%	2.34	51.84%
2460 MHz	3.20	57.63%	1.33	48.78%	2.45	53.03%
2470 MHz	3.15	56.26%	1.34	49.51%	2.34	51.89%
2480 MHz	2.88	53.78%	1.32	49.02%	2.21	50.01%
2490 MHz	2.58	51.67%	1.35	48.16%	2.16	48.91%
2500 MHz	2.61	50.40%	1.24	46.50%	2.05	48.07%



Position #1 Position #2 Position #3

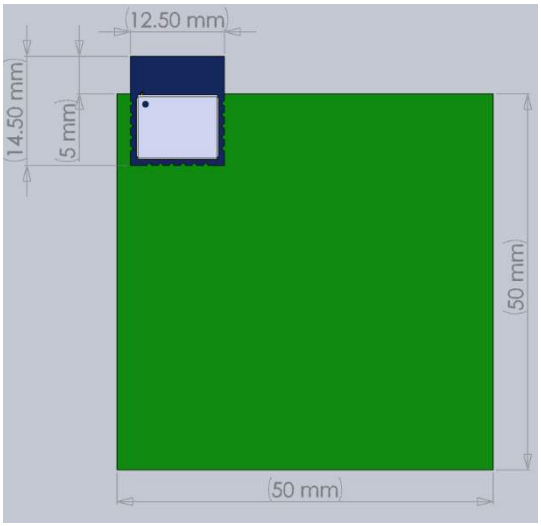


Figure 9: Mounting Positions for Optimum Antenna Performance

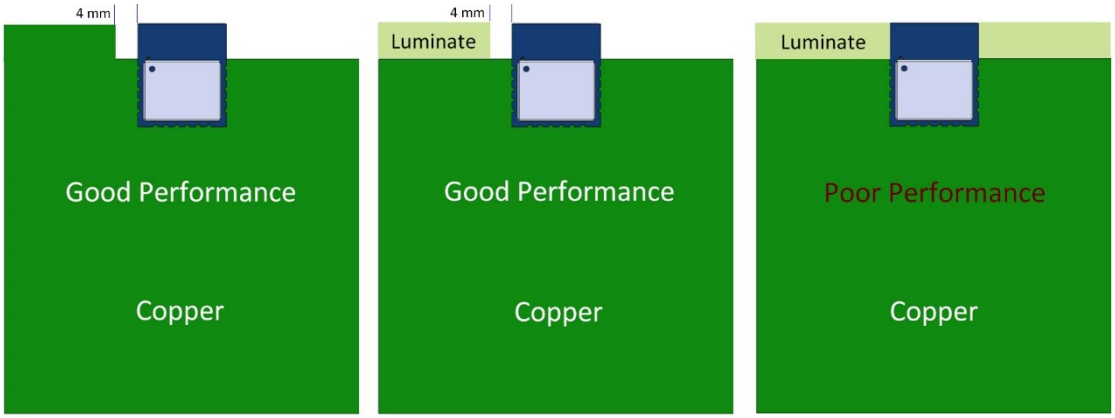


Figure 10: Antenna Performance Proximity with Copper (Left), Laminate (Middle) and Laminate Under Antenna (Right)

The actual module evaluation board layout that has been used to conduct all measurements is presented in the following figure:

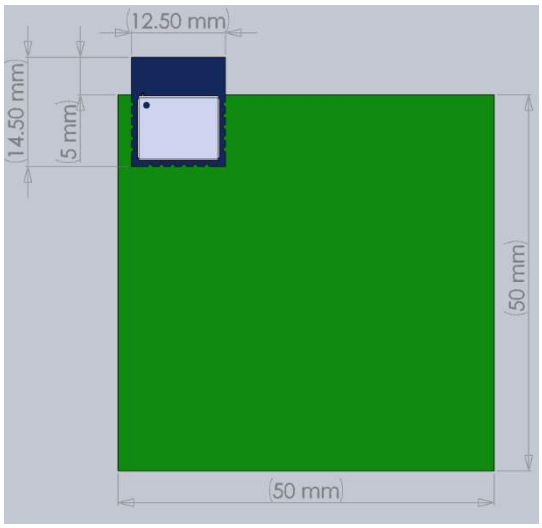


Figure 11: Module Evaluation Board Dimension

8.2. Antenna Graphs

Antenna VSWR measurements for the three mounting positions are described in the following figures:

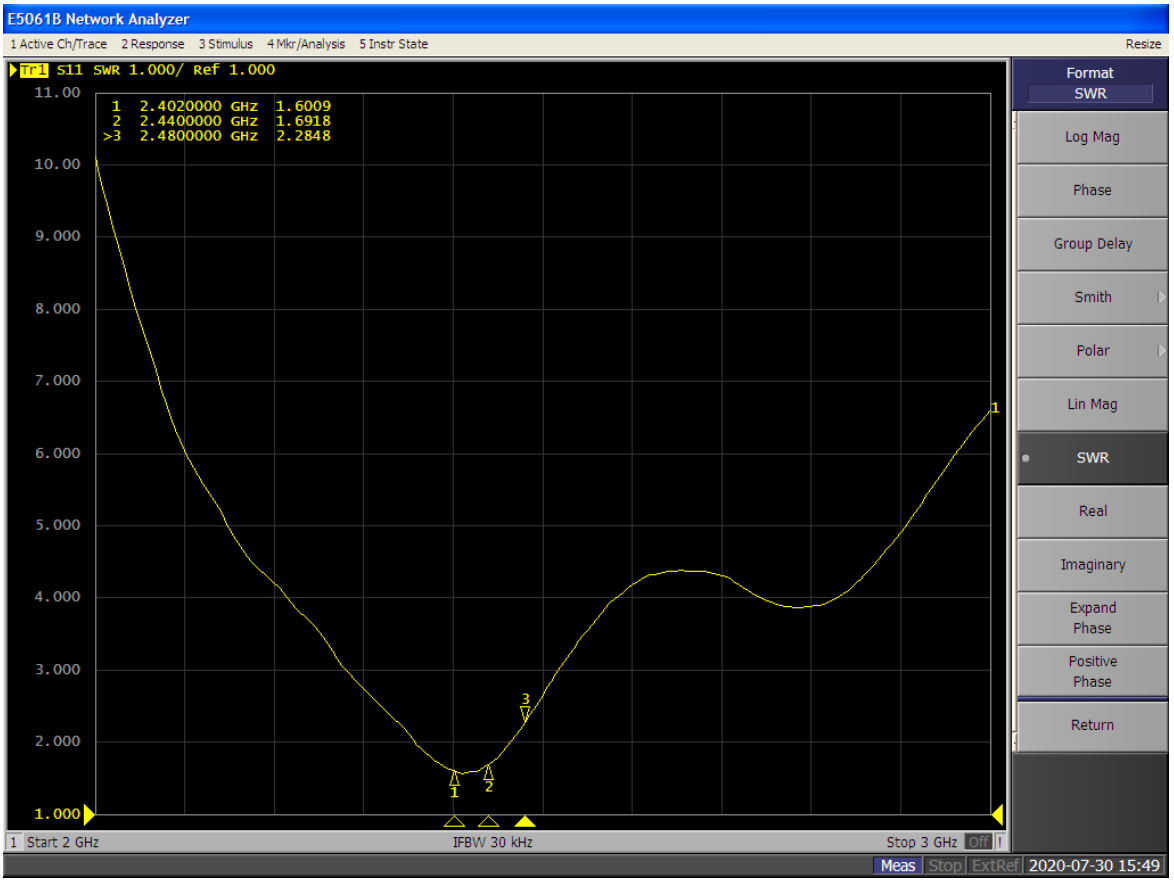


Figure 12: VSWR Mounted in the Upper Left Corner (Position #1) of Evaluation Board

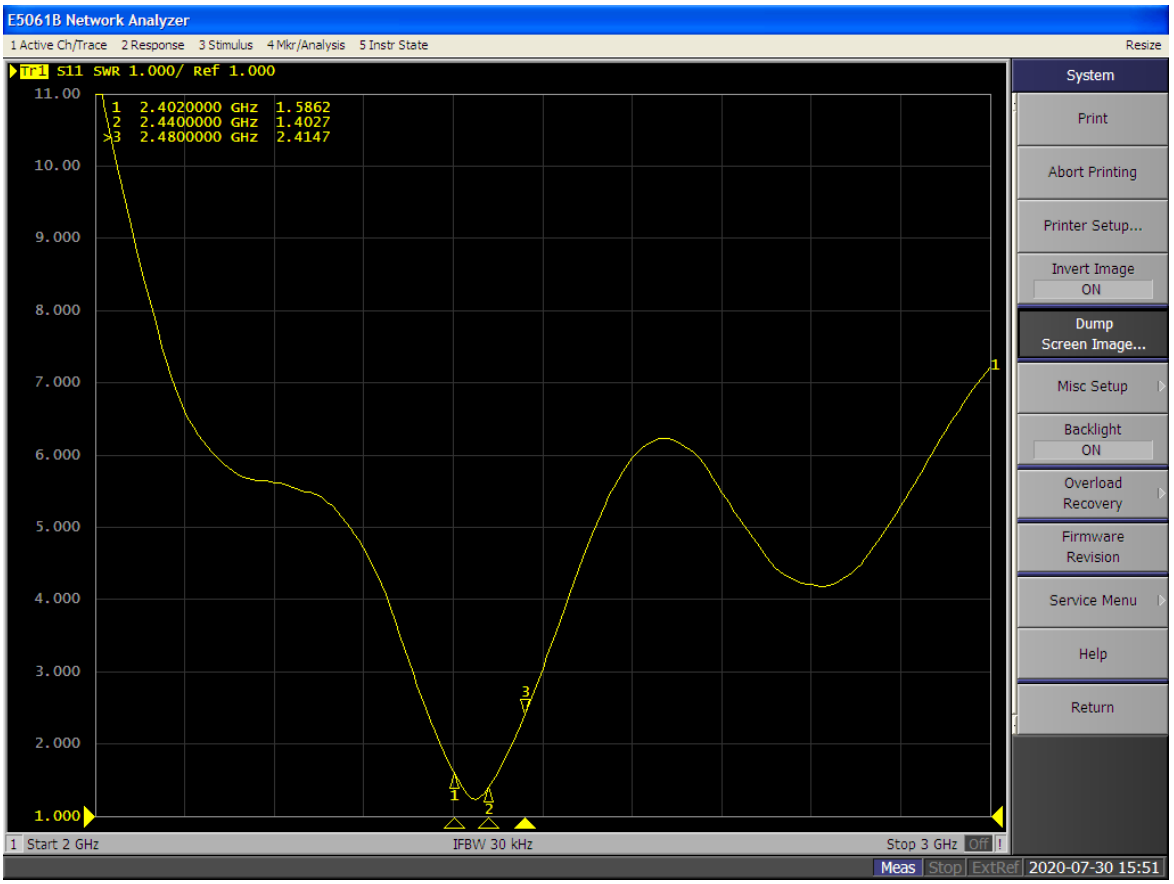


Figure 13: VSWR with Module Mounted in Center (Position #2) of the Evaluation Board

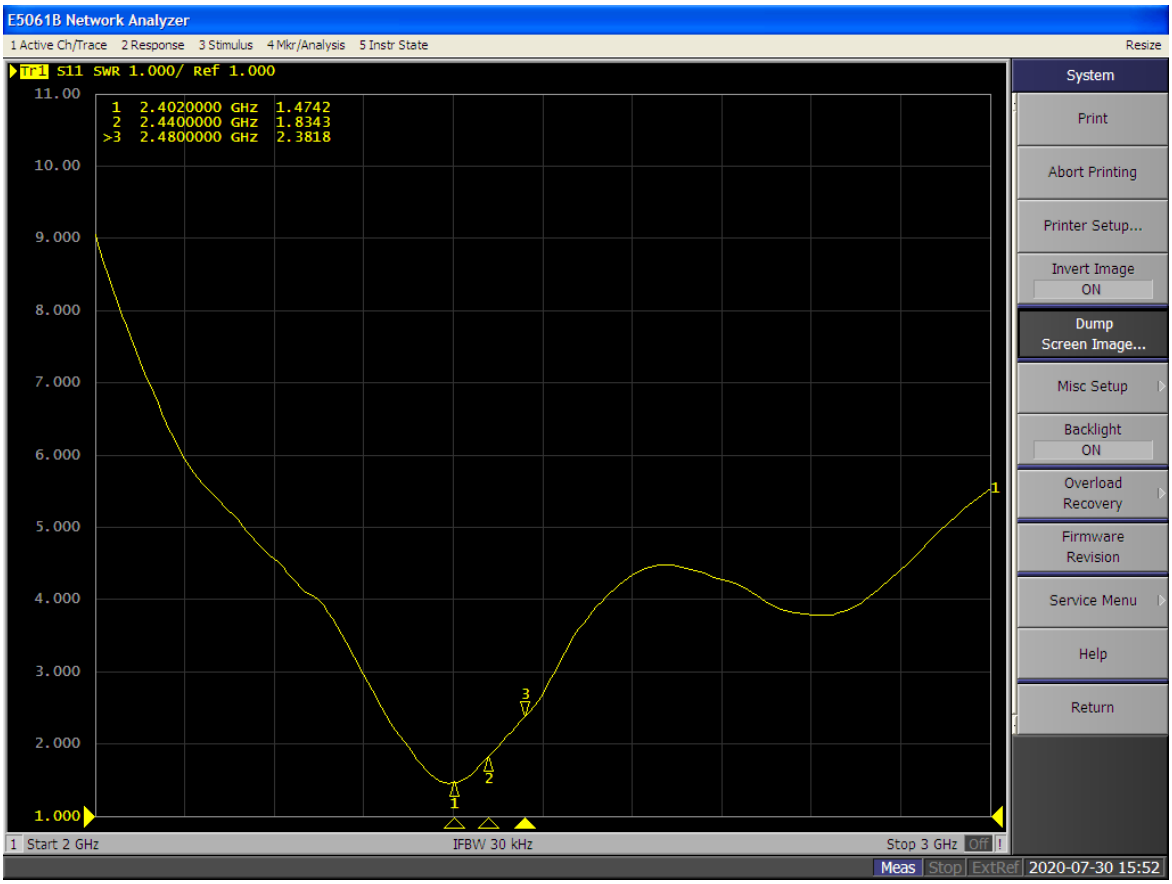


Figure 14: VSWR with Module Mounted in Center (Position #2) of the Evaluation Board

8.3. Radiation Pattern

The module is tested with the placement to the left corner of the host PCB, and the orientation is as below picture. The antenna radiation pattern measurements are carried out in an anechoic chamber. Radiation patterns are presented for three measurement planes: XY, XZ and YZ planes.

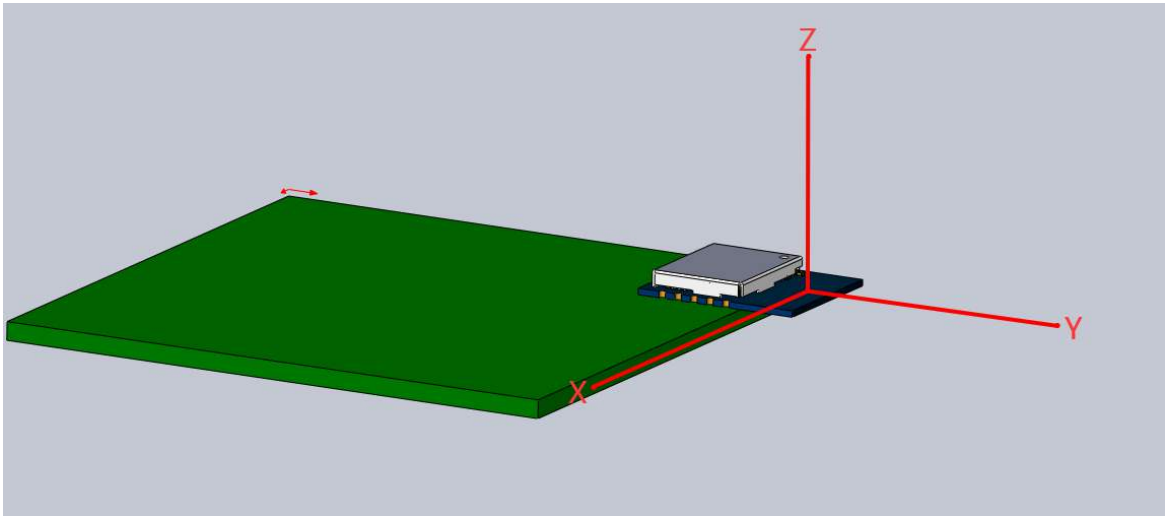


Figure 15: The Orientation of the DUT

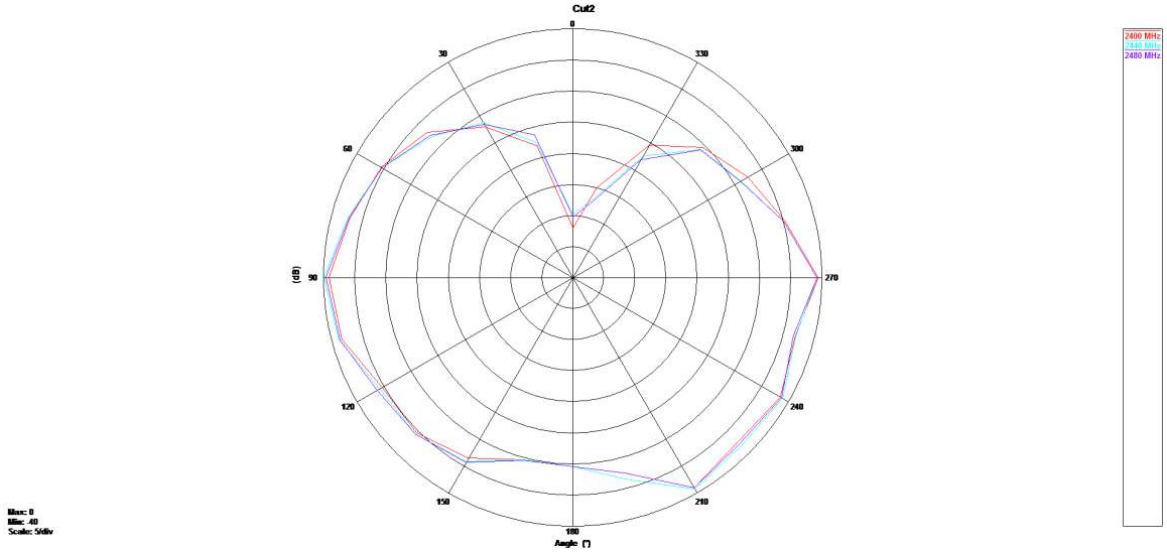


Figure 16: XZ Plane (Phi = 0°)

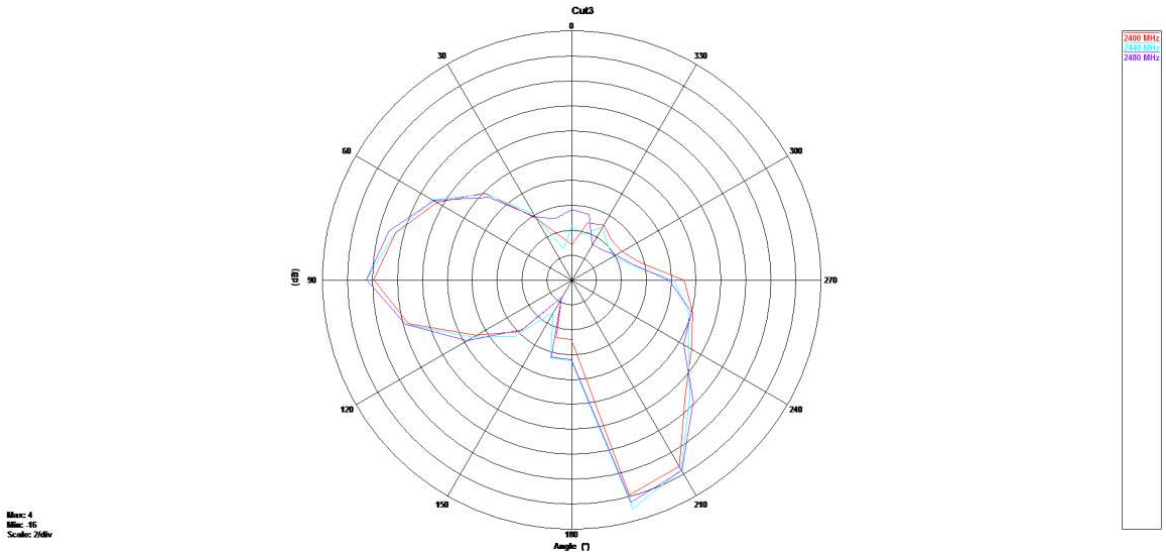


Figure 17: YZ Plane (Phi = 90°)

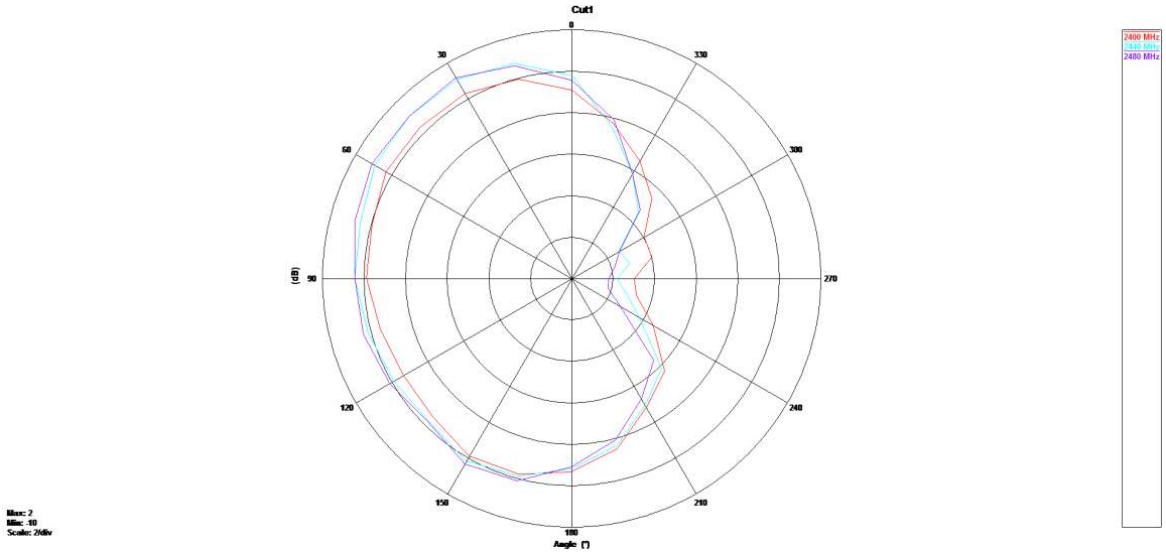


Figure 18: XY Plane (Theta = 90°)

9. Soldering

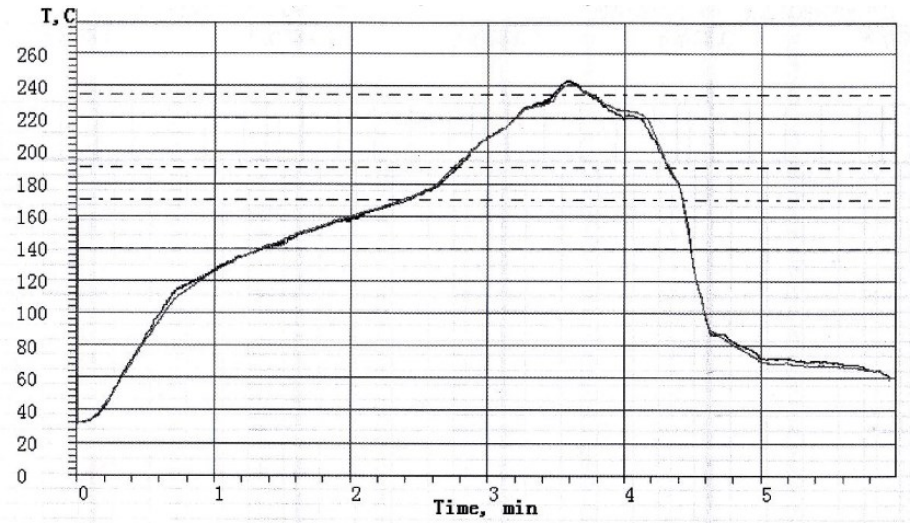


Figure 19: Typical Reflow Profife

10. Ordering Information

Table 11: Ordering Information

Part Number	Size (mm)	Shipping Form	MOQ
BDE-BLEM301	12.5 x 14.5 x 2.1	Tape & Reel	1000

11. Regulatory Information

11.1. Integration Instructions

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

(1) List of applicable FCC rules
FCC Part 15.247

(2) Specific operational use conditions
This transmitter/module and its antenna must not be co-located or operating in conjunction with any transmitter. This information also extends to the host manufacturer's instruction manual.

(3) Limited module procedures
Not applicable.

(4) Trace antenna designs
Not applicable.

(5) RF exposure considerations
This equipment complies with FCC RF radiation exposure limits set forth for an uncontrolled environment. This compliance to FCC radiation exposure limits for an uncontrolled environment, and

minimum of 20cm separation between antenna and body.
The host product manufacturer would provide the above information to end users in their end-product manuals.

(6) Antennas
PCB antenna: 6.15 dBi, 2.4 GHz~2.5 GHz

(7) Label and compliance information
The end product must carry a physical label or shall use e-labelling followed KDB784748D01 and KDB 784748 stating “Contains Transmitter Module FCC ID: 2ABRU-BLEM301”.

(8) Information on test modes and additional testing requirements
For more information on testing, please contact the manufacturer.

(9) Additional testing, Part 15 Subpart B disclaimer
The modular transmitter is only FCC authorized for the specific rule parts (FCC Part 15.247) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. The final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed when contains digital circuitry.

11.2. FCC Statement

Integrator is reminded to assure that these installation instructions will not be made available to the end user of the final host device.

The final host device, into which this RF Module is integrated has to be labelled with an auxiliary label stating the FCC ID of the RF Module, such as "Contains FCC ID: 2ABRU-BLEM301”.

"This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation."

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

(OEM) Integrator has to assure compliance of the entire end-product incl. the integrated RF Module.

For 15 B (§15.107 and if applicable §15.107) compliance, the host manufacturer is required to show compliance with 15 while the module is installed and operating.

Furthermore the module should be transmitting and the evaluation should confirm that the module's intentional emissions (15C) are compliant (fundamental / out-of-band). Finally the integrator has to apply the appropriate equipment authorization (e.g. Verification) for the new host device per definition in §15.101.

11.3. Module Statement

The single-modular transmitter is a self-contained, physically delineated, component for which compliance can be demonstrated independent of the host operating conditions, and which complies with all eight requirements of § 15.212(a)(1) as summarized below.

(1) The radio elements have the radio frequency circuitry shielded.
(2) The module has buffered modulation/data inputs to ensure that the device will comply with Part 15 requirements with any type of input signal.
(3) The module contains power supply regulation on the module.
(4) The module contains a permanently attached antenna.
(5) The module demonstrates compliance in a stand-alone configuration.
(6) The module is labeled with its permanently affixed FCC ID label.
(7) The module complies with all specific rules applicable to the transmitter, including all the conditions provided in the integration instructions by the grantee.
(8) The module complies with RF exposure requirements.

This transmitter/module must not be collocated or operating in conjunction with any other antenna or transmitter.

Revision History

Revision	Date	Description
V1.0	27-July-2020	Initial Released
V1.1	5-August-2020	Update marking, add Integration Instruction, FCC Statement, Module Statement
V1.2	13-November-2020	Update Block Diagram, editing, add product picture, labeling, soldering profile
V1.3	14-November-2020	Editorial correction
V1.4	13-January-2021	Editorial change
V1.5	14-April-2021	Editorial change

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