Product Document

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Datasheet

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AS5715A/AS5715R

On-/Off-Axis Inductive Position Sensor with Sin/Cos Output

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Content Guide

1 General Description

The AS5715A/AS5715R is an inductive sensor IC with differential SIN/COS output for high speed position sensing applications. To fulfill its purpose, the AS5715A/AS5715R device has to be connected to a coil system. The coil system consists of a TX (transmitting) and two RX (receiving) coils typically integrated on a PCB (Printed Circuit Board). The device excites the TX coil with a high frequency voltage. A target above the coil system effects the amount of voltage induced into the RX coils depending on the position of the target. The device senses, demodulates, and amplifies this voltage. If If the coil system is designed properly, then the device output delivers SIN and COS shaped voltages. An ECU (Electronic Control Unit) can calculate the target position by applying an atan2() function to the SIN and COS output signal. The AS5715A/AS5715R is defined as SEooC (Safety Element out of Context) according ISO26262.

1.1 Key Benefits & Features

The benefits and features of AS5715R, On-/Off-Axis Inductive Position Sensor with Sin/Cos Output, are listed below:

Figure 1:
Added Value of Using AS5715R

Features	Benefits
On and off axis applications	Flexible PCB design possible. Enabling hollow shaft and side shaft applications.
Adaptable coil system layout	Adaptable to the pole pair count of the motor
Typical accuracy with 4 pole-pair configuration: <0.075 deg mechanical, <0.3 deg electrical	Low torque ripple and motor noise and increased efficiency
Suitable for high speed applications	3.3 µs propagation delay and output bandwith for applications up to 480000 rpm
Differential SIN and COS output	Easy replacement of existing AMR/GMR sensors
Functional safety diagnostics	ASIL C(D) as SEooC
Suitable for automotive applications	AEC-Q100 Grade 0 qualified up to -40 to 160 °C

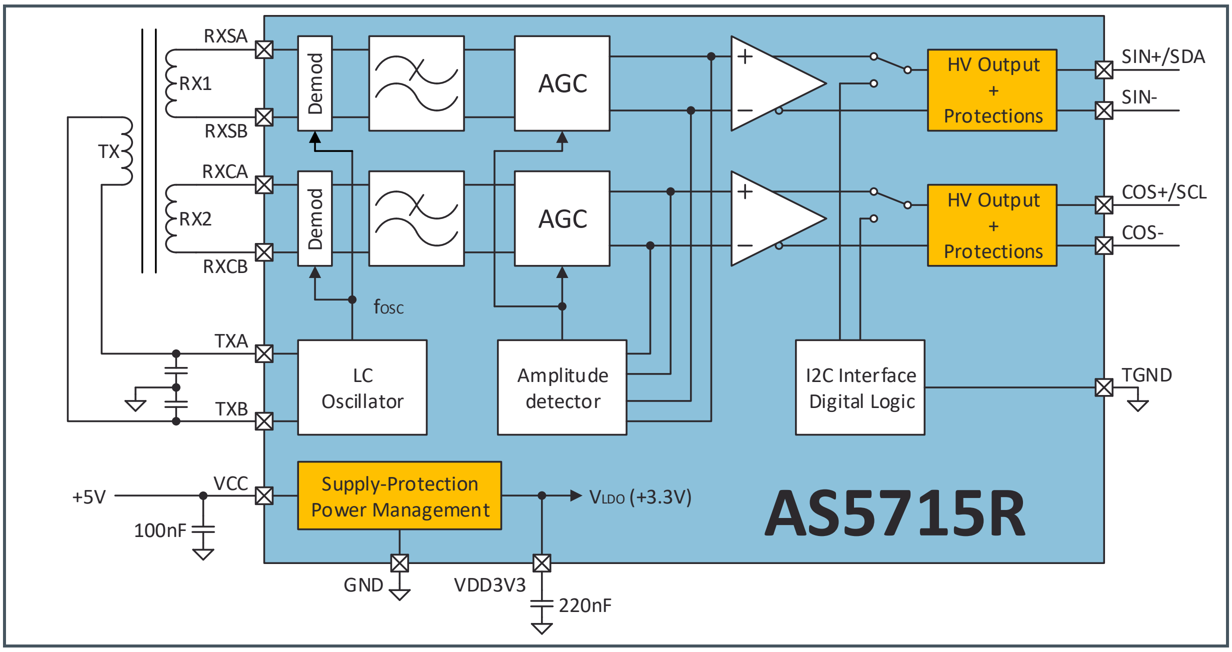
1.2 Applications

Typical applications are: BLDC motor control, traction motors for electric vehicles, electric power steering, brake boosters, replacement of expensive and bulky resolvers, mirror LIDAR and closed loop servo motor systems.

1.3 Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of AS5715R



2 Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS5715R-ZTST	TSSOP-14	AS5715R	Tape & Reel	4500 pcs/reel
AS5715R-ZTSM	TSSOP-14	AS5715R	Tape & Reel	500 pcs/reel
AS5715A-ZTST	TSSOP-14	AS5715A	Tape & Reel	4500 pcs/reel
AS5715A-ZTSM	TSSOP-14	AS5715A	Tape & Reel	500 pcs/reel

The AS5715A is a preprogrammed derivative of the AS5715R. This means that the AS5715A is not programmable. The table below shows how the registers of the AS5715A are programmed:

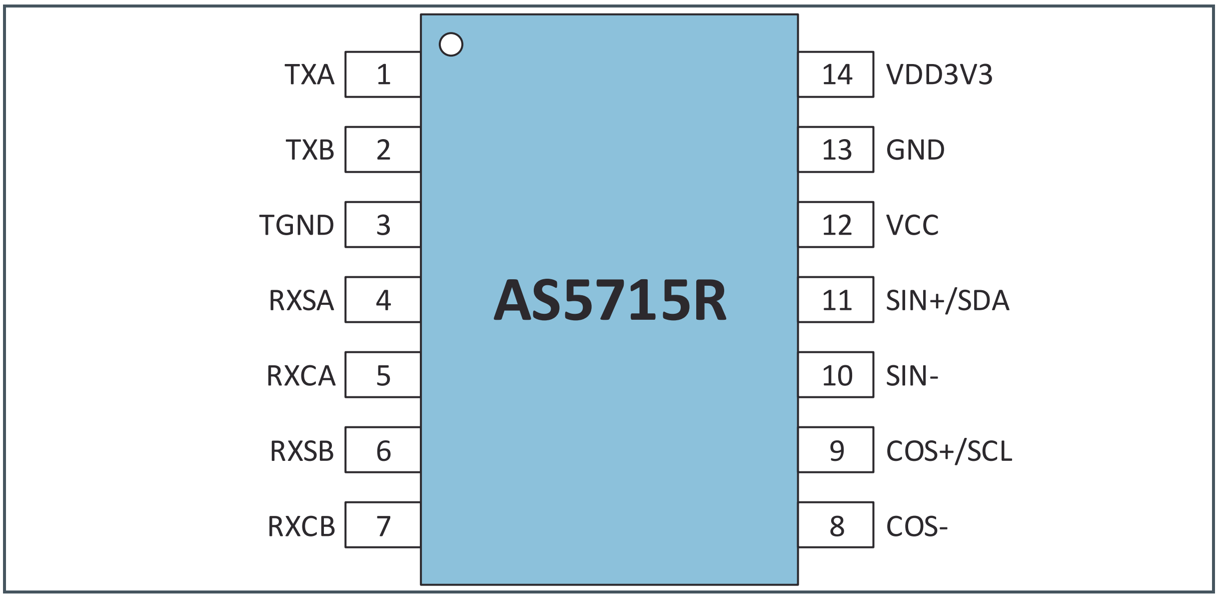
Register	Content
1Dh	C0h
1Eh	D0h

The tolerance of the preprogrammed AS5715A gain factor is ± 1dB.

3 Pin Assignment

3.1 Pin Diagram

Figure 3:
TSSOP-14 Pin Assignment



3.2 Pin Description

Figure 4:
Pin Description of AS5715R (TSSOP14)

Pin Number	Pin Name	Pin Type(1)	Description	Comments
1	TXA	AO	1st side of transmit coil connection	
2	TXB	AO	2nd side of transmit coil connection	
3	TGND	DI	TEST pin	Connect either to GND or VDD3V3 in normal operation
4	RXSA	AI	SIN channel RX input	
5	RXCA	AI	COS channel RX input	
6	RXSB	AI	SIN channel RX input	
7	RXCB	AI	COS channel RX input	
8	COS-	AO	Inverting COS output	
9	COS+/SCL	AO (DI)	Non inverting COS output (SCL in I^2C mode)	
10	SIN-	AO	Inverting SIN output	
11	SIN+/SDA	AO (DIO)	Non inverting SIN output (SDA in I^2C mode)	
12	VCC	S	Input for 5 V Power supply operation	
13	GND	S	Reference GND	
14	VDD3V3	AO	Output of internal LDO	

(1) Explanation of abbreviations:

DI	Digital Input
DIO	Digital Input/Output
AI	Analog Input
AO	Analog Output
S	Supply Pin

4 Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5
Absolute Maximum Ratings of AS5715R

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{CC}	Supply Voltage to Ground	-20	20	V	Applicable for pin VCC
V_{OUT}	Output pin Voltage to GND	-0.3	20	V	Applicable for pins COS+, COS-, SIN+, SIN-
V_{LDO}	Output pin Voltage to GND	-0.3	5.0	V	Applicable for pin VDD3V3
V_{TX}	Output pin Voltage to GND	-0.3	3.6	V	Applicable for pin TXA, TXB
V_{RX}	Input pin Voltage to GND	-0.3	3.6	V	Applicable for pin RXSA, RXSB,RXCA, RXCB
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	AEC-Q100-004
Continuous Power Dissipation (T_A = 160 °C)					
P_T	Continuous Power Dissipation		112	mW	
Electrostatic Discharge					
$ESD_{HBM\ on\ Chip\ level}$	Electrostatic Discharge Human Body Model	± 4000		V	AEC-Q100-002
$ESD_{MM\ on\ Chip\ level}$	Electrostatic Discharge Machine Model	± 150		V	AEC-Q100-003
$ESD_{CDM\ on\ Chip\ level}$	Electrostatic Discharge Charged Device Model	± 500		V	AEC-Q100-011
$ESDC_{CDM\ on\ Chip\ level}$	Electrostatic Discharge CDM on corner pins	± 750		V	AEC-Q100-011
Temperature Ranges and Storage Conditions					
T_A	Operating Ambient Temperature	-40	160	°C	
R_{THJA}	Junction to Ambient Thermal Resistance		89	°C/W	
T_J	Operating Junction Temperature		170	°C	
T_{STRG}	Storage Temperature Range	- 55	125	°C	150 °C for 1000 h
T_{BODY}	Package Body Temperature		260	°C	IPC/JEDEC J-STD-020E(1)
R_{HNC}	Relative Humidity (non-condensing)	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a maximum floor life time of 168 hours

Symbol	Parameter	Min	Max	Unit	Comments
Lifetime and Temperature Profiles					
t_{OP_160}	Cumulative duration in operation	1500		h	T_A = 160 °C

(1) The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020E "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices." The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn)

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

All in this datasheet defined tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

Overall condition: T_A = -40 °C to 160 °C, VCC = 4.5 V to 5.5 V; components specification; unless otherwise noted.

5.1 Power Supply

Figure 6:
Power Supply

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC	Guaranteed positive supply voltage with regulator in use	Beyond that the chip may go into safe state within the VCC_{OVT}/VCC_{UVT} ranges but will continue to work in spec up until that thresholds (no grey zones)	4.5	5.0	5.5	V
t_{VCC_RISE}	VCC supply rise time, rise time has to be higher than specified Min	Guaranteed by design	100			ns
ICC	Supply current	Without output current and Q_{TX} = 40	5	10	12	mA
		Without output current and Q_{TX} = 8, (guaranteed by design)	5		15	mA
t_{START}	Start-up time	Functional mode (guaranteed by design)			3	ms

5.2 Analog Signal Chain

Figure 7:
Analog Signal Chain

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RX}	Input Level on all RX pins	Information parameter (guaranteed by design)	5		200	mVpp
n_{RX}	Differential noise on input	10-30 kHz (guaranteed by design)			1	Vpp
RX_ERR[(1)]	Overall electrical angular error of RX channels	With offset compensation in the ECU (guaranteed by design)			1	°
RX_ERR_{UNCOMP}[(2)]	Overall electrical angular error of RX channels	Without offset and gain compensation			4	°
INL_{RX}	Gain linearity of RX channel	Guaranteed by design			1	%
Delay_error	Phase shift between the SIN and COS channel at f_{IN} = 8 kHz				0.3	°
f_{IN}[(3)]	Frequency of the signal AM modulated to the LC oscillators frequency f_{TX}.		0		8	kHz
$t_{PROPDELAY}$	Propagation delay	SC_filter enabled (guaranteed by design)	3.5	4.65	5.8	µs
		SC_filter disabled (guaranteed by design)	2	2.65	3.3	µs
AGC_{GAIN_H}	Gain factor high		49			dB
AGC_{GAIN_L}	Gain factor low				27	dB
$V_{AGC\_REG\_L}$	AGC low level regulation threshold for p-p signal	Default configuration AGC_cmp_high_thr = 0	32	35	38	% of VCC
		Extended configuration AGC_cmp_high_thr = 1	45	48.5	52	% of VCC
$V_{AGC\_REG\_H}$	AGC high level regulation threshold for p-p signal	Default configuration AGC_cmp_high_thr = 0	66	70	74	% of VCC
		Extended configuration AGC_cmp_high_thr = 1	91	95	99	% of VCC
AGC_{STEP_REG}	AGC regulation gain factor	When V_{AGC_REG} threshold is reached		0.25		dB
t_{REG}	Regulation wait time			25		µs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{AGC\_LIMIT\_L}$	AGC zero crossing threshold for p-p signal	Default configuration AGC_cmp_high_thr = 0	6	9	12	% of VCC
		Extended configuration AGC_cmp_high_thr = 1	9	12	16	% of VCC
$V_{AGC\_LIMIT\_H}$	AGC high level clipping threshold for p-p signal	Default configuration AGC_cmp_high_thr = 0	86	90	93	% of VCC
		Extended configuration AGC_cmp_high_thr = 1	118	122	126	% of VCC
AGC_{STEP_LIMIT}	AGC step gain factor step	When V_{AGC_LIMIT} threshold is reached		3		dB
t_{LIMIT}	Step wait time			3		µs
gain_mm	Overall gain mismatch between SIN and COS channel	Guaranteed by design			2	%

(1) This error includes noise and gain mismatch as main error contributor but also errors caused by other effects. The error caused by noise can be decreased by an input signal with higher amplitude. The error caused by gain mismatch can be reduced by gain error compensation in the ECU. Guaranteed between 10% to 90% of VCC peak to peak differential output.

(2) The parameter RX_ERR_{UNCOMP} specifies the overall uncompensated angular error produced by the IC only, assuming ideal RX input signals. This parameter includes INL_{RX}, Delay_error, V_{OFFSET_RX}, OPN and gain_mm.

(3) Typical calculation: f_{IN} = (rotation_speed_in_rpm / 60) * num_of_pole_pairs

5.3 LC - Oscillator

Figure 8:
LC - Oscillator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{TX}	Coil driving voltage		2.0	2.5	3.0	Vpp
f_{TX}	Dependent on resonant frequency of external LC Tank		2.8		5	MHz
$f_{DET\_WD\_low}$	Lower LC frequency error detection level		2.4	2.6	2.8	MHz
$f_{DET\_WD\_high}$	Upper LC frequency error detection level	Default configuration LC_wide_range = 0	5	5.5	6	MHz
		Extended configuration LC_wide_range = 1	6.9	7.5	8.1	MHz
t_{DET_WD}	Watch Dog Error Detection time	Time it takes to detect if LC oscillator is out of frequency-range		500	1000	µs
THD_{TX}	Harmonic content of TX signal				-30	dB

5.4 Analog Output

Figure 9:
Analog Output

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OP	Output common mode operating point		48	50	52	% of VCC
OP_{DIFF}	OP difference between channels				2.5	% of VCC
CM_{TH}	OP comparator threshold, triggers SM8 if exceeded	Comparison of differential output common mode voltage against 50% of VCC	±100		±500	mV
OSTD	OP temperature drift	Guaranteed by design	-1		1	%
V_{OFFSET_RX}	Offset of differential output signal		-30		30	mV
OPN(1)	Output noise	10 kHz bandwidth; max AGC gain factor SC_filter enabled		1.5	1.9	mVrms
		10 kHz bandwidth; max AGC gain factor SC_filter disabled		1.9	2.4	mVrms
		Unlimited bandwidth; max AGC gain factor SC_filter enabled		3.6	5	mVrms
		Unlimited bandwidth; max AGC gain factor SC_filter disabled		8.5	11	mVrms
IOUT	Output operating current capability	Consists of static current (incl. external pull-up) and dynamic current for capacitive load	3.5			mA
$IOUT_{SCVCC}$	Output short circuit current to VCC	Output pins (SIN+, SIN-, COS+, COS-) forced to VCC	5	15	25	mA
$IOUT_{SCGND}$	Output short circuit current to GND	Output pins (SIN+, SIN-, COS+, COS-) forced to GND	5	15	25	mA
VOUT(2)	Output voltage range	Output pins (SIN+, SIN-, COS+, COS-) to GND	5		95	% of VCC
$IOUT_{HIGH-Z}$(3)	Output leakage current in high-Z	VCC = 4.05 V, R_{PU} = 4 k, VOUT = 96% of VCC (SIN+, SIN-, COS+, COS-)			40	µA
$VOUT_{CLAMPL}$	Output level clamping low (in I²C mode or PWM safe mode)	3 mA sinking at output pins (SIN+, SIN-, COS+, COS-)			10	% of VCC

(1) Guaranteed by design

(2) The parameter VOUT specifies the general possible output voltage range under the assumption, that the ECU is detecting a voltage level out of this range as a failureband. The final amplitude of the output voltage signal depends only on the RX input signal and the AGC gain factor and should fall into this specified range.

(3) The parameter $I_{OUTHIGH-Z}$ specifies the maximum output leakage current at the output pin in high-Z configuration to fulfill the 96% of VCC level, assuming minimum VCC and minimum external pull-up. In the end application, the output level clamping high depends on the external pull-up resistor (R_{PU}), which must be connected between each output pin and the VCC level.

The voltages V_{SIN+}, V_{SIN-}, V_{COS+} and V_{COS-} are measured from the pins SIN+, SIN-, COS+ and COS- to GND. OP refers to OP_{SIN} and OP_{COS}.

$$OP_{SIN} = \frac{V_{SIN+} + V_{SIN-}}{2} \approx 2.5\ \mathrm{V}$$

$$OP_{COS} = \frac{V_{COS+} + V_{COS-}}{2} \approx 2.5\ \mathrm{V}$$

$$OP_{SIN\%} = \frac{OP_{SIN}}{VCC} * 100 \approx 50\ \%\ \mathrm{of\ VCC}$$

$$OP_{COS\%} = \frac{OP_{COS}}{VCC} * 100 \approx 50\ \%\ \mathrm{of\ VCC}$$

$$OP_{SIN} \neq OP_{COS}$$

$$OP_{SIN\%} \neq OP_{COS\%}$$

$$\frac{|OP_{SIN} - OP_{COS}|}{VCC} * 100 < OP_{DIFF}$$

5.5 Power Management

Figure 10:
Power Management

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCC_{OVTH}	VCC overvoltage threshold high	Please refer to Figure 12	5.65	5.8	5.95	V
VCC_{OVTL}	VCC overvoltage threshold low	Please refer to Figure 12	5.5	5.65	5.8	V
VCC_{OVH}	VCC overvoltage hysteresis	Please refer to Figure 12	100	150	200	mV
$t_{VCCOVDT}$	VCC overvoltage detection time	Time from VCC exceeding VCC_{OVTH} to detection asserts Please refer to Figure 12		250	500	µs
$t_{VCCOVRT}$	VCC overvoltage recovery time	Time from VCC falls below VCC_{OVTL} (recovers to VCC) to normal operation Sin/Cos Output signal Please refer to Figure 12		500	1000	µs
VCC_{UVTH}	VCC undervoltage threshold high	Please refer to Figure 12	4.2	4.35	4.5	V
VCC_{UVTL}	VCC undervoltage threshold low	Please refer to Figure 12	4.05	4.2	4.35	V
VCC_{UVH}	VCC undervoltage hysteresis	Please refer to Figure 12	100	150	200	mV
$t_{VCCUVDT}$	VCC undervoltage detection time	Time from VCC falls below VCC_{UVTL} to detection asserts Please refer to Figure 12		250	500	µs
$t_{VCCUVRT}$	VCC undervoltage recovery time	Time from VCC exceeds VCC_{UVTH} (recovers to VCC) to normal operation Sin/Cos Output signal Please refer to Figure 12		500	1000	µs
$VDD3V3_{OVTH}$	VDD3V3 overvoltage threshold high		3.46	3.53	3.60	V
$VDD3V3_{OVTL}$	VDD3V3 overvoltage threshold low		3.34	3.41	3.48	V
$VDD3V3_{OVH}$	VDD3V3 overvoltage hysteresis		30	50	70	mV
$t_{VDD3V3OVDT}$	VDD3V3 overvoltage detection time	Time from VCC exceeds $VDD3V3_{OVTH}$ to detection asserts		250	500	µs
$t_{VDD3V3OVRT}$	VDD3V3 overvoltage recovery time	Time from VCC falls below $VDD3V3_{OVTL}$ (recovers to VDD3V3) to normal operation Sin/Cos Output signal		500	1000	µs
$VDD3V3_{UVTH}$	VDD3V3 undervoltage threshold high		3.09	3.16	3.23	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VDD3V3_{UVTL}$	VDD3V3 undervoltage threshold low		3	3.07	3.14	V
$VDD3V3_{UVH}$	VDD3V3 undervoltage hysteresis		30	50	70	mV
$t_{VDD3V3UVDT}$	VDD3V3 undervoltage detection time	Time from VCC falls below $VDD3V3_{UVTL}$ to detection asserts		250	500	µs
$t_{VDD3V3UVRT}$	VDD3V3 undervoltage recovery time	Time from VCC exceeds $VDD3V3_{UVTH}$ (recovers to VDD3V3) to normal operation Sin/Cos Output signal		500	1000	µs
V_{LDO}	Internally regulated Voltage	VDD3V3 must not be loaded by any external DC current	3.23	3.3	3.34	V
f_{RC}	RC oscillator frequency		7.3	8	8.7	MHz

5.6 Off-Chip Components

Figure 11:
Off-Chip Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{VDD3V3}	Stabilization cap on VDD3V3		80	220	1100	nF
C_{VCC} (2)	Stabilization cap on VCC		80	100		nF
C_{OUT} (1)	Capacitive load on analog output pins	Applicable for output pins (SIN+, SIN-, COS+, COS-)	2.2	4.7	47	nF
L_{TX}	TX coil inductance		1		20	µH
G_{TX}	TX - LC tank AC conductance		0.05		1.5	mS
$C_{LC\text{-}TANK}$	LC tank capacitance	Overall capacitance of 2 series caps	200	600	3000	pF
Q_{TX}	TX coil quality factor		8	20	40	
L_{RX}	RX coil inductance				4	µH
$C_{RX\_parasitic}$	RX coil parasitic capacitance	Differential between input pins RXSA – RXSB and RXCA – RXCB			20	pF
$R_{RX\_parasitic}$	RX coil parasitic resistor				20	Ω
R_{PU} (1)	Pull-up resistors on analog output pins	Applicable for output pins (SIN+, SIN-, COS+, COS-)	4		10	kΩ

(1) Due to the specified output capacitor and pull-up resistor range, full I^2C specification compliance is not guaranteed.
(2) There is no max limit specified, as a higher cap value always leads to better stabilization behavior, but with increasing cap value, a longer startup time must be taken into account. After reaching the internal POR level (~2.8 V), the outputs remain per default in high-Z configuration for 3 ms. If the nominal VCC level is reached within this 3 ms, the outputs are already settled. If the startup takes longer than 3 ms, the output signals will provide immediately the SIN/COS signal according to the RX input signal multiplied with the gain factor. With active AGC regulation, where the thresholds are ratiometric to VCC, a regulation can still occur, as long as the final VCC level is not reached.

Information

All specified tolerances for external components need to be assured over the whole operation conditions range and also over lifetime.

6 Functional Description

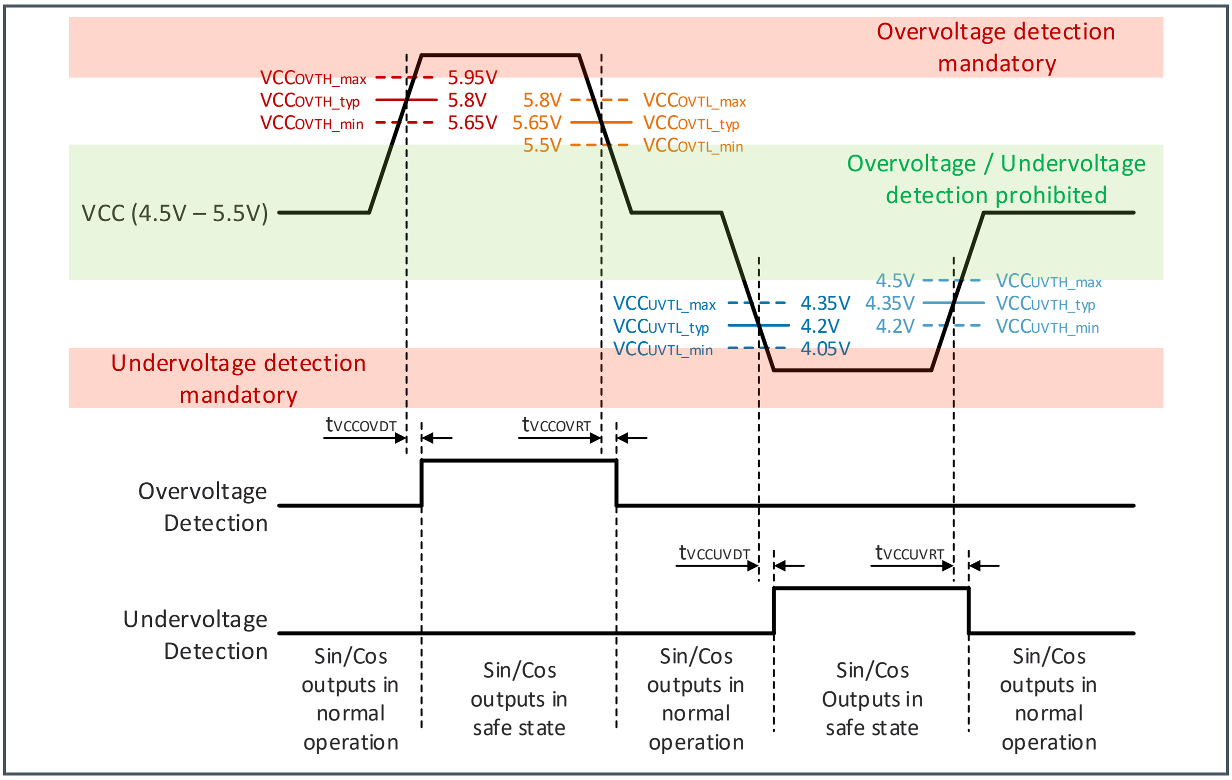
The AS5715A/AS5715R is an inductive-based rotary or linear position sensor using CMOS technology.

6.1 Power Supply

6.1.1 5 V VCC Supply

The device has an integrated overvoltage and undervoltage detection. Figure 12 describes the transition behavior between overvoltage, undervoltage and operational mode condition. An undefined zone is not possible, the device is either in operational mode or in safe mode.

Figure 12:
Reset Thresholds for 5 V VCC Supply



The internal LDO block regulates the 5 V supply voltage (VCC) down to a 3.3 V level (V_{LDO}).

6.2 Oscillator

The AS5715A/AS5715R device and an external LC-tank form an LC-oscillator. The LC-tank consists of the components L_{TX}, C_{LC1} and C_{LC2}. The minimum and maximum specified range of L_{TX} and $C_{LC\text{-}TANK}$ must not be exeeded. Furtermore the parasitic components of L_{TX} and $C_{LC\text{-}TANK}$ must be within the specified range.

Figure 13:
TX Resonator Signal

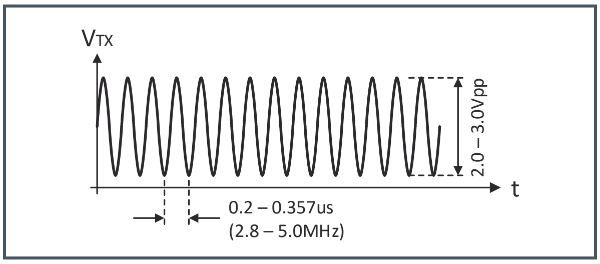
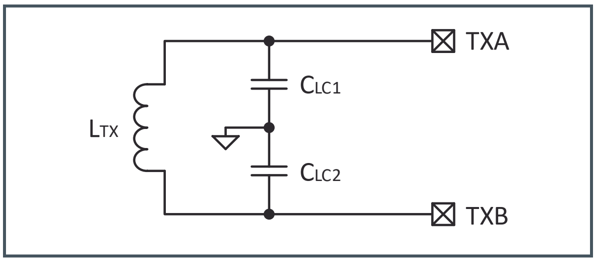


Figure 14:
LC-Tank



Equation 1:

$$C_{LC-TANK} = \frac{C_{LC1} * C_{LC2}}{C_{LC1} + C_{LC2}}$$

Equation 2:

$$f_{TX} = \frac{1}{2 * \pi * \sqrt{L_{TX} * C_{LC-TANK}}}$$

The oscillation frequency of the LC-oscillator is f_{TX} and depends on the LC-tank. Equation 1 and Equation 2 show how to calculate f_{TX}. Note that f_{TX} has to be within the specified range.

6.3 Automatic Gain Control (AGC)

By default, the OTP register *AGC_disable* is set to “0”, therfore the internal AGC algorithm is active and sets the gain for the two AM moduleted RX signals (SIN and COS) as described in Figure 15. Depending on the coil system the AM modulated RX signal may have a high initial offset coming from the coil system. This offsets may result in frequent gain changes over an electrical 360 deg rotation. EMC events that change voltages on the outputs may change the gain and may cause that the device does permanently change it’s currently used gain until the next power on reset.

Alternativly *AGC_disable* can be set to “1”. Then the device permanently operates with the gain selected by the bits *AGC_gain_factor <6:0>*.

The startup procedure of the AGC is described in Figure 15. This startup procedure is executed each time after the device is powered on.

dis_AGC_boost

When the *dis_AGC_boost* bit is “0” then the device does increase the gain until one of the differential outputs (SIN or COS) does reach a positive or negative voltage of $V_{AGC\_REG\_H}/2$ and then does additionaly increase the gain by 4 steps. The maximum possible gain is 109 steps.

dis_AGC_3dBred

When the *dis_AGC_3dBred* bit is “0” then gain is reduced by 18 steps. The purpose of this reduction is that the gain does not change when the target is rotated after the startup procedure, assuming that the differential output signals have no offset and that the distance between the coil sytem and the target stays constant. Without this gain reduction the gain would change after the completion of the startup procedure when the target is rotated and when the target position before the startup is not 0, 90, 180 or 270 degree. The minimum possible gain is 0 steps.

gain_freeze

When the gain freeze bit is “0” then the device does operate in fixed gain operation after the startup procedure. The gain will not change until the next startup.

Normal AGC algorithm regulation

The normal AGC algoritm regulation is described in Figure 16 and Figure 17. The logic gates decide by how many counts the gain will be increased or decreased. A logic “1” at the outputs of the gates causes a gain increase or decrease. A logic “0” at the outputs does not cause any gain change. The gain always changes for both channels together. The inputs of the gates are connected to comparators that compare the absolute value of the differential SIN and COS output signals to four different comperator levels. This comperator levels are derived from $V_{AGC\_LIMIT\_L}$, $V_{AGC\_REG\_L}$, $V_{AGC\_REG\_H}$ and $V_{AGC\_LIMIT\_H}$. The regulation mode and step mode in Figure 16 and Figure 17 is executed periodically with the times t_{REG} and t_{LIMIT}.

Figure 15:
AGC Startup Procedure

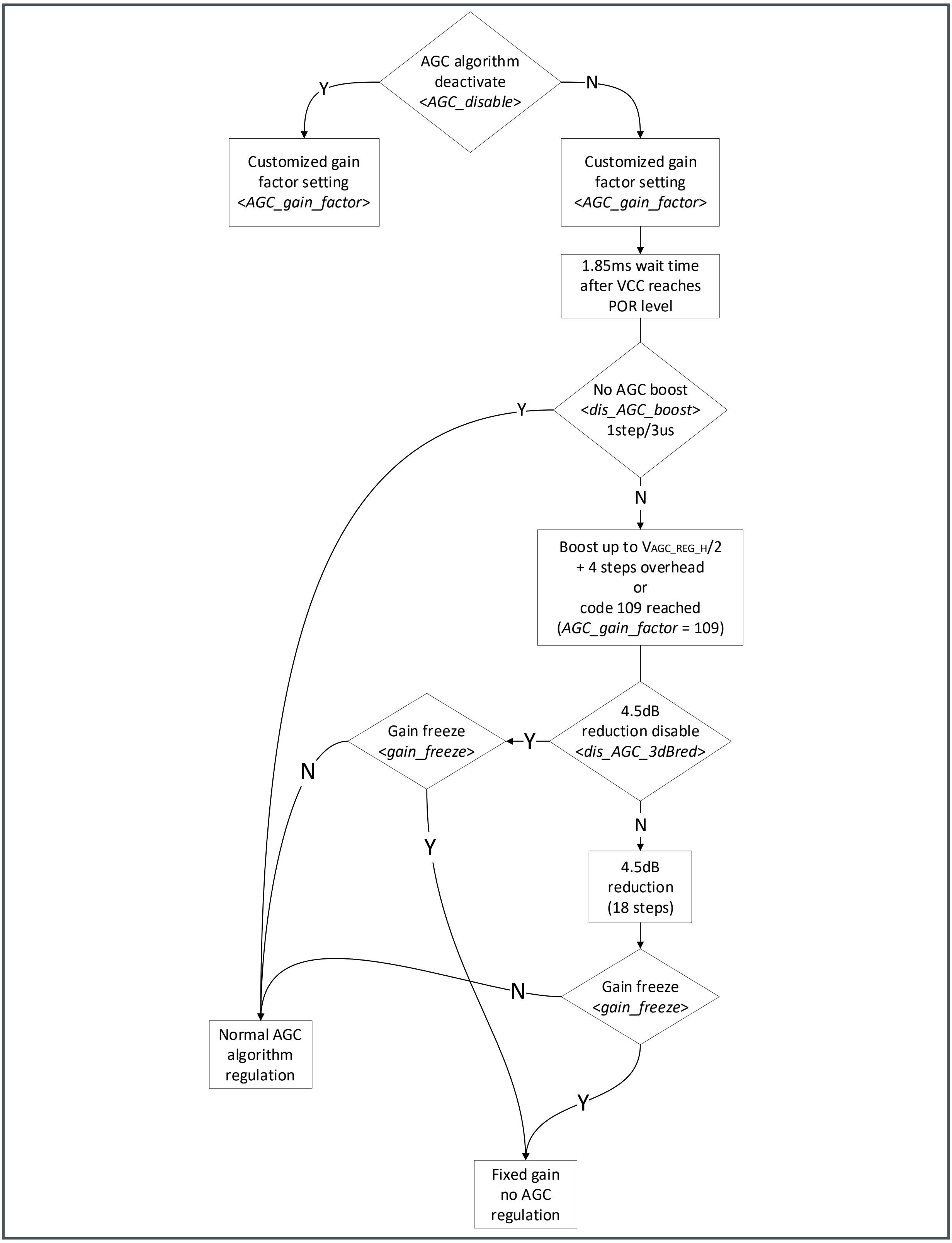


Figure 16:
Digital Implementation of Regulation Mode

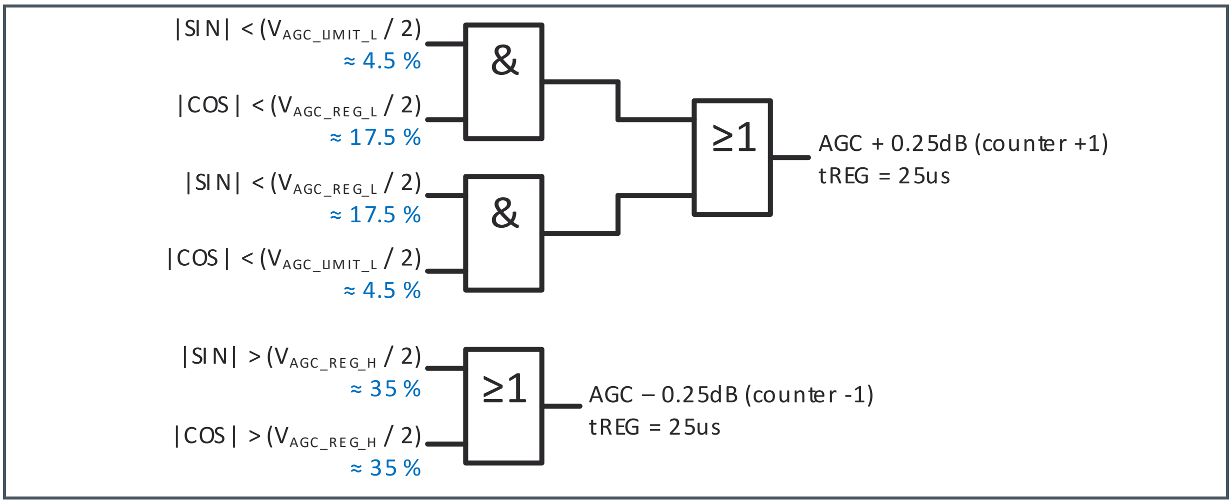


Figure 17:
Digital Implementation of Step Mode

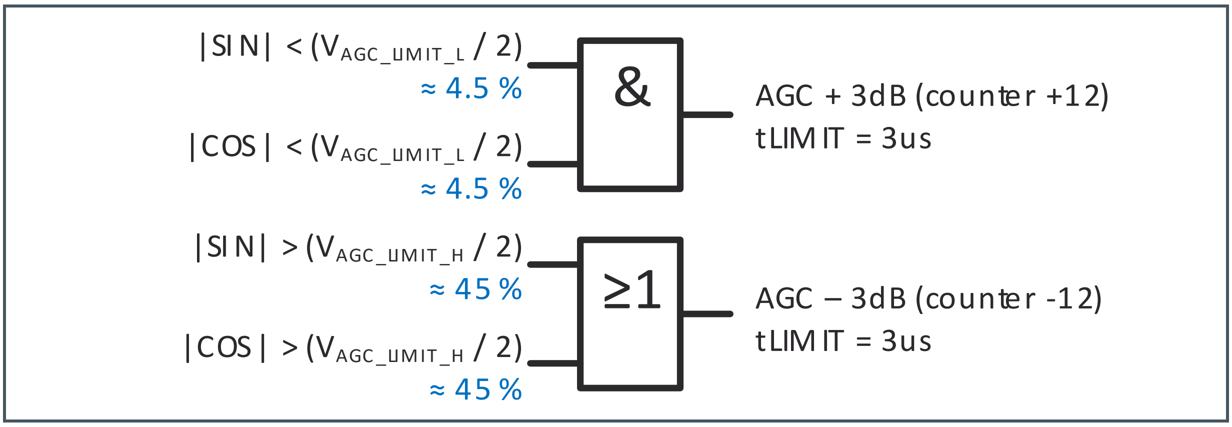
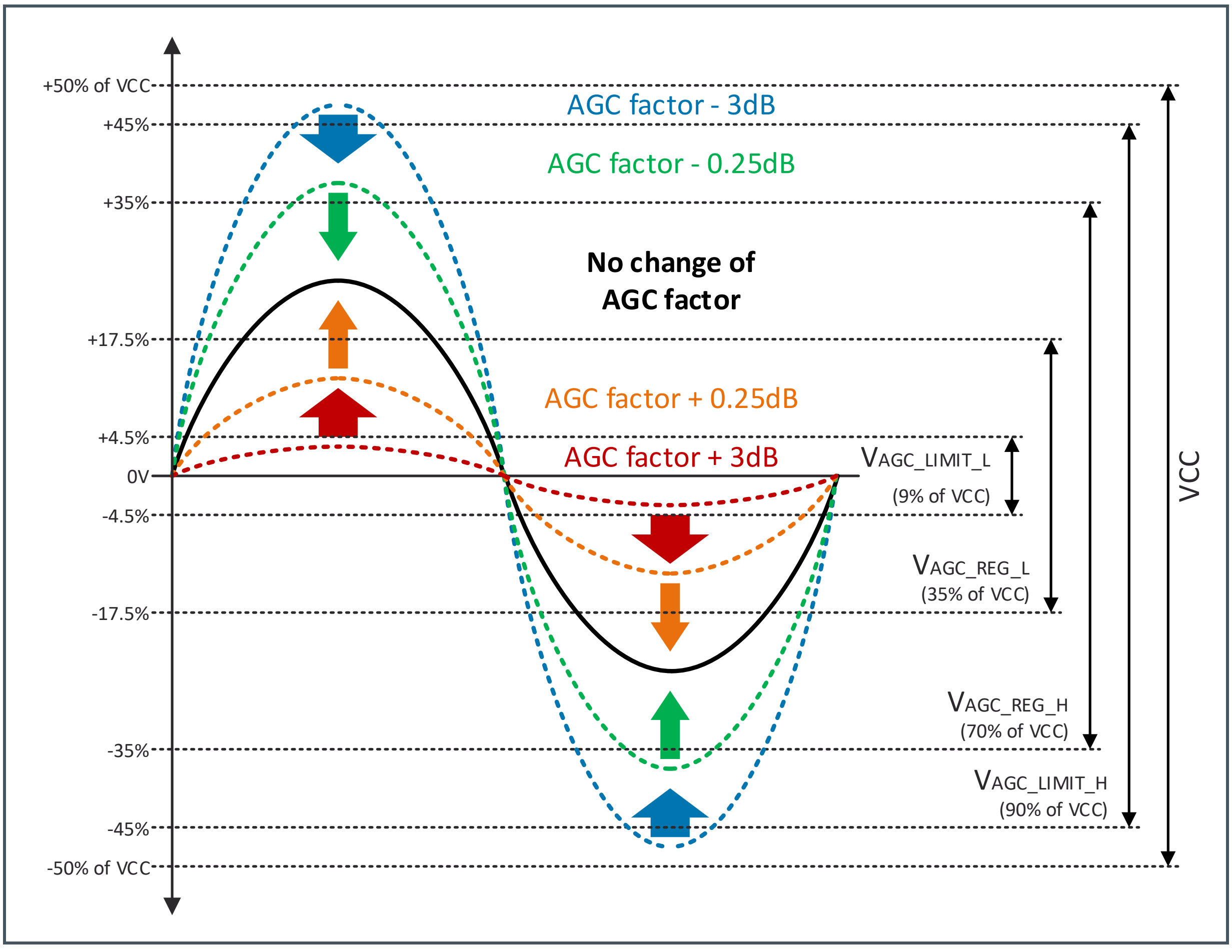


Figure 18:
AGC Regulation and Step Mode



Information

- Whenever the AS5715R moves into safe state (valid for all safety mechanism initiations except the OTP signature check), the AGC gain freezes (assuming that the AGC algorithm is active) for this safe state condition duration.
- As soon as the safe state condition expires and the AS5715R recovers into normal operation mode, the AGC gain unfreezes and it starts regulating with the same gain value as right before entering the safe state condition.
- If the AGC algorithm is disabled, a well defined fixed gain factor must be chosen with respect to the expected maximum RX signal amplitude occurring in certain applications. If the gain factor is set too high, the RX input signal get over-amplified and starts to clip, which may lead into a wrong output signal.

6.4 Output

6.4.1 Output Signals

The differential SIN output signal is the voltage between the pins SIN+ and SIN-.
The differential COS output signal is the voltage between the pins COS+ and COS-.

Figure 19 and Figure 20 show an example of the SIN+ and SIN- signal measured signgle ended (against GND):

- Red signal with peak2peak amplitude of 4.5% of VCC
- Yellow signal with peak2peak amplitude of 17.5% of VCC
- Green signal with peak2peak amplitude of 35% of VCC
- Blue signal with peak2peak amplitude of 45% of VCC

Beside this, the failureband is visible at the low and high side of the output voltage range.

Figure 19 :
SIN+ Single-Ended Output Signal

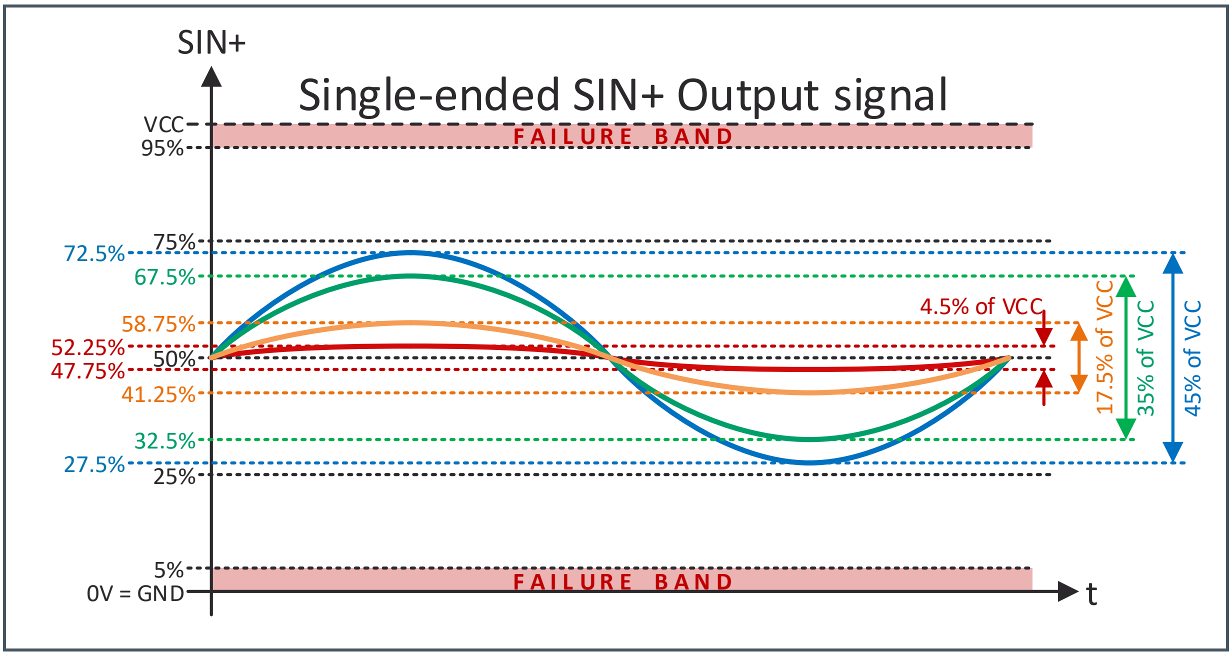
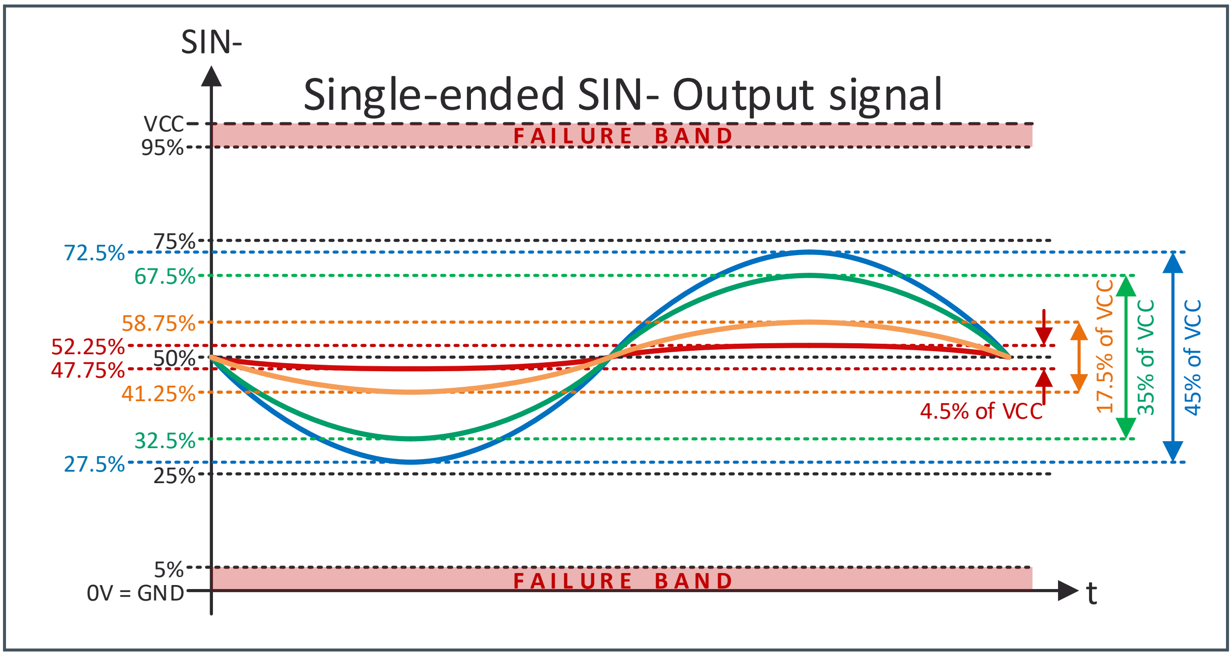


Figure 20 :
SIN- Single-Ended Output Signal

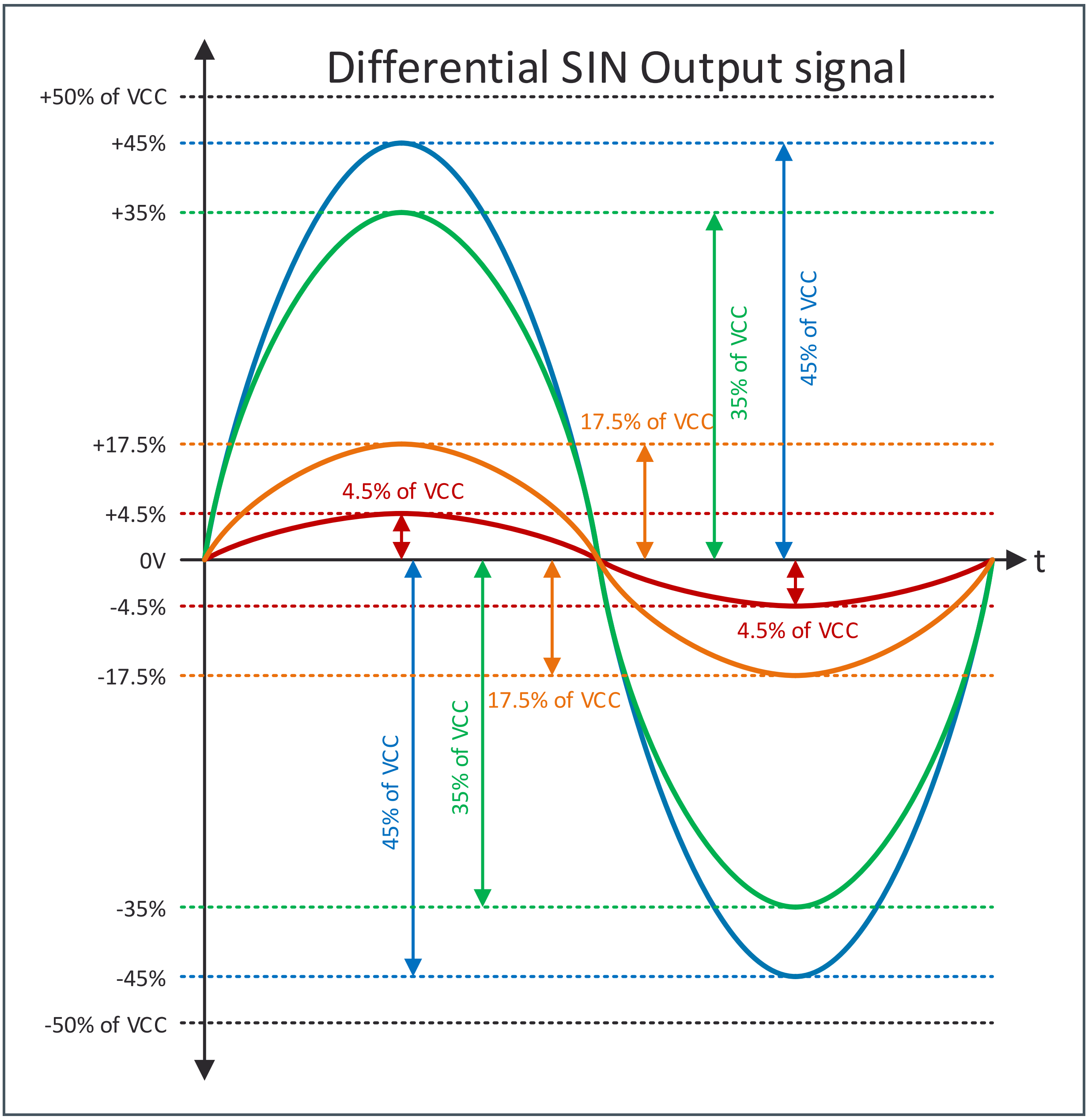


The corresponding differential SIN output signals are drawn in the figure below.

The differential signals are calculated from the single-ended signals (SIN+ minus SIN-):

- Red SIN signal → peak2peak amplitude of 9% of VCC → $V_{AGC\_LIMIT\_L}$ threshold
- Yellow SIN signal → peak2peak amplitude of 35% of VCC → $V_{AGC\_REG\_L}$ threshold
- Green SIN signal → peak2peak amplitude of 70% of VCC → $V_{AGC\_REG\_H}$ threshold
- Blue SIN signal → peak2peak amplitude of 90% of VCC → $V_{AGC\_LIMIT\_H}$ threshold

Figure 21 :
SIN Differential Output Signal



6.5 Diagnostic and Functional Safety

AS5715A/AS5715R can be used in safety critical applications. For this reason, AS5715A/AS5715R is developed as SEooC (Safety Element out of Context) according the ISO26262, with assumed safety goals and assumed ASIL level.

The assumption of use (AoU) and the embedded self-diagnostic, to achieve particular ASIL level in the application, are described in the AS5715A/AS5715R safety manual.

For additional information regarding the ISO26262 flow at ams and the SEooC relevant documents (e.g. FMEDA, safety manual) please contact the technical support of ams.

Figure 22:
Diagnostic Table

Symbol	Safety Mechanism	Recoverable	Safety State
SM1	Watchdog failure Oscillator frequency out of range	Yes, if the frequency f is again within the range of $f_{DET\_WD\_low} < f < f_{DET\_WD\_high}$.	Safe State Definition 1
SM2	Receive coil open detection	Yes, if coil open is resolved	Safe State Definition 2
SM3	VCC overvoltage detection	Yes, if VCC is below the specified threshold. (see Figure 12)	Safe State Definition 3
SM4	VCC undervoltage detection	Yes, if VCC is above the specified threshold (see Figure 12)	Safe State Definition 4
SM5	V_{LDO} overvoltage detection	Yes, if V_{LDO} returns to the specified range	Safe State Definition 5
SM6	V_{LDO} undervoltage detection	Yes, if V_{LDO} returns to the specified range	Safe State Definition 6
SM7	OTP Signature check	No, the device stays in failure band until the OTP content is correct and a power on reset is performed.	Safe State Definition 7
SM8	Output Short circuit detection	Yes, if short is resolved	Safe State Definition 8
SM9	VCC Reverse polarity	Yes, if polarity is correct.	Safe State Definition 9
SM10	Output signal too low	Yes, if output signal amplitude is getting increased	Safe State Definition 10
SM11	Output signal too high	Yes, if output signal amplitude is getting decreased	Safe State Definition 11

Figure 23:
Safe State Definition

Symbol	Safe State Definition	signaling_disable	SIN+	SIN-	COS+	COS-
SSD1	Safe State for SM1	0 1	PWM (0:100) high-Z	high-Z	high-Z	high-Z
SSD2	Safe State for SM2	0 1	PWM (20:80) high-Z	high-Z	high-Z	high-Z
SSD3	Safe State for SM3	0 1	high-Z	high-Z	high-Z	high-Z
SSD4	Safe State for SM4	0 1	PWM (40:60) high-Z	high-Z	high-Z	high-Z
SSD5	Safe State for SM5	0 1	high-Z	high-Z	high-Z	high-Z
SSD6	Safe State for SM6	0 1	PWM (60:40) high-Z	high-Z	high-Z	high-Z
SSD7	Safe State for SM7	0 1	PWM (70:30) high-Z	high-Z	high-Z	high-Z
SSD8	Safe State for SM8	0 1	high-Z	high-Z	high-Z	high-Z
SSD9	Safe State for SM9	0 1	high-Z	high-Z	high-Z	high-Z
SSD10(1)	Safe State for SM10	0 1	PWM (80:20) high-Z	high-Z	high-Z	high-Z
SSD11(1)	Safe State for SM11	0 1	PWM (90:10) high-Z	high-Z	high-Z	high-Z

(1) Enable/disable by customer OTP bit setting

The PWM frequency is 500 Hz. The PWM voltage may not be rectangular, depending on the used pullup resistor and output capacitor.

e.g. PWM (20:80) stands for 20% high level and 80% low level

6.6 I²C Interface and Communication Procedure

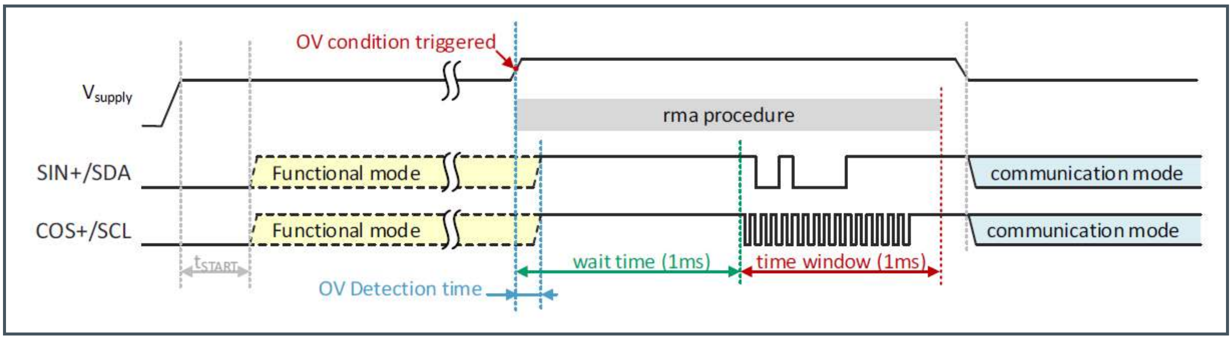
The AS5715R will start up in operational mode after powering up. In operational mode the 4 analog outputs of the device are operational.

The AS5715R features and OTP (One Time Programmable) memory. This memory can be used to programm custom settings. The OTP can be programmed over an I²C interface which is applicable at the pins SIN+/SDA and COS+/SCL. To activate the I²C interface, the so called customer rma procedure is performed. The customer rma procedure allows to switch the analog outputs into I²C mode in order to allow programming over I²C. To switch the outputs back into operational mode without burning the OTP, the pass2funct command can be used.

6.6.1 Customer rma Procedure

1. On the VCC pin, an overvoltage condition must be applied by supplying with a voltage between 5.95 V and 20 V.
2. The OV detection takes ~50 µs followed by a 1 ms wait time. After this, a 1 ms window is open to execute the customer rma procedure.
3. To execute the customer rma procedure it is necessary to apply 2 pulses (= 2 x rising edge) on SIN+/SDA and independent from that, 16 pulses (= 16 x rising edge) on COS+/SCL during the rma window. The pulses must be applied with a frequency <1 MHz.
4. After this, the I²C port is open and the VCC supply voltage must be reduced to the operationg voltage range before I²C communication is possible.

Figure 24:
Customer rma Procedure



6.6.2 pass2funct Command

The pass2funct command is usefull to check the effect of changed memory settings before burning them into the OTP. The pass2funct switches the device from I²C mode into functional mode without the need to perform a power on reset or burning the OTP.

If a register bit gets changed, it is important also to adjust the signature byte as well. Even if a correct signature is written, the signature error is triggered, because the error is latched. To clean the signature error it´s necessary to write dsp_rst before performing a pass2funct command.

The pass2funct is executed when the register **PASS2FUNCT** (address f1h) is written with the value 01010011b (53h). After the pass2funct command, the I²C interface is disabled and the only way to enable again the communication mode is an execution of the customer rma procedure.

6.6.3 Customer Signature Calculation

After the desired bit settings of the customer OTP registers **P2RAM_BYTE_13**, **P2RAM_BYTE_14** and **P2RAM_BYTE_15**, the correct setting of the customer signature bits must be applied into register **P2RAM_BYTE_16**. The OTP of AS5715R uses a BIST technique with Multiple Input Signature Register circuits. To activate this Built-In-Self-Test, a calculation of the signature byte is necessary which has to be stored in the OTP during programming. For calculating the signature byte, the content of the whole memory has to be read out. Out of this information, the following calculation has to be done.

```
@content =($byte0, $byte1, $byte2, $byte3, $byte4, $byte5, $byte6, $byte7, $byte8,
$byte9, $byte10, $byte11, $byte12, $byte13, $byte14, $byte15);

$misr = 0;
for($i=12; $i< 15; $i++) {
$misr_shift = ($misr<<1);
$misr_xor = ($misr_shift ^ $content[$i]) & 0xFF;
$misr_msb = $misr/(128);
if ($misr_msb eq 0) {
$misr = $misr_xor;
}
else
{
$misr = ($misr_xor ^ 29) & 0xFF;
}
```

6.6.4 Burning Procedure for Customer OTP Section

Before to activate the burning procedure of the customer OTP section, the customer has to write first the unlock command 01h to the register **P2RAM_CONTROL** (address 03h), otherwise the burning function is locked. Now the OTP is ready for burning.

The BURN command has to be triggered by writing 08h to the register **P2RAM_CONTROL**. The status of the burning procedure can be seen by polling the BURN bit. During burn operation it stays high and get released to 0 after the burning procedure has finished. The content of the register **P2RAM_CONTROL** will be 09h during burning and 01h when burning procedure is finished.

To check the quality of the burned fuses, right after the burning process, the whole customer OTP section (register **P2RAM_BYTE_13** up to register **P2RAM_BYTE_16**) should be set to 00h. Using the LOAD operation by writing 04h to the register **P2RAM_CONTROL** will load the content of the burned fuses into the customer OTP section and the correct content can be checked.

The same routine has to be done with the GLOAD command!
Set the whole customer OTP section (register **P2RAM_BYTE_13** up to register **P2RAM_BYTE_16**) to 00h again. Use the GLOAD + LOAD operation by writing 44h to the register **P2RAM_CONTROL** and this will load again the content of the burned fuses into the customer OTP section and check, if the content is correct.

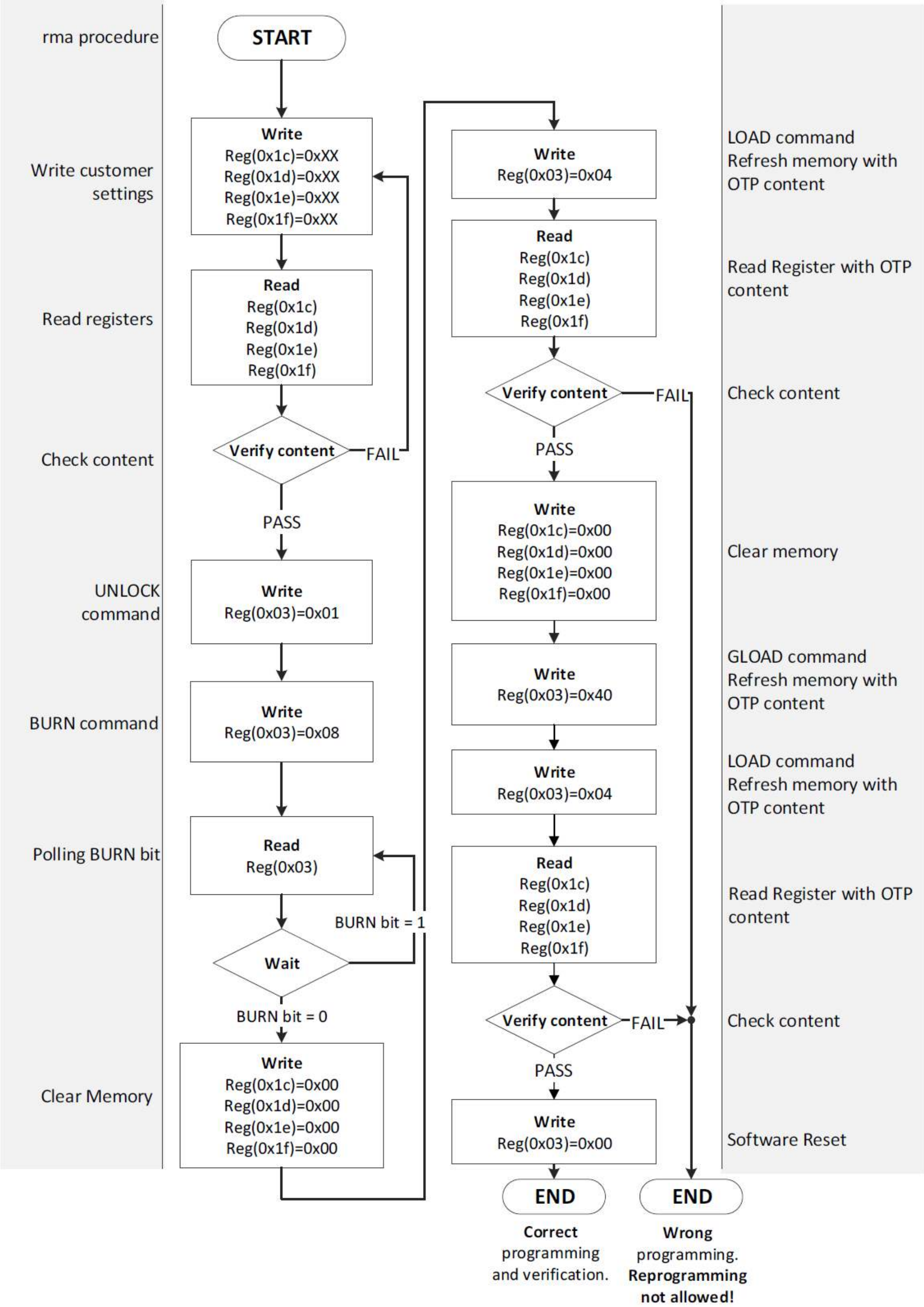
Information

GLOAD Test:

Restricted to temperature range: 25 °C ± 20 °C
Right after the programming procedure (max. 1 hour with same conditions 25 °C ± 20 °C), same VCC voltage. The GLOAD test is only for the verification of the burned OTP fuses during the programming sequence. A use of the GLOAD in other cases is not allowed.

6.6.5 Programming Flowchart

Figure 25:
Programming Flowchart



7 Register Description

7.1 Register Overview

Figure 26:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
OTP Registers									
1h	***ERROR***	*<7> VLDO_under voltage*	*<6> VLDO_ov ervoltage*	*<5> VCC_und ervoltage*	*<4> VCC_ove rvoltage*	*<3> coil_sc_br eak*	*<2> cust_sign ature_err*	*<1> ams_signa ture_err*	*<0> watchdo g_failure*
2h	***RESET***								*dsp_rst*
3h	***P2RAM _CONT ROL***					*<3> BURN bit*			
10h	**CHIPID0**	*<7:0> Chip_ID*							
11h	**CHIPID1**	*<15:8> Chip_ID*							
12h	**CHIPID2**	*<23:16> Chip_ID*							
1ch	**P2RAM _BYTE_ 13**	*<7> cust_ spare1*	*<6> short_n_ dis*	*<5> short_p_ dis*	*<4> AGC_ cmp_ high_thr*	*<3> gain_ freeze*	*<2> dis_ AGC_ 3dBred*	*<1> dis_AGC_ boost*	*<0> en_out_ startup*
1dh	**P2RAM _BYTE_ 14**	*<7> signaling_dis able*	*<6> gain_ check_ disable*	*<5> LC_wide_ range*	*<4> vdd3v3_ ov_ disable*	*<3> vdd3v3_ uv_ disable*	*<2> vcc_ov_ disable*	*<1> vcc_uv_ disable*	*<0> SC_filter_ disable*
1eh	**P2RAM _BYTE_ 15**	*<7> AGC_ disable*	*<6:0> AGC_gain_factor*						
1fh	**P2RAM _BYTE_ 16**	*<7:0> cust_signature*							
f2h	**AGC_V ALUE**	*<7> gain_error*	*<6:0> agc_cnt_value*						

7.2 Detailed Register Description

7.2.1 P2RAM_BYTE_13 Register (Address 1ch)

Addr: 1ch		P2RAM_BYTE_13		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	*cust_spare1*	b0	RW	Customer spare bit
6	*short_n_dis*	b0	RW	Disables the output short circuit monitoring to GND 0 : Active 1 : Inactive
5	*short_p_dis*	b0	RW	Disables the output short circuit monitoring to VCC 0 : Active 1 : Inactive
4	*AGC_cmp_high_thr*	b0	RW	Sets all AGC threshold to a 30% higher value 0 : Normal AGC comparator thresholds 1 : 30% higher AGC comparator thresholds
3	*gain_freeze*	b0	RW	Allows to freeze the AGC gain factor after the boost to the $V_{AGC\_REG\_H}$ threshold (depends on 3dB reduction setting) 0 : No gain freeze 1 : Gain freeze after boost (if *dis_AGC_3dBred* is set) or after boost + 3dB reduction (if *dis_AGC_3dBred* is not set)
2	*dis_AGC_3dBred*	b0	RW	Disables the AGC gain factor reduction of 3dB after the boost to the $V_{AGC\_REG\_H}$ threshold 0 : 3dB gain reduction 1 : No gain reduction
1	*dis_AGC_boost*	b0	RW	Disables the automatic AGC incrementing (boost) after startup up the 70% threshold or code 109 0 : AGC boost enabled 1 : AGC boost disabled
0	*en_out_startup*	b0	RW	Enables the analog SIN/COS outputs also during startup phase 0 : SIN/COS outputs are disabled during startup phase 1 : SIN/COS outputs are enabled during startup phase

7.2.2 P2RAM_BYTE_14 Register (Address 1dh)

Addr: 1dh		P2RAM_BYTE_14		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	*signaling_disable*	b0	RW	Disables the signaling of failure type on analog outputs 0 : Failure signaling on outputs enabled 1 : Failure signaling on outputs disabled
6	*gain_check_disable*	b0	RW	Disables the output signal amplitude monitoring (signal too high/too low) 0 : Output signal amplitude monitoring enabled 1 : Output signal amplitude monitoring disabled
5	*LC_wide_range*	b0	RW	Set a wider range for LC frequency check in watchdog 0 : LC check counter range (26/55) 1 : LC check counter range (26/75)
4	*vdd3v3_ov_disable*	b0	RW	Disables the 3.3 V regulator overvoltage flag 0 : 3.3 V OV monitoring enabled 1 : 3.3 V OV monitoring disabled
3	*vdd3v3_uv_disable*	b0	RW	Disables the 3.3 V regulator undervoltage flag 0 : 3.3 V UV monitoring enabled 1 : 3.3 V UV monitoring disabled
2	*vcc_ov_disable*	b0	RW	Disables the VCC overvoltage flag 0 : VCC OV monitoring enabled 1 : VCC OV monitoring disabled
1	*vcc_uv_disable*	b0	RW	Disables the VCC undervoltage flag 0 : VCC UV monitoring enabled 1 : VCC UV monitoring disabled
0	*SC_filter_disable*	b0	RW	Disables the SC filter in RX chain 0 : SC filter is enabled 1 : SC filter is disabled

7.2.3 P2RAM_BYTE_15 Register (Address 1eh)

Addr: 1eh		P2RAM_BYTE_15		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	*AGC_disable*	b0	RW	Disables the AGC algorithm 0 : AGC algorithm is enabled 1 : AGC algorithm is disabled
6:0	*AGC_gain_factor*	b000 0000	RW	Defines the fixed gain factor if *AGC_disable* = 1 or defines the default gain factor (after startup or reset) if *AGC_disable* = 0 0 : 25dB … 109 : 52.25 dB 110 – 127 : not applicable *AGC_gain_factor_dB = AGC_gain_factor ** AGC_{STEP_REG} *+ 25*

7.2.4 P2RAM_BYTE_16 Register (Address 1fh)

Addr: 1fh		P2RAM_BYTE_16		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	*cust_signature*	b0000 0000	RW	Signature byte for the customer OTP section

7.2.5 AGC_VALUE Register (Address f2h)

Addr: f2h		AGC_VALUE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	*gain_error*	b0	RO	Gain error flag triggered by AGC saturated + too low or too high signal
6:0	*agc_cnt_value*		RO	Read current gain value (for evaluation purposes only)

8 Functional Safety

8.1 Safety Manual

The Safety Manual, available upon request, contains all the necessary information for the system integrator, to integrate AS5715A/AS5715R in a safety related item.

The sensor is supporting the ISO26262 as Safety Element out of Context (SEooC).

The Safety Manual includes the following information:

- Product development lifecycle
- Description of the technical safety concept on system level
- Detailed information of Assumption of Use of the element with respect to its intended use, which includes
  - System Safe State information
  - Fault Tolerant Time Interval
  - Coverage information

As part of the Safety Manual, the Verification and Safety Analysis Report includes following information:

- HW architectural metric results (Single Point Fault Metric)
- Description of verifications based on the ISO26262
- Detailed FMEDA

9 Application Information

9.1 Typical Application Circuits

Figure 27:
Typical Differential Output Application for 5 V VCC Supply System

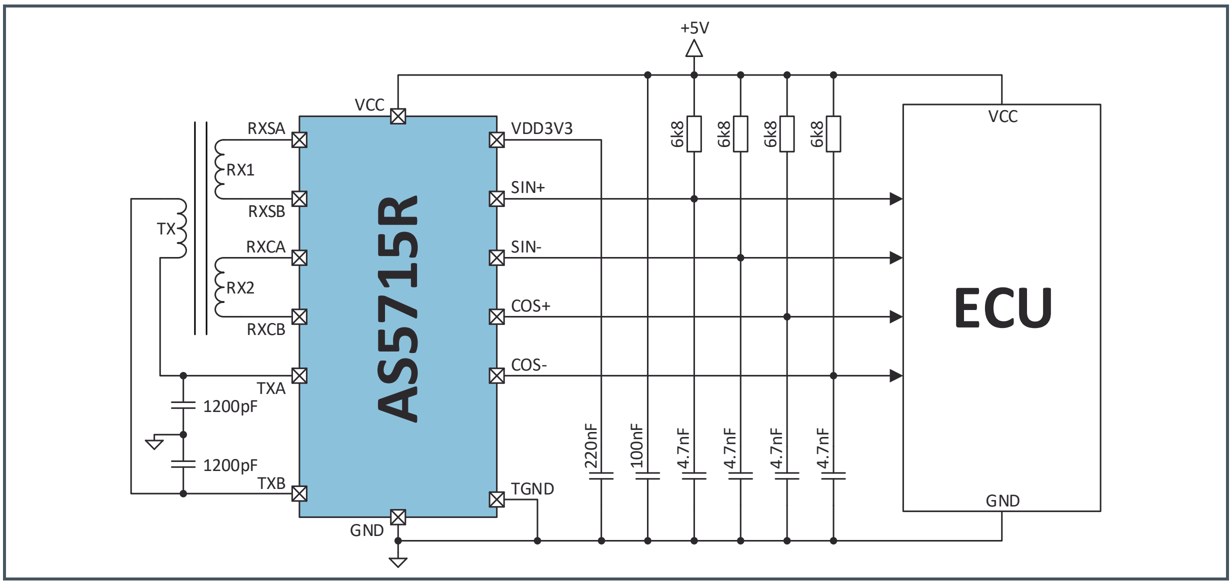
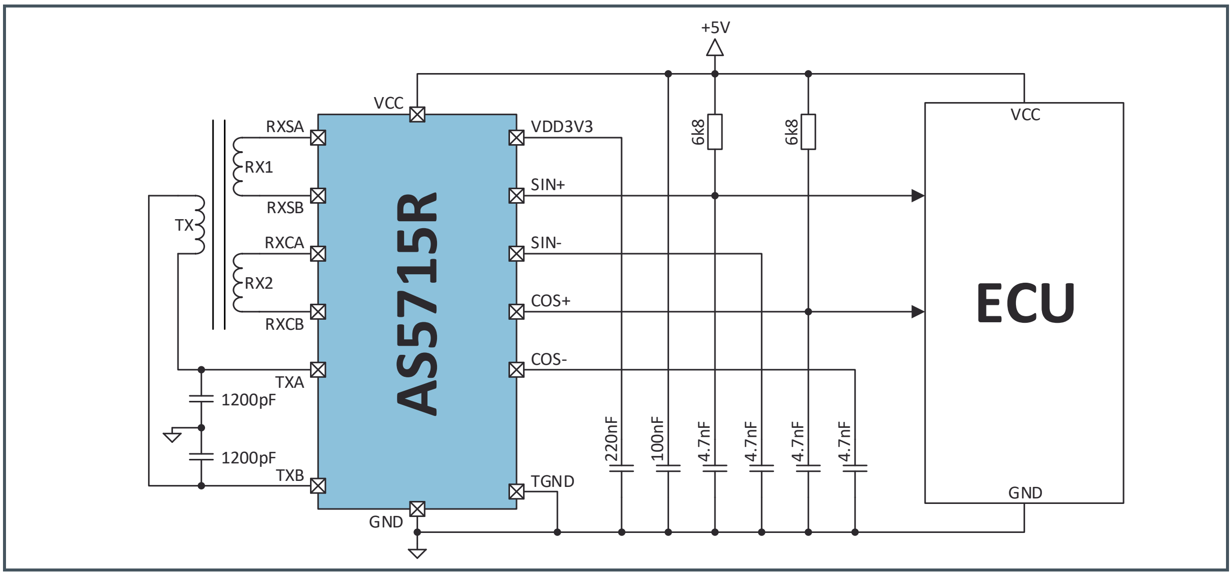


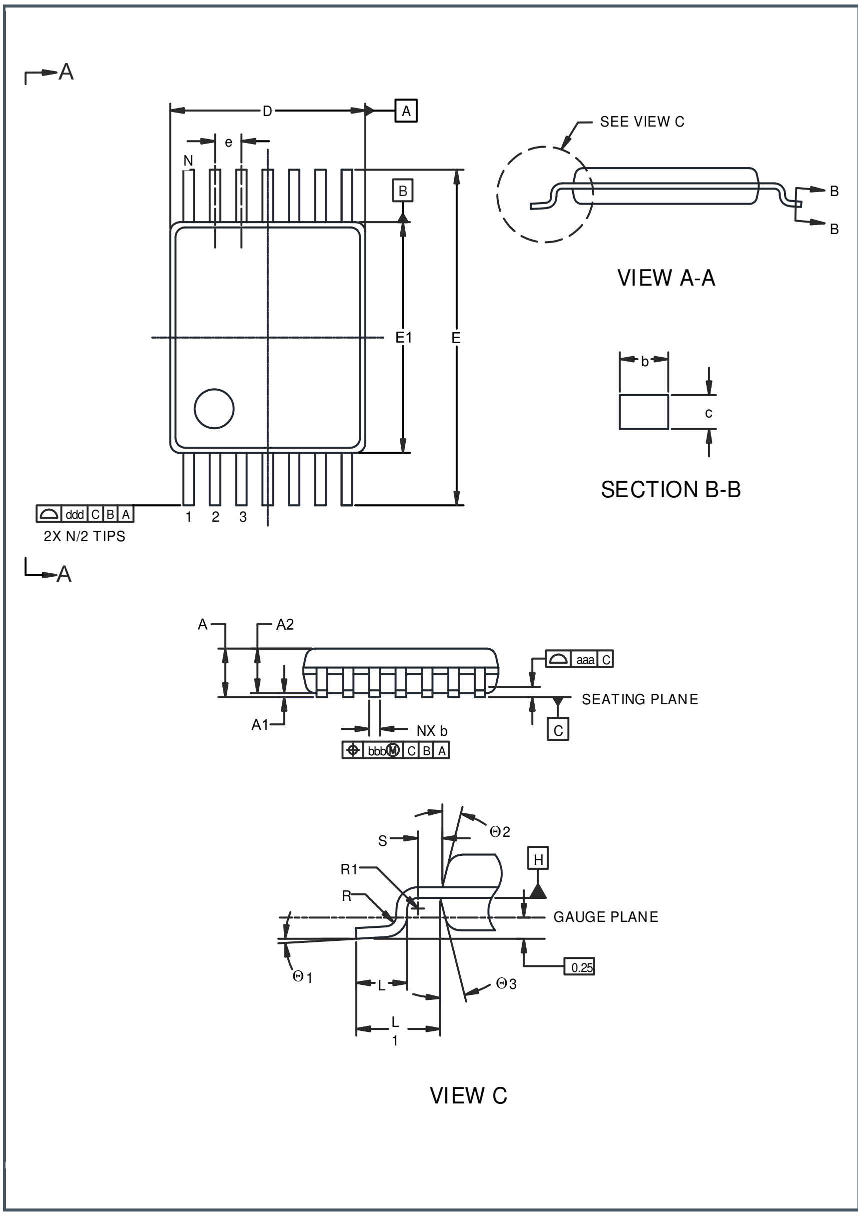
Figure 28:
Typical Single Ended Output Application for 5 V VCC Supply System



(1) The accuracy specifications in this datasheed are valid for the Differential Output Application only

10 Package Drawings & Markings

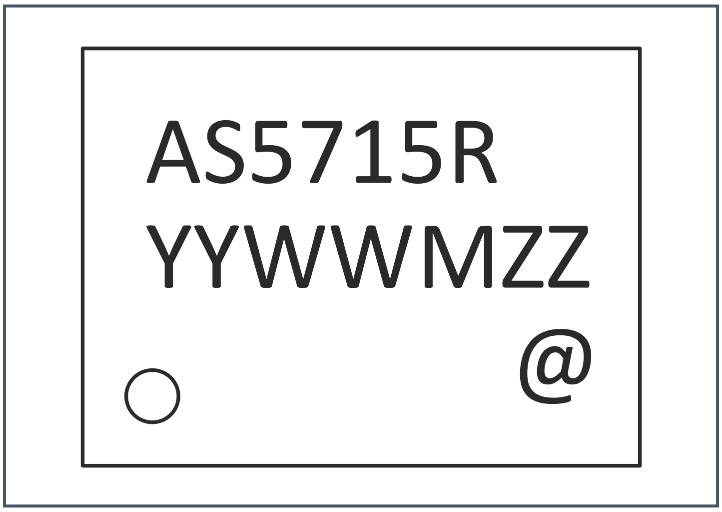
Figure 29:
TSSOP14 Package Outline Drawing



Ref.	Min	Nom	Max
A			1.20
A1	0.05		0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
E		6.40 BSC	
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
R	0.09		
R1	0.09		
S	0.20		
Θ1	0°		8°
Θ2		12 REF	
Θ3		12 REF	
aaa		0.10	
bbb		0.10	
ccc		0.05	
ddd		0.20	
N		14	

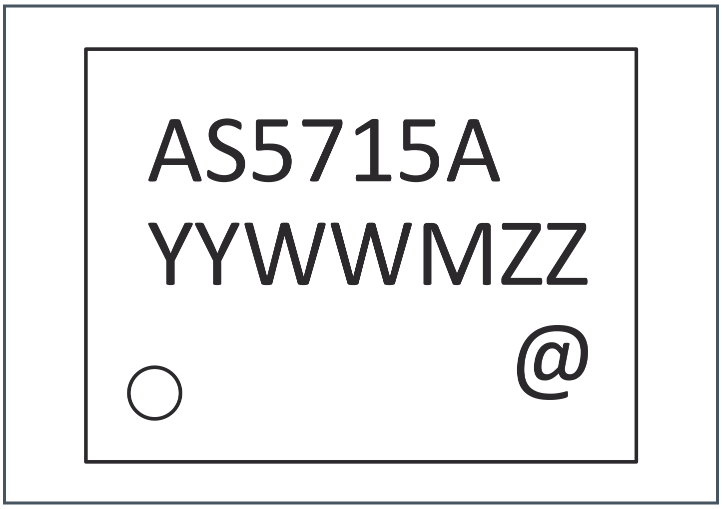
(1) All dimensions are in millimeters. Angles in degrees.
(2) Dimensioning and tolerancing conform to ASME Y14.5-2009.
(3) N is the total number of terminals.

Figure 30:
TSSOP14 Package Marking/Code for AS5715R



YY	Manufacturing Year
WW	Manufacturing Week
M	Assembly Plant Identifier
ZZ	Assembly Traceability Code
@	Sublot Identifier

Figure 31:
TSSOP14 Package Marking/Code for AS5715A



YY	Manufacturing Year
WW	Manufacturing Week
M	Assembly Plant Identifier
ZZ	Assembly Traceability Code
@	Sublot Identifier

11 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v4-00	Page
Changed typical value for the propagation delay	11
Chapter 6.6.4	30
Figure 26	33
Chapter 7.2.5	36

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

12 Legal Information

RoHS Compliant & ams Green Statement

RoHS Compliant: The term RoHS compliant means that ams AG products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories plus additional 4 substance categories (per amendment EU 2015/863), including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, RoHS compliant products are suitable for use in specified lead-free processes.

ams Green (RoHS compliant and no Sb/Br/Cl): ams Green defines that in addition to RoHS compliance, our products are free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material) and do not contain Chlorine (Cl not exceed 0.1% by weight in homogeneous material).

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