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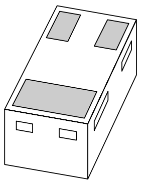


PMZ1000UN

N-channel TrenchMOS standard level FET

Rev. 2 — 17 September 2010 Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Fast switching
- Low conduction losses due to low on-state resistance
- Saves PCB space due to small footprint (90 % smaller than SOT23)
- Suitable for use in compact designs due to low profile (55 % lower than SOT23)

1.3 Applications

- Driver circuits
- Switching in portable appliances

1.4 Quick reference data

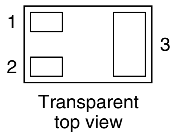
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	-	30	V
I_D	drain current	T_{amb} = 25 °C; V_{GS} = 10 V; see Figure 1	-	-	480	mA
P_{tot}	total power dissipation	T_{amb} = 25 °C; see Figure 2	-	-	350	mW
Static characteristics						
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.2 A; T_j = 25 °C; see Figure 8	-	-	1	Ω

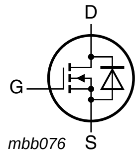
2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	S	source		
3	D	drain		



SOT883 (SC-101)



3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZ1000UN	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883

4. Marking

Table 4. Marking codes

Type number	Marking code
PMZ1000UN	6N

5. Limiting values

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 5. Limiting values

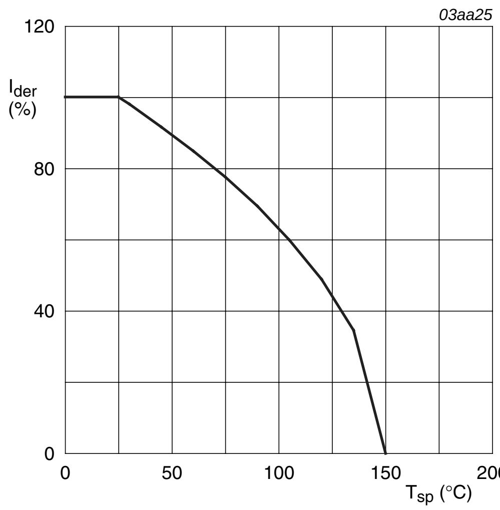
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 150 °C	-	30	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 150 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage		–8	+8	V
I_D	drain current	T_{amb} = 25 °C; V_{GS} = 10 V; see Figure 1	-	480	mA
I_{DM}	peak drain current	T_{amb} = 25 °C; t_p ≤ 10 µs; pulsed	-	1.8	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; see Figure 2	-	350	mW
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–55	+150	°C

Table 5. Limiting values *…continued*

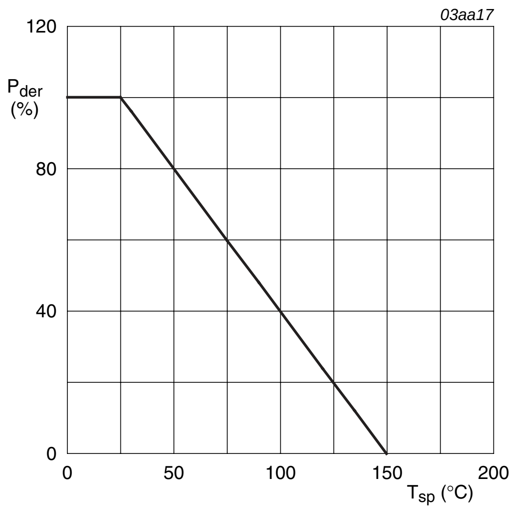
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Source-drain diode					
I_S	source current	T_{amb} = 25 °C	-	480	mA
Electrostatic discharge					
V_{ESD}	electrostatic discharge voltage	HBM; C = 100 pF; R = 1.5 kΩ	-	60	V
		MM; C = 200 pF	-	30	V



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature

6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 3		-	-	50	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	-	-	355	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

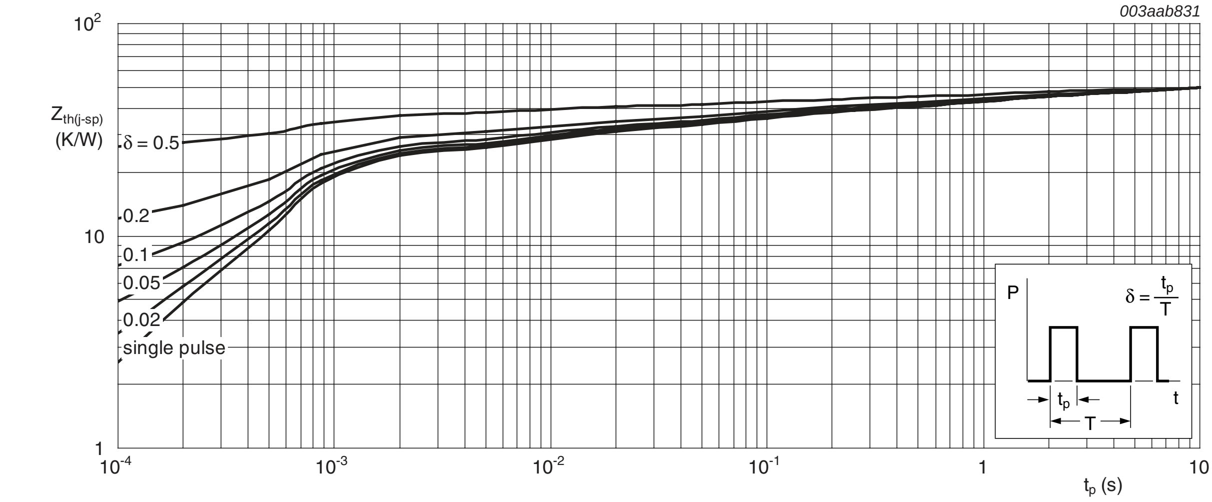


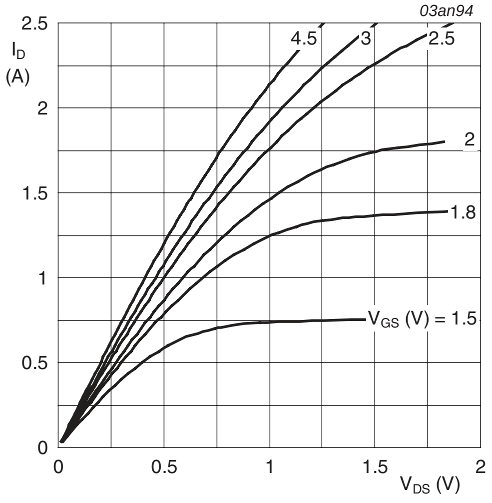
Fig 3. Transient thermal impedance from junction to solder point as a function of pulse duration

7. Characteristics

Table 7. Characteristics

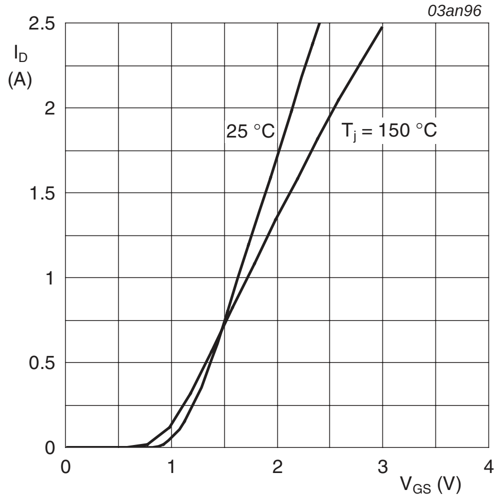
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 10 µA; V_{GS} = 0 V				
		T_j = 25 °C	30	-	-	V
		T_j = −55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 0.25 mA; V_{DS} = V_{GS}; see Figure 6 and 7				
		T_j = 25 °C	0.45	0.7	0.95	V
		T_j = 150 °C	0.25	-	-	V
		T_j = −55 °C	-	-	1.15	V
I_{DSS}	drain leakage current	V_{DS} = 30 V; V_{GS} = 0 V				
		T_j = 25 °C	-	-	1	µA
		T_j = 150 °C	-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = ±8 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 0.2 A; see Figure 8				
		T_j = 25 °C	-	-	1	Ω
		T_j = 150 °C	-	-	1.5	Ω
		V_{GS} = 2.5 V; I_D = 0.1 A; Figure 8	-	-	1.1	Ω
		V_{GS} = 1.8 V; I_D = 0.075 A; Figure 8	-	-	1.4	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 1 A; V_{DS} = 15 V; V_{GS} = 4.5 V; see Figure 9 and 10	-	0.89	-	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.2	-	nC
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; see Figure 11	-	43	-	pF
C_{oss}	output capacitance		-	7.7	-	pF
C_{rss}	reverse transfer capacitance		-	4.8	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 15 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 6 Ω	-	4	-	ns
t_r	rise time		-	7.5	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
t_f	fall time		-	4.5	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 0.3 A; V_{GS} = 0 V; see Figure 11	-	0.76	1.2	V



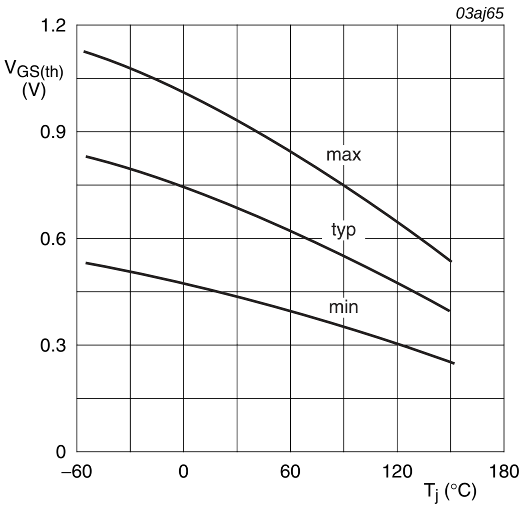
T_j = 25 °C

Fig 4. Output characteristics: drain current as a function of drain-source voltage; typical values



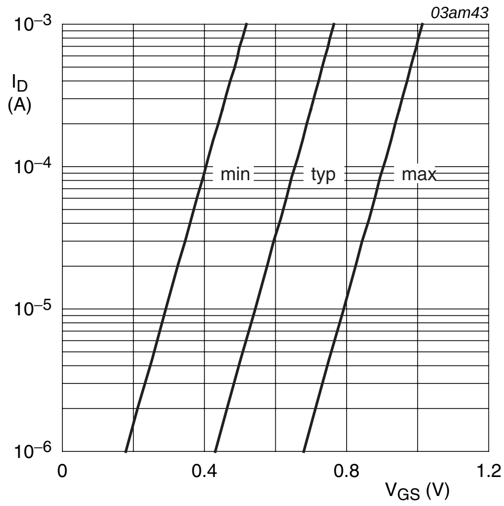
T_j = 25 °C and 150 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 5. Transfer characteristics: drain current as a function of gate-source voltage; typical values



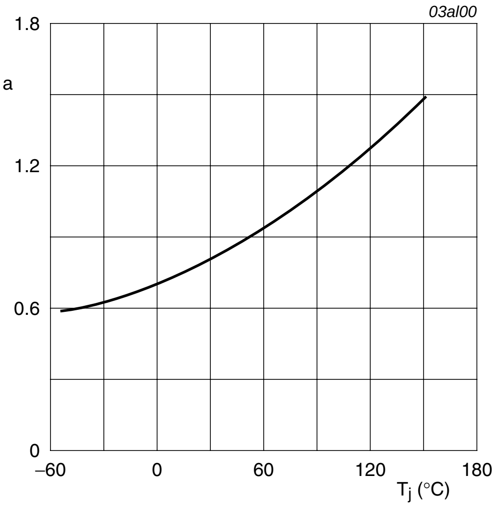
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 6. Gate-source threshold voltage as a function of junction temperature



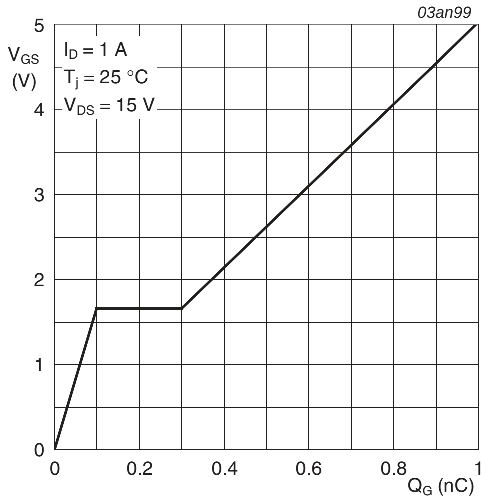
T_j = 25 °C; V_{DS} = 5 V

Fig 7. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance as a function of junction temperature



I_D = 1 A; V_{DS} = 15 V

Fig 9. Gate-source voltage as a function of gate charge; typical values

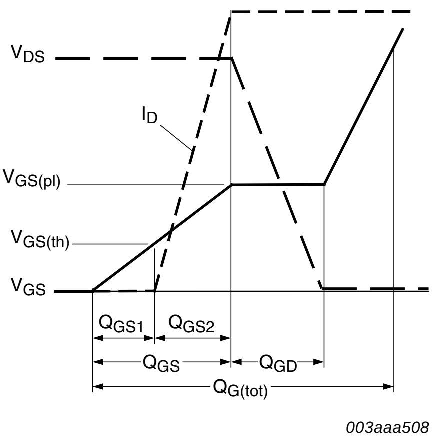
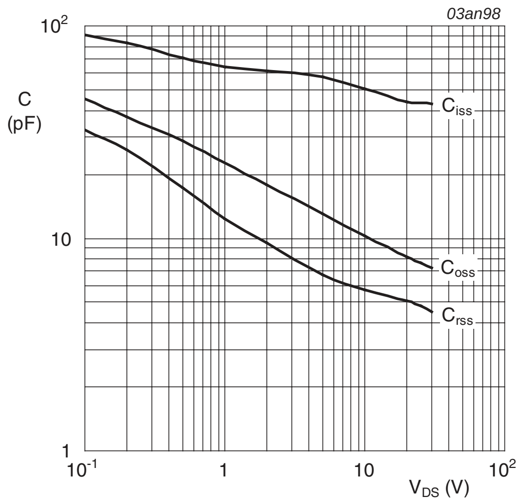
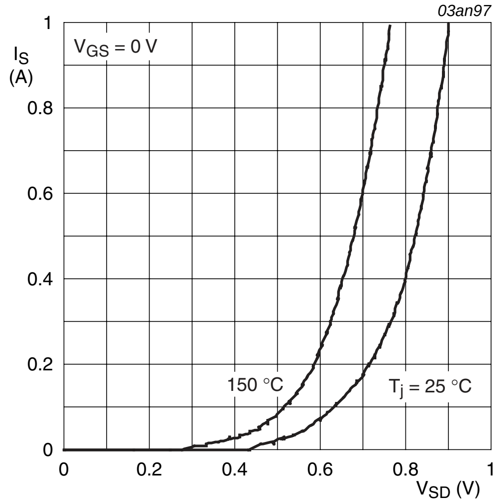


Fig 10. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

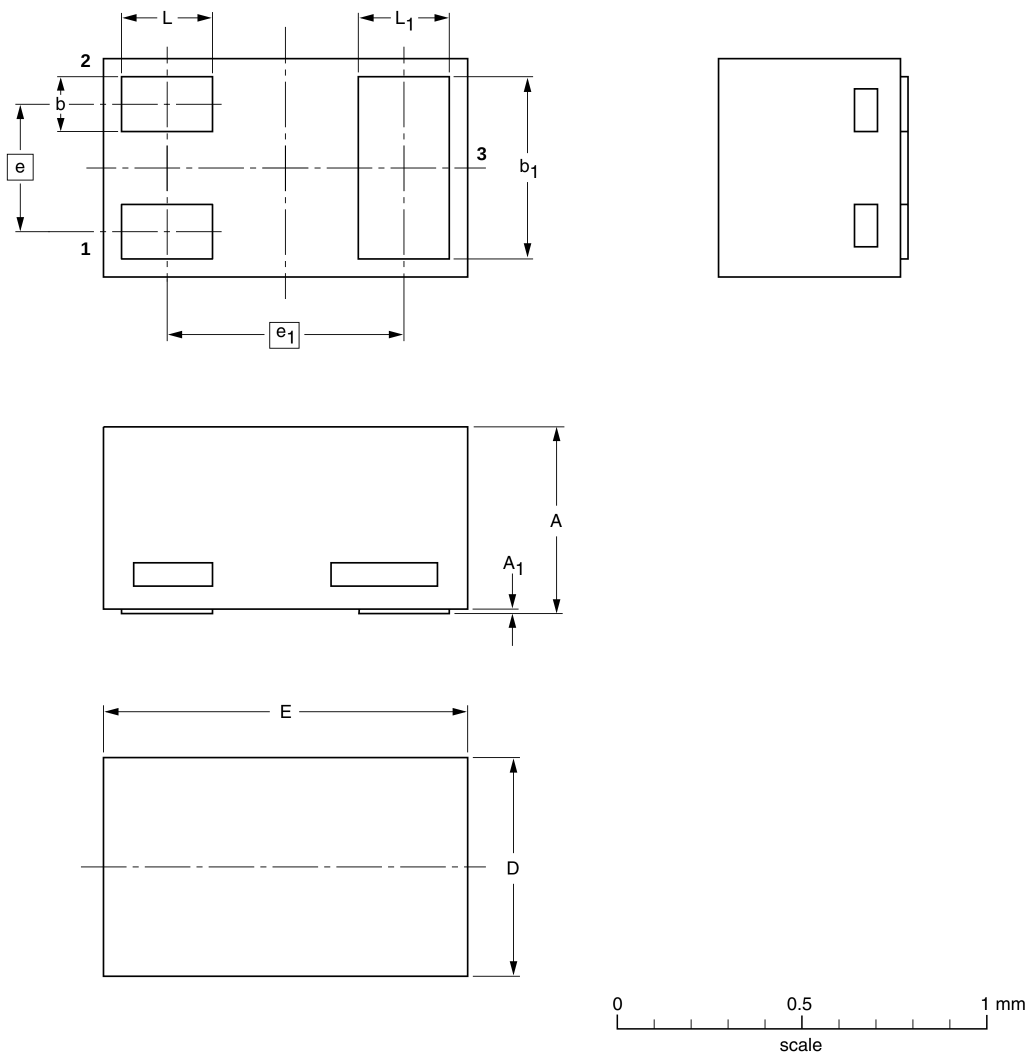


T_j = 25 °C and 150 °C; V_{GS} = 0 V

Fig 12. Source current as a function of source-drain voltage; typical values

8. Package outline

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm **SOT883**



DIMENSIONS (mm are the original dimensions)

UNIT	A$^{(1)}$	A_1 max.	b	b_1	D	E	e	e_1	L	L_1
mm	0.50 0.46	0.03	0.20 0.12	0.55 0.47	0.62 0.55	1.02 0.95	0.35	0.65	0.30 0.22	0.30 0.22

Note

1. Including plating thickness

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT883			SC-101			~~03-02-05~~ 03-04-03

Fig 13. Package outline SO883 (SC-101)

9. Soldering

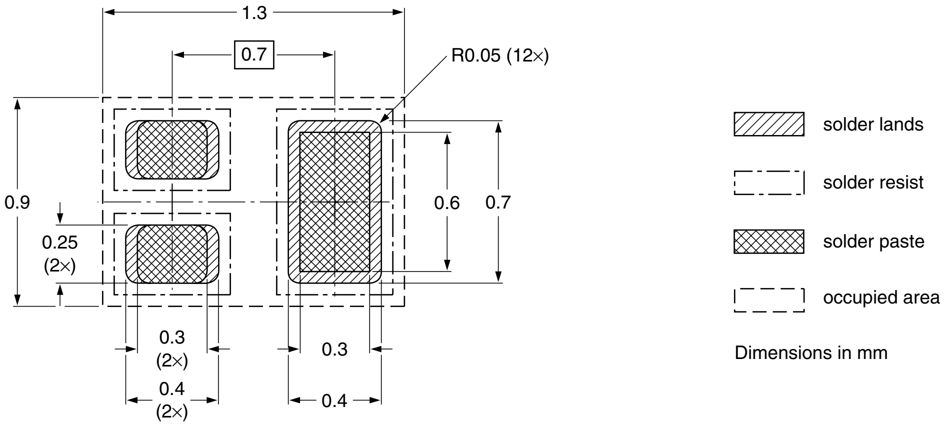


Fig 14. Reflow soldering footprint SOT883 (SC-101)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMZ1000UN v.2	20100917	Product data sheet	-	PMZ1000UN_1
Modifications:	• Modifications of thermal parameters • Section 11 "Legal information": updated			
PMZ1000UN_1	20100224	Product data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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13. Contents

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Document identifier: PMZ1000UN