FAIRCHILD SEMICONDUCTOR™

July 2000

FM93CS06 (MICROWIRE™ Bus Interface) 256-Bit Serial EEPROM with Data Protect and Sequential Read

General Description

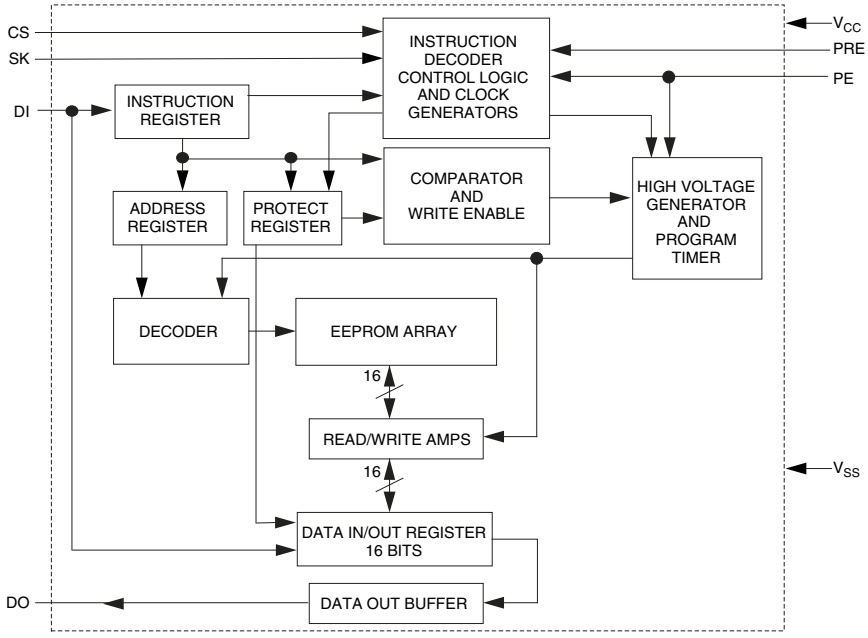
FM93CS06 is a 256-bit CMOS non-volatile EEPROM organized as 16 x 16-bit array. This device features MICROWIRE interface which is a 4-wire serial bus with chipselect (CS), clock (SK), data input (DI) and data output (DO) signals. This interface is compatible to many of standard Microcontrollers and Microprocessors. FM93CS06 offers programmable write protection to the memory array using a special register called Protect Register. Selected memory locations can be protected against write by programming this Protect Register with the address of the first memory location to be protected (all locations greater than or equal to this first address are then protected from further change). Additionally, this address can be "permanently locked" into the device, making all future attempts to change data impossible. In addition this device features "sequential read", by which, entire memory can be read in one cycle instead of multiple single byte read cycles. There are 10 instructions implemented on the FM93CS06, 5 of which are for memory operations and the remaining 5 are for Protect Register operations. This device is fabricated using Fairchild Semiconductor floating-gate CMOS process for high reliability, high endurance and low power consumption.

"LZ" and "L" versions of FM93CS06 offer very low standby current making them suitable for low power applications. This device is offered in both SO and TSSOP packages for small space considerations.

Features

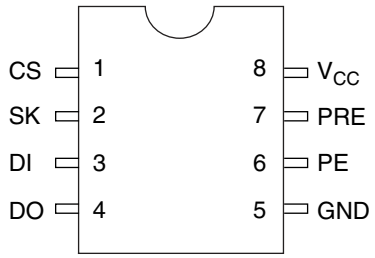
- Wide V_{CC} 2.7V - 5.5V
- Programmable write protection
- Sequential register read
- Typical active current of 200μA
  10μA standby current typical
  1μA standby current typical (L)
  0.1μA standby current typical (LZ)
- No Erase instruction required before Write instruction
- Self timed write cycle
- Device status during programming cycles
- 40 year data retention
- Endurance: 1,000,000 data changes
- Packages available: 8-pin SO, 8-pin DIP, 8-pin TSSOP

Functional Diagram



Connection Diagram

Dual-In-Line Package (N)
8–Pin SO (M8) and 8–Pin TSSOP (MT8)



Top View
Package Number
N08E, M08A and MTC08

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
PE	Program Enable
PRE	Protect Register Enable
V_{CC}	Power Supply

Ordering Information

FM 93 CS XX LZ E XXX

	Letter	Description
Package	N	8-pin DIP
	M8	8-pin SO
	MT8	8-pin TSSOP
Temp. Range	None	0 to 70°C
	V	-40 to +125°C
	E	-40 to +85°C
Voltage Operating Range	Blank	4.5V to 5.5V
	L	2.7V to 5.5V
	LZ	2.7V to 5.5V and <1µA Standby Current
Density	06	256 bits
	C	CMOS
	CS	Data protect and sequential read
Interface	93	MICROWIRE
Fairchild Memory Prefix		

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
FM93CS06	0°C to +70°C
FM93CS06E	-40°C to +85°C
FM93CS06V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 4.5V to 5.5V unless otherwise specified

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK=1.0 MHz		1	mA
I_{CCS}	Standby Current	CS = V_{IL}		50	µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±-1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 2	0.8 V_{CC} +1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	I_{OL} = 2.1 mA I_{OH} = -400 µA	 2.4	0.4	V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	I_{OL} = 10 µA I_{OH} = -10 µA	 V_{CC} - 0.2	0.2	V
f_{SK}	SK Clock Frequency	(Note 3)		1	MHz
t_{SKH}	SK High Time	0°C to +70°C -40°C to +125°C	250 300		ns
t_{SKL}	SK Low Time		250		ns
t_{CS}	Minimum CS Low Time	(Note 4)	250		ns
t_{CSS}	CS Setup Time		50		ns
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		100		ns
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		20		ns
t_{PD}	Output Delay			500	ns
t_{SV}	CS to Status Valid			500	ns
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		100	ns
t_{WP}	Write Cycle Time			10	ms

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltages with Respect to Ground	+6.5V to -0.3V
Lead Temperature (Soldering, 10 sec.)	+300°C
ESD rating	2000V

Operating Conditions

Ambient Operating Temperature	
FM93CS06L/LZ	0°C to +70°C
FM93CS06LE/LZE	-40°C to +85°C
FM93CS06LV/LZV	-40°C to +125°C
Power Supply (V_{CC})	2.7V to 5.5V

DC and AC Electrical Characteristics V_{CC} = 2.7V to 4.5V unless otherwise specified. Refer to page 3 for V_{CC} = 4.5V to 5.5V.

Symbol	Parameter	Conditions	Min	Max	Units
I_{CCA}	Operating Current	CS = V_{IH}, SK= 250 KHz		1	mA
I_{CCS}	Standby Current L LZ (2.7V to 4.5V)	CS = V_{IL}		 10 1	 µA µA
I_{IL} I_{OL}	Input Leakage Output Leakage	V_{IN} = 0V to V_{CC} (Note 2)		±1	µA
V_{IL} V_{IH}	Input Low Voltage Input High Voltage		-0.1 $0.8V_{CC}$	$0.15V_{CC}$ V_{CC} +1	V
V_{OL} V_{OH}	Output Low Voltage Output High Voltage	I_{OL} = 10µA I_{OH} = -10µA	 $0.9V_{CC}$	$0.1V_{CC}$	V
f_{SK}	SK Clock Frequency	(Note 3)	0	250	KHz
t_{SKH}	SK High Time		1		µs
t_{SKL}	SK Low Time		1		µs
t_{CS}	Minimum CS Low Time	(Note 4)	1		µs
t_{CSS}	CS Setup Time		0.2		µs
t_{PRES}	PRE Setup Time		50		ns
t_{DH}	DO Hold Time		70		ns
t_{PES}	PE Setup Time		50		ns
t_{DIS}	DI Setup Time		0.4		µs
t_{CSH}	CS Hold Time		0		ns
t_{PEH}	PE Hold Time		250		ns
t_{PREH}	PRE Hold Time		50		ns
t_{DIH}	DI Hold Time		0.4		µs
t_{PD}	Output Delay			2	µs
t_{SV}	CS to Status Valid			1	µs
t_{DF}	CS to DO in Hi-Z	CS = V_{IL}		0.4	µs
t_{WP}	Write Cycle Time			15	ms

Capacitance T_A = 25°C, f = 1 MHz or 250 KHz(Note 5)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance		5	pF
C_{IN}	Input Capacitance		5	pF

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical leakage values are in the 20nA range.

Note 3: The shortest allowable SK clock period = $1/f_{SK}$ (as shown under the f_{SK} parameter). Maximum SK clock speed (minimum SK period) is determined by the interaction of several AC parameters stated in the datasheet. Within this SK period, both t_{SKH} and t_{SKL} limits must be observed. Therefore, it is not allowable to set $1/f_{SK} = t_{SKHminimum} + t_{SKLminimum}$ for shorter SK cycle time operation.

Note 4: CS (Chip Select) must be brought low (to V_{IL}) for an interval of t_{CS} in order to reset all internal device registers (device reset) prior to beginning another opcode cycle. (This is shown in the opcode diagram on the following page.)

Note 5: This parameter is periodically sampled and not 100% tested.

AC Test Conditions

V_{CC} Range	V_{IL}/V_{IH} Input Levels	V_{IL}/V_{IH} Timing Level	V_{OL}/V_{OH} Timing Level	I_{OL}/I_{OH}
2.7V ≤ V_{CC} ≤ 5.5V (Extended Voltage Levels)	0.3V/1.8V	1.0V	0.8V/1.5V	±10µA
4.5V ≤ V_{CC} ≤ 5.5V (TTL Levels)	0.4V/2.4V	1.0V/2.0V	0.4V/2.4V	2.1mA/-0.4mA
Output Load: 1 TTL Gate (C_L = 100 pF)				

Pin Description

Chip Select (CS)

This is an active high input pin to FM93CS06 EEPROM (the device) and is generated by a master that is controlling the device. A high level on this pin selects the device and a low level deselects the device. All serial communications with the device is enabled only when this pin is held high. However this pin cannot be permanently tied high, as a rising edge on this signal is required to reset the internal state-machine to accept a new cycle and a falling edge to initiate an internal programming after a write cycle. All activity on the SK, DI and DO pins are ignored while CS is held low.

Serial Clock (SK)

This is an input pin to the device and is generated by the master that is controlling the device. This is a clock signal that synchronizes the communication between a master and the device. All input information (DI) to the device is latched on the rising edge of this clock input, while output data (DO) from the device is driven from the rising edge of this clock input. This pin is gated by CS signal.

Serial Input (DI)

This is an input pin to the device and is generated by the master that is controlling the device. The master transfers Input information (Start bit, Opcode bits, Array addresses and Data) serially via this pin into the device. This Input information is latched on the rising edge of the SCK. This pin is gated by CS signal.

Serial Output (DO)

This is an output pin from the device and is used to transfer Output data via this pin to the controlling master. Output data is serially shifted out on this pin from the rising edge of the SCK. This pin is active only when the device is selected.

Protect Register Enable (PRE)

This is an active high input pin to the device and is used to distinguish operations to memory array and operations to Protect Register. When this pin is held low, operations to the memory array are enabled. When this pin is held high, operations to the Protect Register are enabled. This pin operates in conjunction with PE pin. Refer Table1 for functional matrix of this pin for various operations.

Program Enable (PE)

This is an active high input pin to the device and is used to enable operations, that are write in nature, to the memory array and to the Protect register. When this pin is held high, operations that are “write” in nature are enabled. When this pin is held low, operations that are “write” in nature are disabled. This pin operates in conjunction with PRE pin. Refer Table1 for functional matrix of this pin for various operations.

Microwire Interface

A typical communication on the Microwire bus is made through the CS, SK, DI and DO signals. To facilitate various operations on the Memory array and on the Protect Register, a set of 10 instructions are implemented on FM93CS06. The format of each instruction is listed in Table 1.

Instruction

Each of the above 10 instructions is explained under individual instruction descriptions.

Start Bit

This is a 1-bit field and is the first bit that is clocked into the device when a Microwire cycle starts. This bit has to be “1” for a valid cycle to begin. Any number of preceding “0” can be clocked into the device before clocking a “1”.

Opcode

This is a 2-bit field and should immediately follow the start bit. These two bits (along with PRE, PE signals and 2 MSB of address field) select a particular instruction to be executed.

Address Field

This is a 6-bit field and should immediately follow the Opcode bits. In FM93CS06, only the LSB 4 bits are used for address decoding during READ, WRITE and PRWRITE instructions. During these instructions (READ, WRITE and PRWRITE), the MSB 2 bits are "don't care" (can be 0 or 1). During all other instructions (with the exception of PRREAD), the MSB 2 bits are used to decode instruction (along with Opcode bits, PRE and PE signals).

Data Field

This is a 16-bit field and should immediately follow the Address bits. Only the WRITE and WRALL instructions require this field. D15 (MSB) is clocked first and D0 (LSB) is clocked last (both during writes as well as reads).

TABLE 1. Instruction set

Instruction	Start Bit	Opcode Field	Address Field						Data Field	PRE Pin	PE Pin
READ	1	10	X	X	A3	A2	A1	A0		0	X
WEN	1	00	1	1	X	X	X	X		0	1
WRITE	1	01	X	X	A3	A2	A1	A0	D15-D0	0	1
WRALL	1	00	0	1	X	X	X	X	D15-D0	0	1
WDS	1	00	0	0	X	X	X	X		0	X
PRREAD	1	10	X	X	X	X	X	X		1	X
PREN	1	00	1	1	X	X	X	X		1	1
PRCLEAR	1	11	1	1	1	1	1	1		1	1
PRWRITE	1	01	X	X	A3	A2	A1	A0		1	1
PRDS	1	00	0	0	0	0	0	0		1	1

Functional Description

A typical Microwire cycle starts by first selecting the device (bringing the CS signal high). Once the device is selected, a valid Start bit ("1") should be issued to properly recognize the cycle. Following this, the 2-bit opcode of appropriate instruction should be issued. After the opcode bits, the 6-bit address information should be issued. For certain instructions, some (or all) of these 6 bits are don't care values (can be "0" or "1"), but they should still be issued. Following the address information, depending on the instruction (WRITE and WRALL), 16-Bit data is issued. Otherwise, depending on the instruction (READ and PRREAD), the device starts to drive the output data on the DO line. Other instructions perform certain control functions and do not deal with data bits. The Microwire cycle ends when the CS signal is brought low. However during certain instructions, falling edge of the CS signal initiates an internal cycle (Programming), and the device remains busy till the completion of the internal cycle. Each of the 10 instructions is explained in detail in the following sections.

Memory Instructions

Following five instructions, READ, WEN, WRITE, WRALL and WDS are specific to operations intended for memory array. The PRE pin should be held low during these instructions.

1) Read and Sequential Read (READ)

READ instruction allows data to be read from a selected location in the memory array. Input information (Start bit, Opcode and Address) for this instruction should be issued as listed under Table1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer from the selected memory location into a 16-bit serial-out shift register. This 16-bit data is then shifted out on the DO pin. D15 bit (MSB) is shifted out first and D0 bit (LSB) is shifted out last. A dummy-bit (logical 0) precedes this 16-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 16-bit data, the CS signal can be brought low to end the Read cycle. The PRE pin should be held low during this cycle. Refer *Read cycle diagram*.

This device also offers "sequential memory read" operation to allow reading of data from the additional memory locations instead of just one location. It is started in the same manner as normal read but the cycle is continued to read further data (instead of terminating after reading the first 16-bit data). After providing 16-bit data, the device automatically increments the address pointer to the next location and continues to provide the data from that location. Any number of locations can be read out in this manner, however, after reading out from the last location, the address pointer points back to the first location. If the cycle is continued further, data will be read from this first location onward. In this mode of read, the dummy-bit is present only when the very first data is read (like normal read cycle) and is not present on subsequent data reads. The PRE pin should be held low during this cycle. Refer *Sequential Read cycle diagram*.

2) Write Enable (WEN)

When V_{CC} is applied to the part, it "powers up" in the Write Disable (WDS) state. Therefore, all programming operations (for both memory array and Protect Register) must be preceded by a Write Enable (WEN) instruction. Once a Write Enable instruction is executed, programming remains enabled until a Write Disable (WDS) instruction is executed or V_{CC} is completely removed from the part. Input information (Start bit, Opcode and Address) for this WEN instruction should be issued as listed under Table1. The device becomes write-enabled at the end of this cycle when the CS signal is brought low. The PRE pin should be held low during this cycle. Execution of a READ instruction is independent of WEN instruction. Refer *Write Enable cycle diagram.*

3) Write (WRITE)

WRITE instruction allows write operation to a specified location in the memory with a specified data. This instruction is valid only when the following are true:

- Device is write-enabled (Refer WEN instruction)
- Address of the write location is not write-protected
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRITE instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction.

The status of the internal programming cycle can be polled at any time by bringing the CS signal high again, after t_{CS} interval. When CS signal is high, the DO pin indicates the READY/BUSY status of the chip. DO = logical 0 indicates that the programming is still in progress. DO = logical 1 indicates that the programming is finished and the device is ready for another instruction. It is not required to provide the SK clock during this status polling. While the device is busy, it is recommended that no new instruction be issued. Refer *Write cycle diagram.*

It is also recommended to follow this instruction (after the device becomes READY) with a Write Disable (WDS) instruction to safeguard data against corruption due to spurious noise, inadvertent writes etc.

4) Write All (WRALL)

Write all (WRALL) instruction is similar to the Write instruction except that WRALL instruction will simultaneously program all memory locations with the data pattern specified in the instruction. This instruction is valid only when the following are true:

- Protect Register has been cleared (Refer PRCLEAR instruction)
- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin should be held low during this cycle

Input information (Start bit, Opcode, Address and Data) for this WRALL instruction should be issued as listed under Table1. After inputting the last bit of data (D0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Write All cycle diagram.*

5) Write Disable (WDS)

Write Disable (WDS) instruction disables all programming operations and is recommended to follow all programming operations. Executing this instruction after a valid write instruction would protect against accidental data disturb due to spurious noise, glitches, inadvertent writes etc. Input information (Start bit, Opcode and Address) for this WDS instruction should be issued as listed under Table1. The device becomes write-disabled at the end of this cycle when the CS signal is brought low. Execution of a READ instruction is independent of WDS instruction. Refer *Write Disable cycle diagram.*

Protect Register Instructions

Following five instructions, PRREAD, PREN, PRCLEAR, PRWRITE and PRDS are specific to operations intended for Protect Register. The PRE pin should be held high during these instructions.

1) Protect Register Read (PRREAD)

This instruction reads the content of the internal Protect Register. Content of this register is 6-bit wide and is the starting address of the "write-protected" section of the memory array. All memory locations greater than or equal to this address are write-protected. Input information (Start bit, Opcode and Address) for this PRREAD instruction should be issued as listed under Table1. Upon receiving a valid input information, decoding of the opcode and the address is made, followed by data transfer (address information) from the Protect Register. This 6-bit data is then shifted out on the DO pin with the MSB first and the LSB last. Like the READ instruction a dummy-bit (logical 0) precedes this 6-bit data output string. Output data changes are initiated on the rising edge of the SK clock. After reading the 6-bit data, the CS signal can be brought low to end the PRREAD cycle. The PRE pin should be held high during this cycle. Refer *Protect Register Read cycle diagram.*

Though the content of this register is 6-bit wide, only the last 4 bits (LSB) are valid for FM93CS06 device.

2) Protect Register Enable (PREN)

This instruction is required to enable PRCLEAR, PRWRITE and PRDS instructions and should be executed prior to executing PRCLEAR, PRWRITE and PRDS instructions. However, this PREN instruction is enabled (valid) only the following are true

- Device is write-enabled (Refer WEN instruction)
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PREN instruction should be issued as listed under Table1. The Protect Register becomes enabled for PRCLEAR, PRWRITE and PRDS instructions at the end of this cycle when the CS signal is brought low. Note that this PREN instruction **must immediately precede** a PRCLEAR, PRWRITE or PRDS instruction. In other words, no other instruction should be executed between a PREN instruction and a PRCLEAR, PRWRITE or PRDS instruction. Refer *Protect Register Enable cycle diagram.*

3) Protect Register Clear (PRCLEAR)

This instruction clears the content of the Protect register and therefore enables write operations (WRITE or WRALL) to all memory locations. Executing this instruction will program the content of the Protect Register with a pattern of all 1s. However, in this case, WRITE operation to the last memory address (0x001111) is still enabled. PRCLEAR instruction is enabled (valid) only when the following are true:

- PREN instruction was executed **immediately prior** to PRCLEAR instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRCLEAR instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed clear cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal clear cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Clear cycle diagram.*

4) Protect Register Write (PRWRITE)

This instruction is used to write the starting address of the memory section to be write-protected into the Protect register. After the execution of PRWRITE instruction, all memory locations greater than or equal to this address are write-protected. PRWRITE instruction is enabled (valid) only the following are true:

- PRCLEAR instruction was executed first (to clear the Protect Register)
- PREN instruction was executed **immediately prior** to PRWRITE instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRWRITE instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. Refer *Protect Register Write cycle diagram.*

5) Protect Register Disable (PRDS)

Unlike all other instructions, this instruction is a **one-time-only** instruction which when executed **permanently write-protects the Protect Register** and renders it unalterable in the future. This instruction is useful to safeguard vital data (typically read only data) in the memory against any possible corruption. PRDS instruction is enabled (valid) only the following are true:

- PREN instruction was executed **immediately prior** to PRDS instruction
- PE pin is held high during this cycle
- PRE pin is held high during this cycle

Input information (Start bit, Opcode and Address) for this PRDS instruction should be issued as listed under Table1. After inputting the last bit of address (A0 bit), CS signal must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. It takes t_{WP} time (Refer appropriate DC and AC Electrical Characteristics table) for the internal programming cycle to finish. During this time, the device remains busy and is not ready for another instruction. Status of the internal programming can be polled as described under WRITE instruction description. While the device is busy, it is recommended that no new instruction be issued. The Protect Register is permanently write-protected at the end of this cycle. Refer *Protect Register Disable cycle diagram.*

Clearing of Ready/Busy status

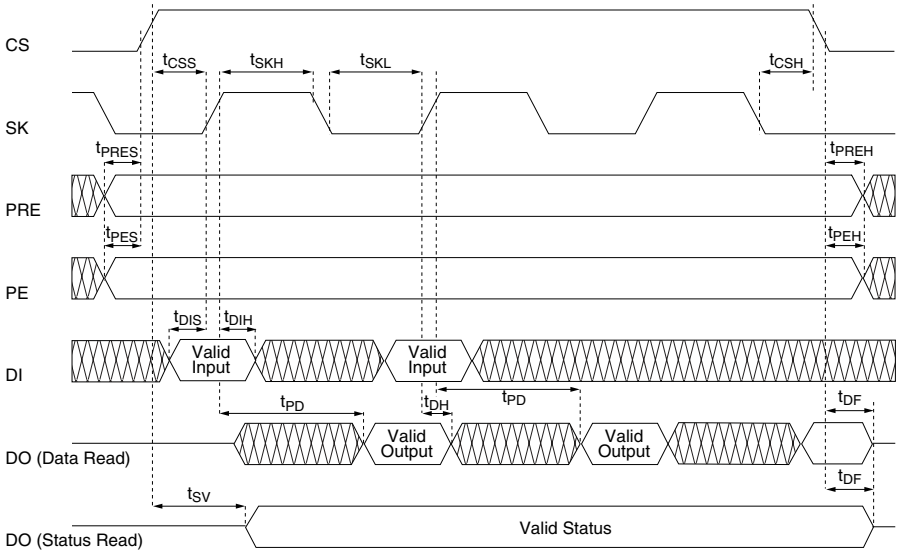
When programming is in progress, the Data-Out pin will display the programming status as either BUSY (low) or READY (high) when CS is brought high (DO output will be tri-stated when CS is low). To restate, during programming, the CS pin may be brought high and low any number of times to view the programming status without affecting the programming operation. Once programming is completed (Output in READY state), the output is 'cleared' (returned to normal tri-state condition) by clocking in a Start Bit. After the Start Bit is clocked in, the output will return to a tri-stated condition. When clocked in, this Start Bit can be the first bit in a command string, or CS can be brought low again to reset all internal circuits. Refer *Clearing Ready Status* diagram.

Related Document

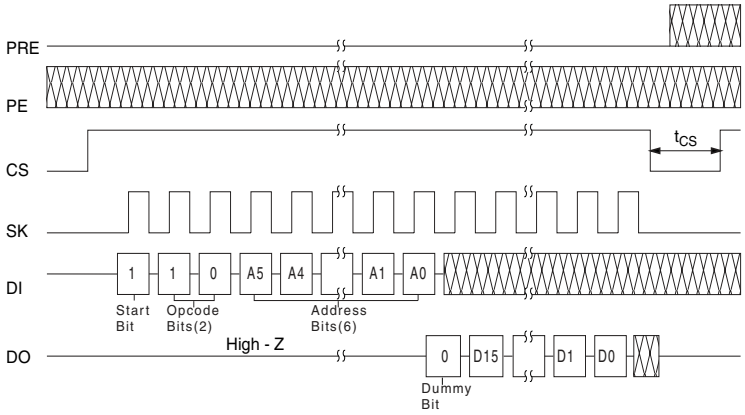
Application Note: AN758 - Using Fairchild's MICROWIRE™ EEPROM.

Timing Diagrams

SYNCHRONOUS DATA TIMING

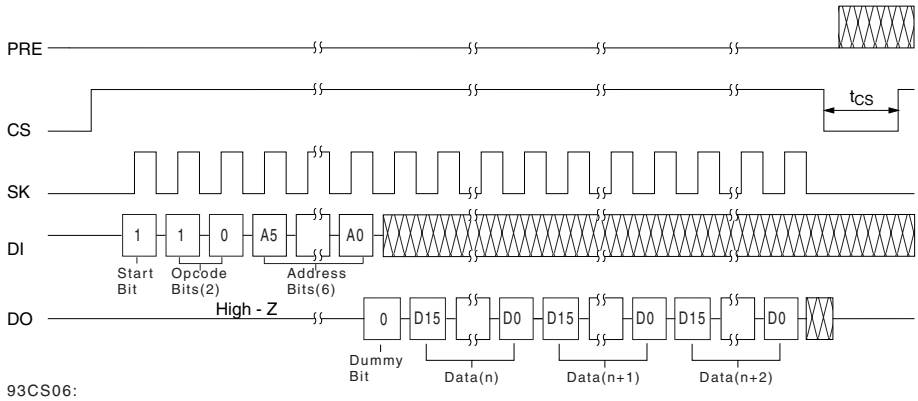


NORMAL READ CYCLE (READ)



93CS06:
Address bits pattern -> x-x-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A3-A0 -> User defined)

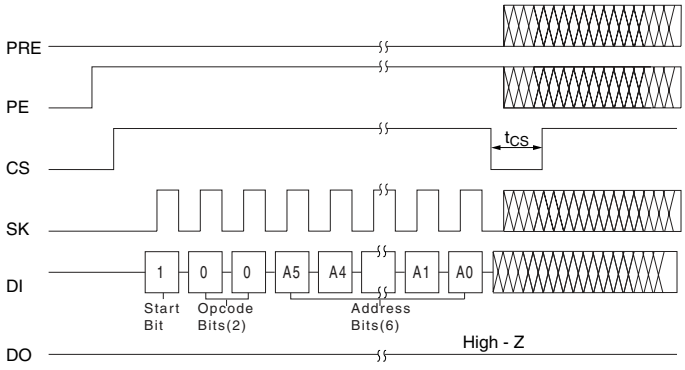
SEQUENTIAL READ CYCLE (PRE = 0; PE = X)



93CS06:
Address bits pattern -> x-x-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A3-A0 -> User defined)

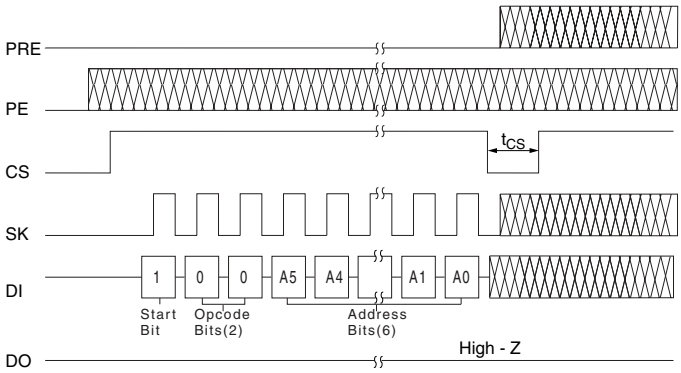
Timing Diagrams (Continued)

WRITE ENABLE CYCLE (WEN)



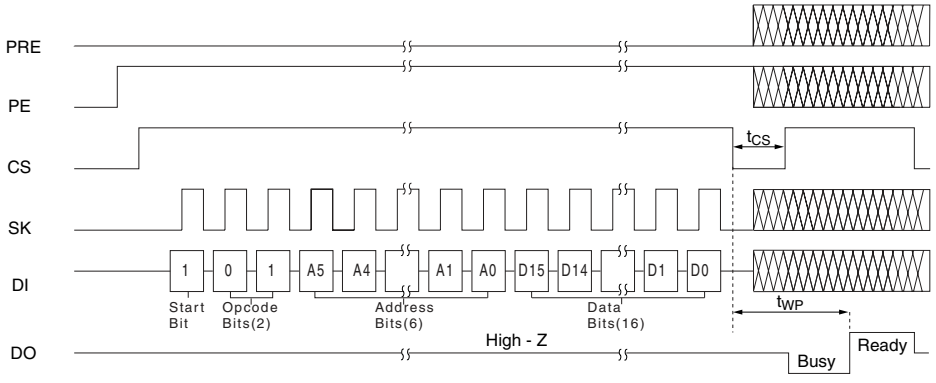
93CS06:
Address bits pattern -> 1-1-x-x-x-x; (x -> Don't Care, can be 0 or 1)

WRITE DISABLE CYCLE (WDS)



93CS06:
Address bits pattern -> 0-0-x-x-x-x; (x -> Don't Care, can be 0 or 1)

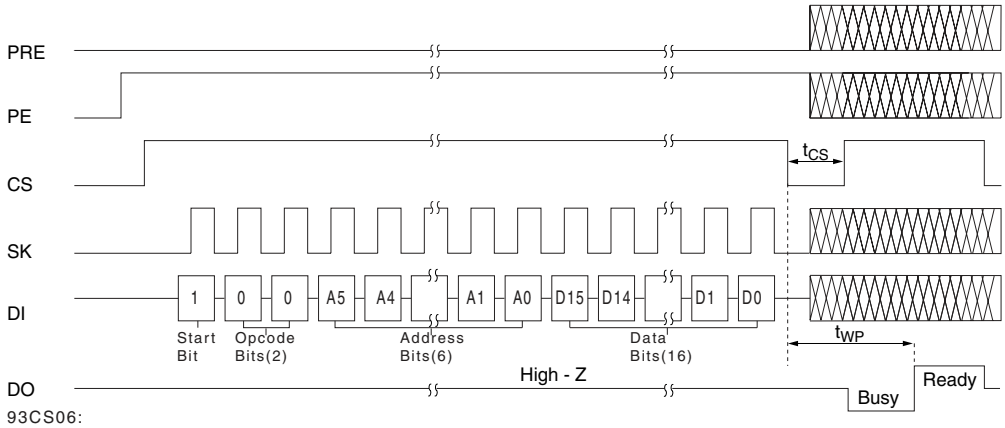
WRITE CYCLE (WRITE)



93CS06:
Address bits pattern -> x-x-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A3-A0 -> User defined)
Data bits pattern -> User defined

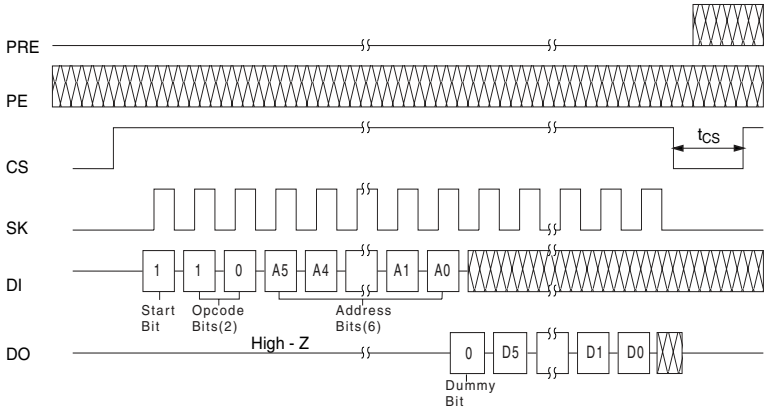
Timing Diagrams (Continued)

WRITE ALL CYCLE (WRALL)



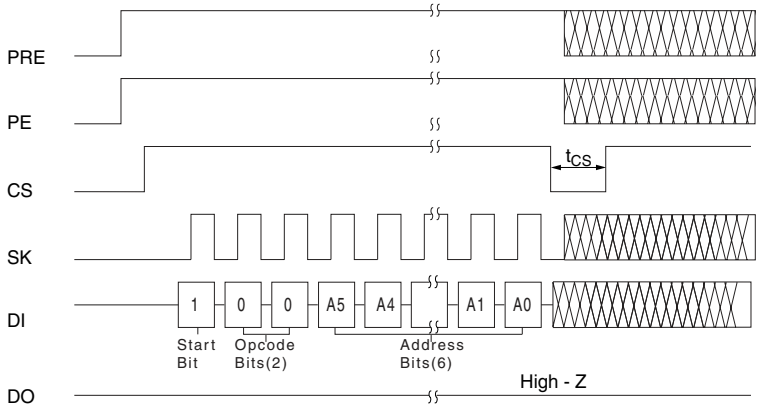
93CS06:
Address bits pattern -> 0-1-x-x-x-x; (x -> Don't Care, can be 0 or 1)
Data bits pattern -> User defined

PROTECT REGISTER READ CYCLE (PRREAD)



93CS06:
Address bits pattern -> x-x-x-x-x-x; (x -> Don't Care, can be 0 or 1)
Of the 6-bit output data(D5-D0), only D3 to D0 are valid and they correspond to A3 to A0 respectively.

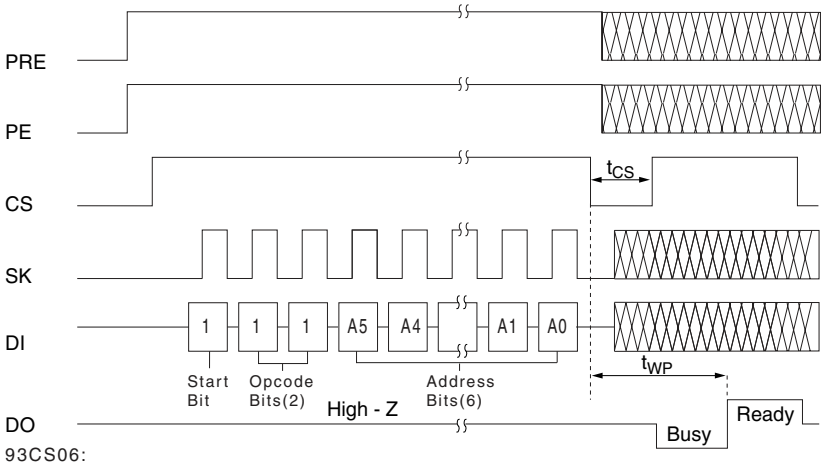
PROTECT REGISTER ENABLE CYCLE (PREN)



93CS06:
Address bits pattern -> 1-1-x-x-x-x; (x -> Don't Care, can be 0 or 1)

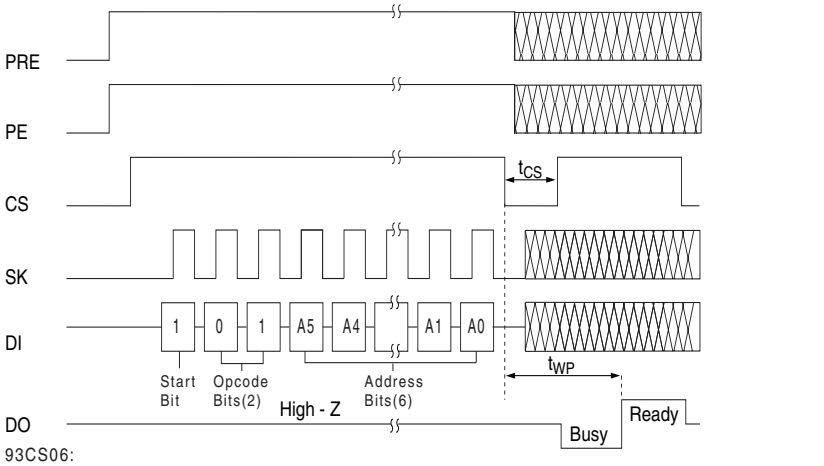
Timing Diagrams (Continued)

PROTECT REGISTER CLEAR CYCLE (PRCLEAR)



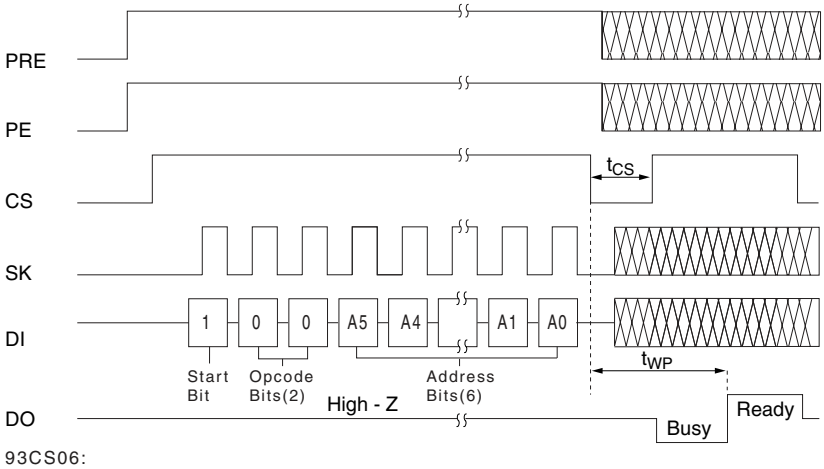
93CS06:
Address bits pattern -> 1-1-1-1-1-1

PROTECT REGISTER WRITE CYCLE (PRWRITE)



93CS06:
Address bits pattern -> x-x-A3-A2-A1-A0; (x -> Don't Care, can be 0 or 1); (A3-A0 -> User defined)

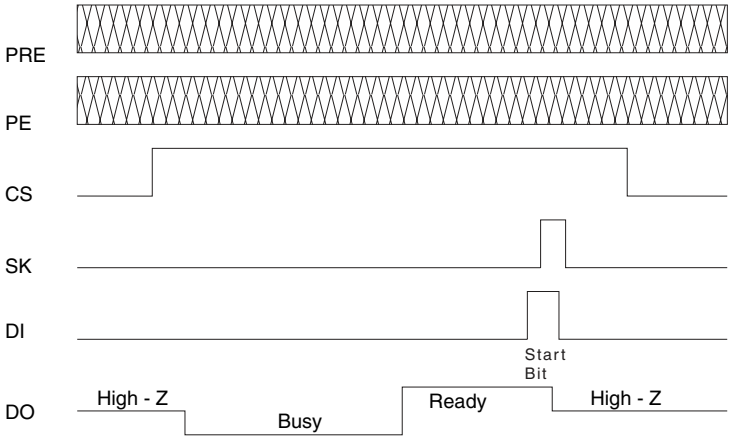
PROTECT REGISTER DISABLE CYCLE (PRDS)



93CS06:
Address bits pattern -> 0-0-0-0-0-0

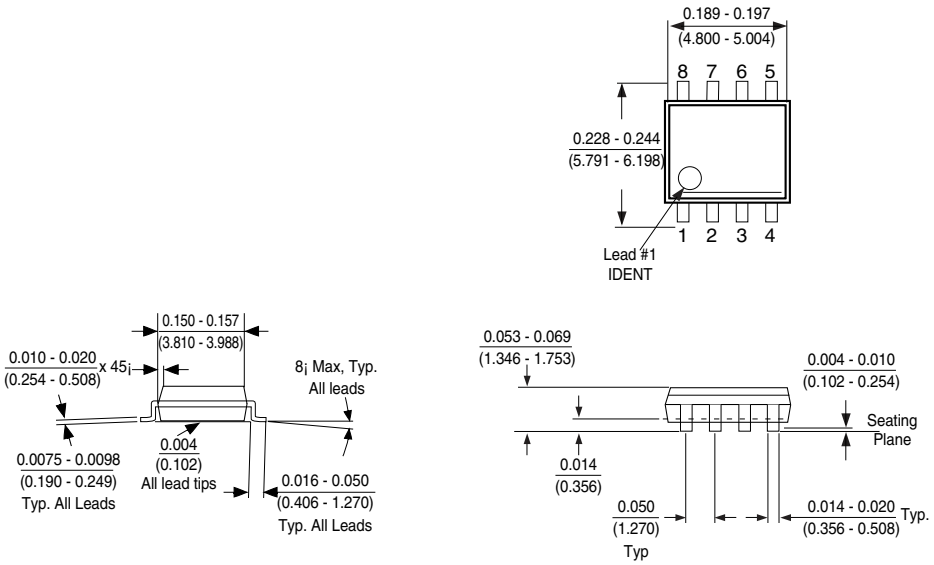
Timing Diagrams (Continued)

CLEARING READY STATUS



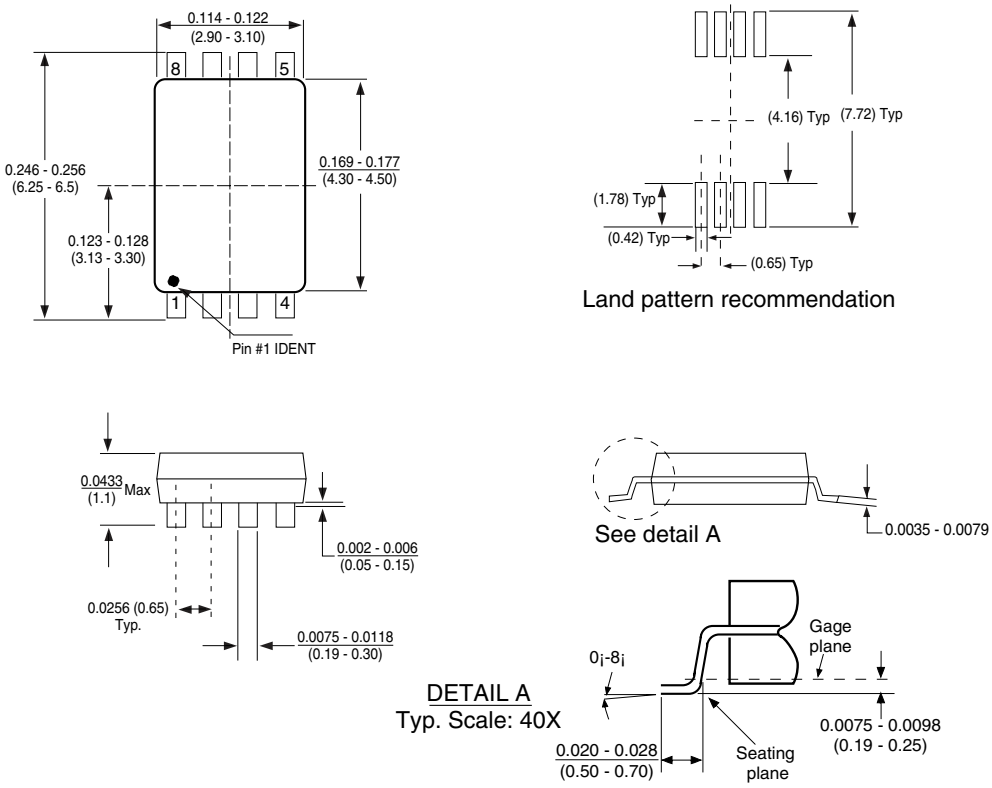
Note: This Start bit can also be part of a next instruction. Hence the cycle can be continued(instead of getting terminated, as shown) as if a new instruction is being issued.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Package, Small Outline, 0.15 Wide, 8-Lead (M8)
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted

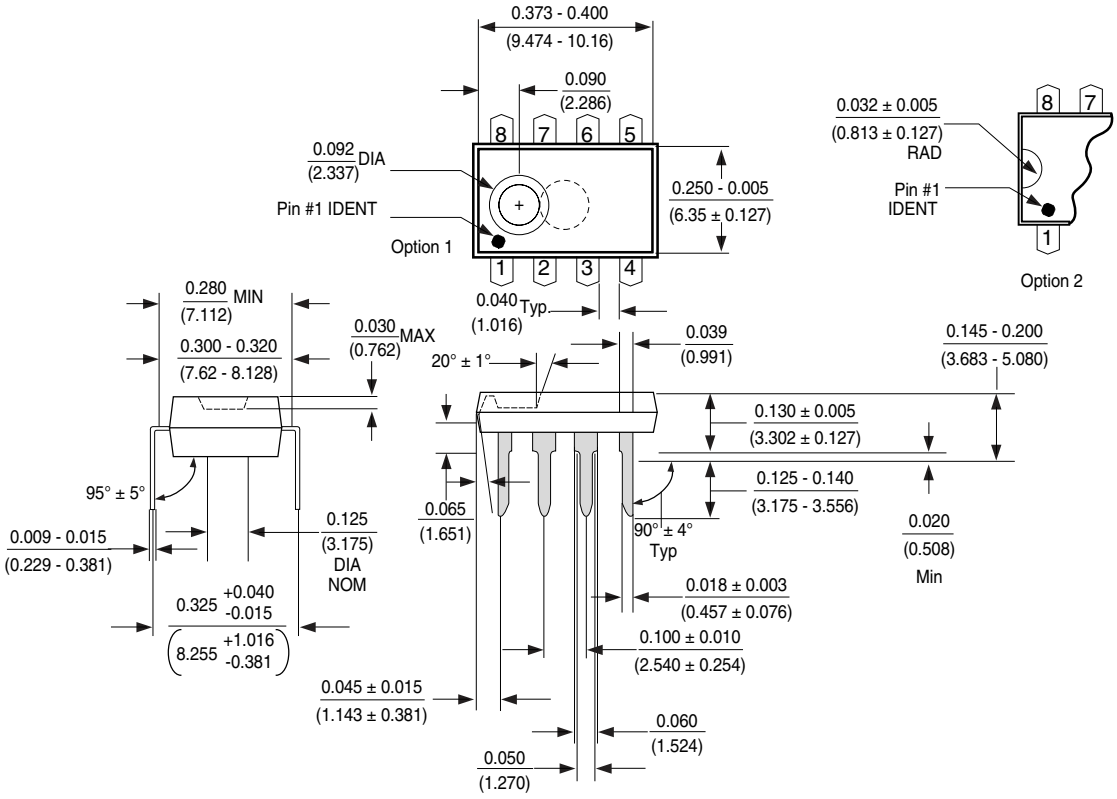


Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Dual-In-Line Package (N)
Package Number N08E

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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