

# 8-Bit Registers with Master Reset or Clock Enable

SN54/74LS273 SN54/74LS377

SN54/74S273 SN54/74S377

## Features/Benefits

- 20-Pin SKINNYDIP® saves space
- 8-bit data path matches byte boundaries
- Ideal for microprogram instruction registers
- Ideal for microprogram interface
- Suitable for pipeline data registers
- Useful in timing, sequencing, and control circuits
- Three '273s may replace four '174s
- Three '377s may replace four '378s/Am25S07s

## Description

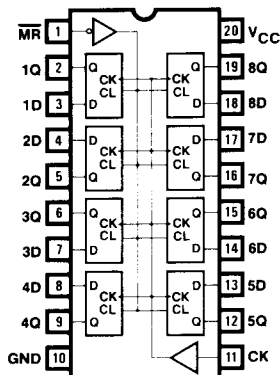
These 8-bit registers contain eight D-type flip-flops, they feature very low  $I_{CC}$  (17 mA typical) on the low-power Schottky devices and very-high-speed operation on the Schottky devices. The '273 register is loaded on the rising edge of the clock (CK) and asyn-

## Function Table '273

INPUTS		OUTPUT	
MR	CLOCK	DATA	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L or H or ↓	X	Q <sub>0</sub>

## Logic Symbols

8-Bit Register with Master Reset '273



## Ordering Information

PART NUMBER	PKG	TEMP	POLA-RITY	CONTROL OPTION	POWER
SN54LS273 SN74LS273	J,F,L,W N,J,L	Mil Com	Non-invert	Master Reset	LS
SN54LS377 SN74LS377	J,F,L,W N,J,L	Mil Com		Clock Enable	
SN54S273 SN74S273	J,F,L,W N,J,L	Mil Com	Non-invert	Master Reset	S
SN54S377 SN74S377	J,F,L,W N,J,L	Mil Com		Clock Enable	

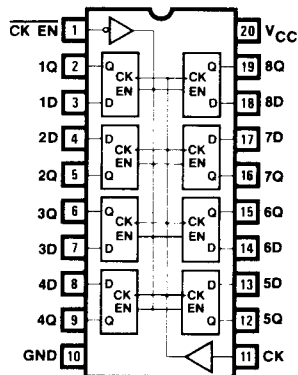
chronously cleared whenever the master reset line,  $\overline{MR}$ , is low. The '377 register is loaded on the rising edge of the clock provided that the clock enable line, CK EN, is low.

All of the 8-bit devices are packaged in the popular 20-pin SKINNYDIP.

## Function Table '377

INPUTS		OUTPUT	
CK EN	CLOCK	DATA	Q
H	X	X	Q <sub>0</sub>
L	↑	H	H
L	↑	L	L
X	L or H or ↓	X	Q <sub>0</sub>

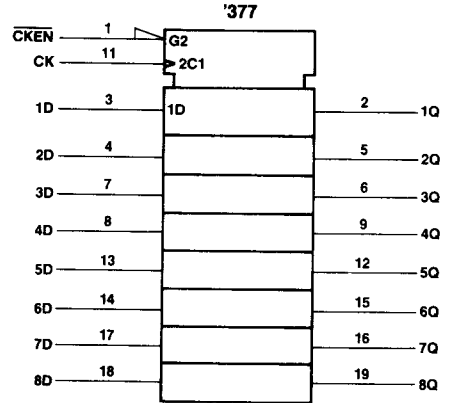
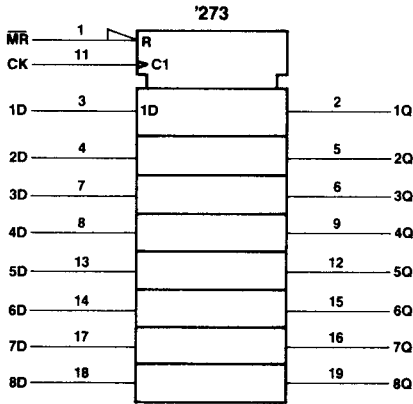
8-Bit Register with Clock Enable '377



**Absolute Maximum Ratings**

Supply voltage $V_{CC}$ .....	7 V
Input voltage .....	5.5 V
Off-state output voltage .....	5.5 V
Storage temperature range .....	-65° C to + 150° C

**IEEE Symbols**



**Operating Conditions**

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface, Test Load/Waveforms)	FIGURE	MILITARY			COMMERCIAL			UNIT						
				MIN	TYP	MAX	MIN	TYP	MAX							
$V_{CC}$	Supply voltage			4.5	5	5.5	4.75	5	5.25	V						
$T_A$	Operating free-air temperature			-55		125	0		75	°C						
$t_W$	Width of clock	High- $t_{WH}$	1	20			20			ns						
		Low- $t_{WL}$														
$t_{WMR}$	Width of Master Reset ('LS273 only)	Low- $t_{WMRL}$	2	20			20			ns						
$t_{rec}$		$\overline{MR}$ to CK ('S273 only)	2	25	↑		25	↑		ns						
$t_{su}$	Setup time	Data input to CK	3	20	↑		20	↑		ns						
		Low $\overline{CK EN}$ to CK ('LS377 only)									4	25	↑		25	↑
		High $\overline{CK EN}$ to CK ('LS377 only)														
$t_h$	Hold time	Data input	3	5	↑		5	↑		ns						
		Low $\overline{CK EN}$ to CK ('LS377 only)									4	5	↑		5	↑
		High $\overline{CK EN}$ to CK ('LS377 only)														

↑ The arrow indicates the transition of the clock/enable input used for reference. ↑ for the low-to-high transition. ↓ for the high-to-low transition.

**Electrical Characteristics** Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY		COMMERCIAL		UNIT
				MIN	TYP	MAX	MIN	
V <sub>IL</sub>	Low-level input voltage				0.7		0.8	V
V <sub>IH</sub>	High-level input voltage			2		2		V
V <sub>IC</sub>	Input clamp voltage	V <sub>CC</sub> = MIN	I <sub>I</sub> = -18 mA		-1.5		-1.5	V
I <sub>IL</sub>	Low-level input current	V <sub>CC</sub> = MAX	V <sub>I</sub> = 0.4 V		-0.4		-0.4	mA
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX	V <sub>I</sub> = 2.7 V		20		20	μA
I <sub>I</sub>	Maximum input current	V <sub>CC</sub> = MAX	V <sub>I</sub> = 7 V		0.1		0.1	mA
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN V <sub>IL</sub> = MAX V <sub>IH</sub> = 2 V	I <sub>OL</sub> = 4 mA	0.25	0.4	0.25	0.4	V
			I <sub>OL</sub> = 8 mA			0.35	0.5	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN V <sub>IL</sub> = MAX V <sub>IH</sub> = 2 V	I <sub>OH</sub> = -400 μA	2.5	3.4	2.7	3.4	V
I <sub>OS</sub>	Output short-circuit current*	V <sub>CC</sub> = MAX		-20	-100	-20	-100	mA
I <sub>CC</sub>	Supply current †	V <sub>CC</sub> = MAX Outputs open	LS273	17	27	17	27	mA
			LS377	17	28	17	28	

\* Note more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

† I<sub>CC</sub> is measured after first a momentary ground, and then 4.5 V is applied to clock, while the following other input conditions are held:

- (a) for the 'LS273 — 4.5 V on all data and master-reset inputs.
- (b) for the 'LS377 — ground on all data and clock-enable inputs.

**Switching Characteristics** V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	LS273			LS377			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>MAX</sub>	Maximum Clock frequency	C <sub>L</sub> = 15 pF R <sub>L</sub> = 2KΩ	30	40		35	40	MHz	
t <sub>PLH</sub>	Clock to Output delay				27			27	ns
t <sub>PHL</sub>					27			27	ns
t <sub>PHL</sub>	Master Reset to output delay ('LS273 only)				27				ns

### Absolute Maximum Ratings

Supply voltage $V_{CC}$ .....	7 V
Input voltage .....	5.5 V
Off-state output voltage .....	5.5 V
Storage temperature range .....	-65° C to + 150° C

### Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS (See Interface, Test Load/Waveforms)	FIGURE	MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{CC}$	Supply voltage			4.5	5	5.5	4.75	5	5.25	V
$T_A$	Operating free-air temperature			-55		125	0		75	°C
$t_W$	Width of clock	High- $t_{WH}$	1	7			7			ns
		Low- $t_{WL}$								
$t_{WMR}$	Width of Master Reset ('S273 only)	Low- $t_{WMRL}$	2	10			10			ns
$t_{rec}$		$\overline{MR}$ to CK ('S273 only)	2	7 †			7 †			ns
$t_{su}$	Setup time	Data input to CK	3	5 †			5 †			ns
		Low $\overline{CK EN}$ to CK ('S377 only)	4	9 †			9 †			
		High $\overline{CK EN}$ to CK ('S377 only)	4	9 †			9 †			
$t_h$	Hold time	Data input	3	3 †			3 †			ns ns
		Low $\overline{CK EN}$ to CK ('S377 only)	4	3 †			3 †			
		High $\overline{CK EN}$ to CK ('S377 only)		0 †			0 †			

† The arrow indicates the transition of the clock/enable input used for reference. † for the low-to-high transition, ‡ for the high-to-low transition.

### Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
$V_{IL}$	Low-level input voltage					0.8			0.8	V
$V_{IH}$	High-level input voltage			2			2			V
$V_{IC}$	Input clamp voltage	$V_{CC} = \text{MIN}$	$I_I = -18 \text{ mA}$			-1.2			-1.2	V
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.5 \text{ V}$			-250			-250	μA
$I_{IH}$	High-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.7 \text{ V}$			50			50	μA
$I_I$	Maximum input current	$V_{CC} = \text{MAX}$	$V_I = 5.5 \text{ V}$			1			1	mA
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}$ $V_{IL} = \text{MAX}$ $V_{IH} = 2 \text{ V}$	$I_{OL} = 20 \text{ mA}$			0.5			0.5	V
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}$ $V_{IL} = \text{MAX}$ $V_{IH} = 2 \text{ V}$	$I_{OH} = -1 \text{ mA}$	2.5	3.4		2.7	3.4		V
$I_{OS}$	Output short-circuit current*	$V_{CC} = \text{MAX}$		-40		-100	-40		-100	mA
$I_{CC}$	Supply current †	$V_{CC} = \text{MAX}$	'S273	150			150			mA
		Outputs open	'S377	160			160			

\* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second

**Switching Characteristics**  $V_{CC} = 5V, T_A = 25^\circ C$

SYMBOL	PARAMETER	TEST CONDITIONS (See Test Load/Waveforms)	'S273			'S377			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f <sub>MAX</sub>	Maximum Clock frequency	C <sub>L</sub> = 15 pF R <sub>L</sub> = 280Ω	75	110		75	110		MHz
t <sub>PLH</sub>	Clock to Output delay			6	15		6	15	ns
t <sub>PHL</sub>				9	15		9	15	ns
t <sub>PHL</sub>	Master Reset to output delay (‘S273 only)			13	22				ns

CLOCK PULSE WIDTH AND CLOCK TO OUTPUT DELAYS

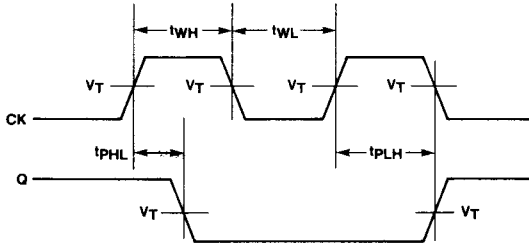


Figure 1

DATA SET-UP AND HOLD TIMES

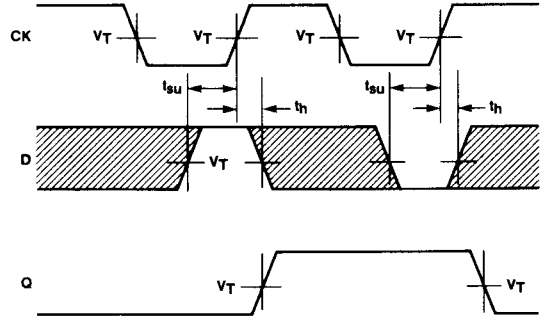


Figure 3

MASTER RESET PULSE WIDTH, MASTER RESET TO OUTPUT DELAY AND MASTER RESET TO CLOCK RECOVERY TIME FOR 'S273

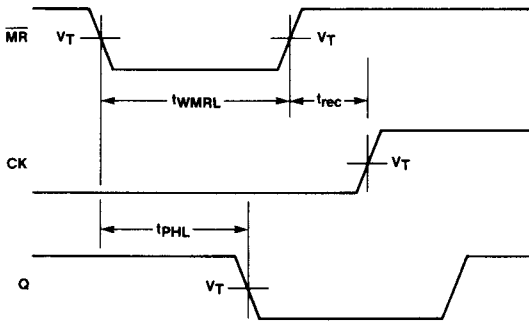


Figure 2

CLOCK ENABLE SETUP AND HOLD TIMES FOR 'S377

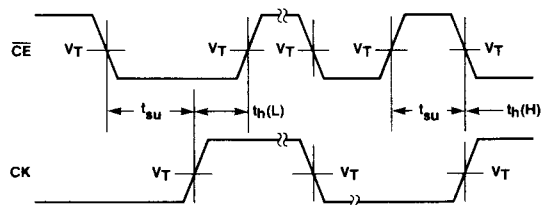
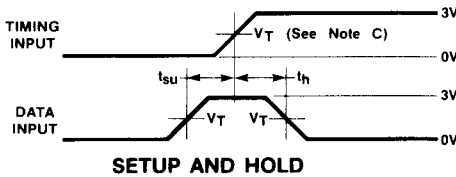
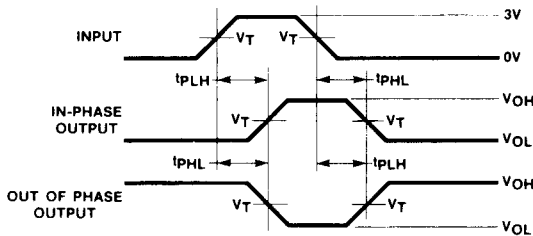


Figure 4

Test Waveforms

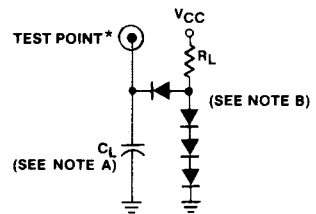


SETUP AND HOLD



PROPAGATION DELAY

Test Load

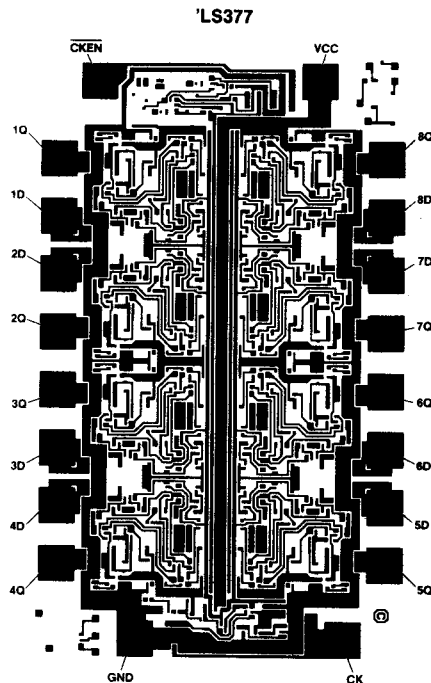
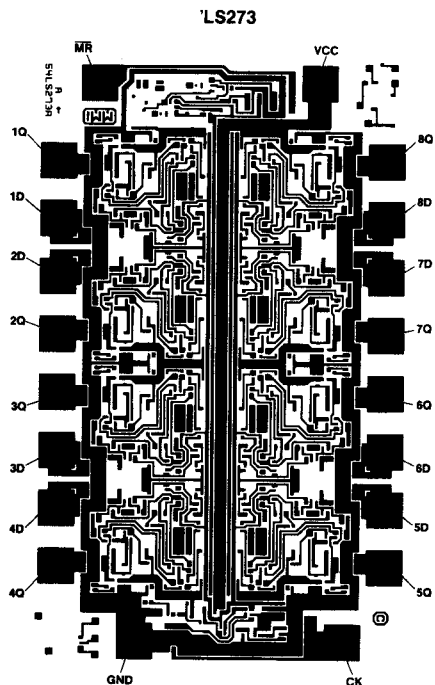


\* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

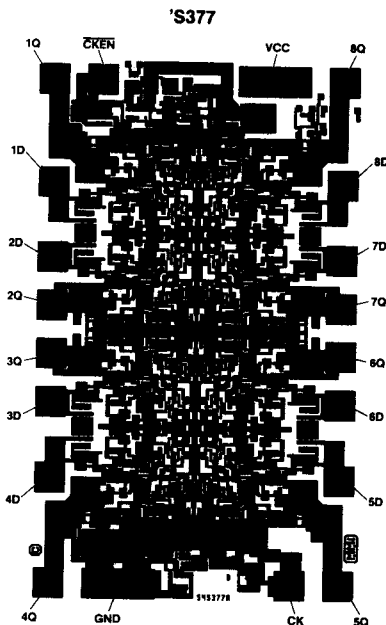
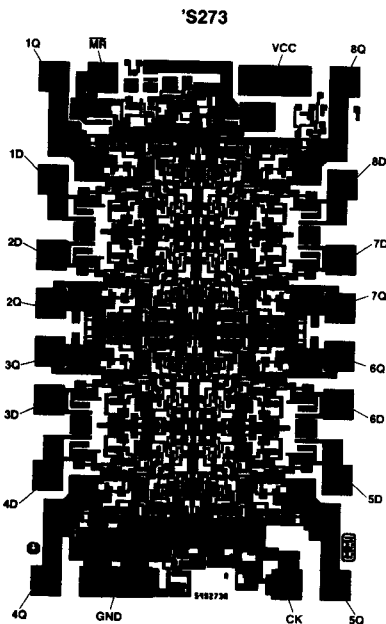
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. All diodes are 1N916 or 1N3064.
- C. For Series 54/74S,  $V_T = 1.5$  V.  
For Series 54/74LS,  $V_T = 1.3$  V.
- D. In the examples above the phase relationships between inputs and outputs have been chosen arbitrarily.
- E. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_{OUT} = 50\Omega$  and:  
For Series 54/74S,  $t_R \leq 2.5$  ns,  $t_P \leq 2.5$  ns.

Die Configurations



Die Size: 58x93 mil<sup>2</sup>



Die Size: 56x87 mil<sup>2</sup>

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