19-5400; Rev 3; 9/04

EVALUATION KIT AVAILABLE

10-Bit, 80Msps, Single 3.0V, Low-Power ADC with Internal Reference

General Description

The MAX1448 3V, 10-bit analog-to-digital converter (ADC) features a fully differential input, a pipelined 10-stage ADC architecture with wideband track-and-hold (T/H), and digital error correction incorporating a fully differential signal path. The ADC is optimized for low-power, high dynamic performance in imaging and digital communications applications. The converter operates from a single 2.7V to 3.6V supply, consuming only 120mW while delivering a 59dB (typ) signal-to-noise ratio (SNR) at a 20MHz input frequency. The fully differential input stage has a -3dB 400MHz bandwidth and may be operated with single-ended inputs. In addition to low operating power, the MAX1448 features a 5µA power-down mode for idle periods.

An internal 2.048V precision bandgap reference is used to set the ADC full-scale range. A flexible reference structure allows the user to supply a buffered, direct, or externally derived reference for applications requiring increased accuracy or a different input voltage range.

Lower speed, pin-compatible versions of the MAX1448 are also available. Refer to the MAX1444 data sheet for a 40Msps version and to the MAX1446 data sheet for a 60Msps version.

The MAX1448 has parallel, offset binary, CMOS-compatible three-state outputs that can be operated from 1.7V to 3.6V to allow flexible interfacing. The device is available in a 5mm x 5mm 32-pin TQFP package and is specified over the extended industrial (-40°C to +85°C) temperature range.

Applications

Ultrasound Imaging

CCD Imaging

Baseband and IF Digitization

Digital Set-Top Boxes

Video Digitizing Applications

Pin Configuration appears at end of data sheet.

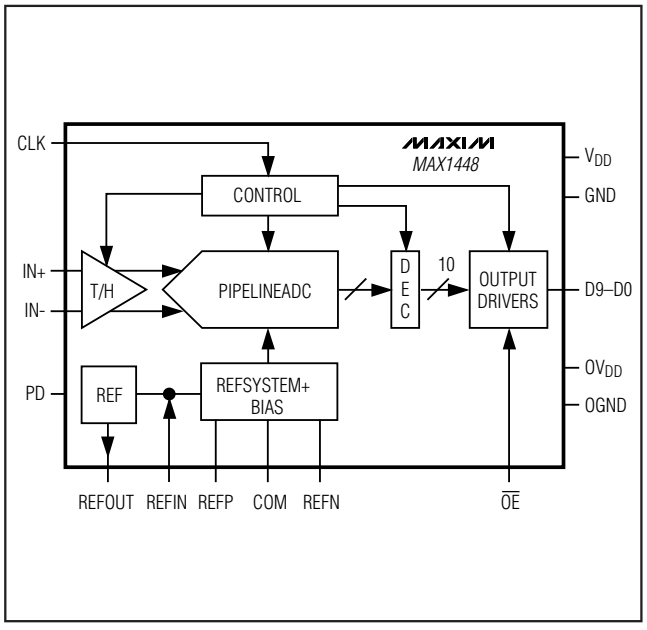
Features

- **Single 3.0V Operation**
- **Excellent Dynamic Performance**
  - **59dB SNR at f_{IN} = 20MHz**
  - **74dBc SFDR at f_{IN} = 20MHz**
- **Low Power**
  - **40mA (Normal Operation)**
  - **5µA (Shutdown Mode)**
- **Fully Differential Analog Input**
- **Wide $2V_{P-P}$ Differential Input Voltage Range**
- **400MHz -3dB Input Bandwidth**
- **On-Chip 2.048V Precision Bandgap Reference**
- **CMOS-Compatible Three-State Outputs**
- **32-Pin TQFP Package**
- **Evaluation Kit Available (MAX1448 EV Kit)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1448EHJ	-40°C to +85°C	32 TQFP

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

V_{DD}, OV_{DD} to GND .....-0.3V to +3.6V
OGND to GND.....-0.3V to +0.3V
IN+, IN- to GND.....-0.3V to V_{DD}
REFIN, REFOUT, REFP,
REFN, and COM to GND.....-0.3V to (V_{DD} + 0.3V)
$\overline{OE}$, PD, CLK to GND.....-0.3V to (V_{DD} + 0.3V)
D9–D0 to GND.....-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFP (derate 18.7mW/°C above +70°C).....1495.3mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.0V, OV_{DD} = 2V, 0.1µF and 1µF capacitors from REFP, REFN, and COM to GND, V_{REFIN} = 2.048V, REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential with respect to COM), C_L = 10pF at digital outputs, f_{CLK} = 83.3MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization; typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			10			Bits
Integral Nonlinearity	INL	f_{IN} = 7.47MHz, T_A ≥ +25°C		±0.7	±2.2	LSB
Differential Nonlinearity	DNL	f_{IN} = 7.47MHz, no missing codes		±0.4	±1.0	LSB
Offset Error				<±1	±1.7	%FS
Gain Error		T_A ≥ +25°C		0	±2	%FS
ANALOG INPUT						
Input Differential Range	V_{DIFF}	Differential or single-ended inputs		±1.0		V
Common-Mode Voltage Range	V_{COM}			V_{DD}/2 ± 0.5		V
Input Resistance	R_{IN}	Switched capacitor load		25		kΩ
Input Capacitance	C_{IN}			5		pF
CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}		80			MHz
Data Latency				5.5		Cycles
DYNAMIC CHARACTERISTICS (F_{CLK} = 83.3MHZ, 4096-POINT FFT)						
Signal-to-Noise Ratio	SNR	f_{IN} = 7.47MHz	56.5	59.1		dB
		f_{IN} = 20MHz	56	59		
		f_{IN} = 39.9MHz (Note 1)		58.5		
Signal-to-Noise + Distortion (Up to 5th Harmonic)	SINAD	f_{IN} = 7.47MHz	55.8	59		dB
		f_{IN} = 20MHz	55.3	58.8		
		f_{IN} = 39.9MHz (Note 1)		58		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.0V, OV_{DD} = 2V, 0.1µF and 1µF capacitors from REFP, REFN, and COM to GND, V_{REFIN} = 2.048V, REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential with respect to COM), C_L = 10pF at digital outputs, f_{CLK} = 83.3MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization; typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range	SFDR	f_{IN} = 7.47MHz	61	74		dBc
		f_{IN} = 20MHz	61	74		
		f_{IN} = 39.9MHz (Note 1)		73		
Third-Harmonic Distortion	HD3	f_{IN} = 7.47MHz		-74		dBc
		f_{IN} = 20MHz		-74		
		f_{IN} = 39.9MHz (Note 1)		-73		
Intermodulation Distortion Two-Tone	IMD_{TT}	f_1 = 24MHz at -6.5dB FS, f_2 = 26MHz at -6.5dB FS (Note 2)		-74		dBc
Third-Order Intermodulation Distortion	IM3	f_1 = 24MHz at -6.5dB FS, f_2 = 26MHz at -6.5dB FS (Note 2)		-74		dBc
Total Harmonic Distortion (First 5 Harmonics)	THD	f_{IN} = 7.47MHz		-72	-60	dBc
		f_{IN} = 20MHz		-70	-60	
		f_{IN} = 39.9MHz (Note 1)		-69		
Small-Signal Bandwidth		Input at -20dB FS, differential inputs		500		MHz
Full-Power Bandwidth	FPBW	Input at -0.5dB FS, differential inputs		400		MHz
Aperture Delay	t_{AD}			1		ns
Aperture Jitter	t_{AJ}			2		ps_{RMS}
Overdrive Recovery Time		For 1.5 × full-scale input		2		ns
Differential Gain				±1		%
Differential Phase				±0.25		Degrees
Output Noise		IN+ = IN- = COM		0.2		LSB_{RMS}
INTERNAL REFERENCE						
Reference Output Voltage	REFOUT			2.048 ±1%		V
Reference Temperature Coefficient	TC_{REF}			60		ppm/°C
Load Regulation				1.25		mV/mA
BUFFERED EXTERNAL REFERENCE (V_{REFIN} = 2.048V)						
REFIN Input Voltage	V_{REFIN}			2.048		
Positive Reference Output Voltage	V_{REFP}			2.012		V
Negative Reference Output Voltage	V_{REFN}			0.988		V
Common-Mode Level	V_{COM}			V_{DD} / 2		V
Differential Reference Output Voltage Range	ΔV_{REF}	ΔV_{REF} = V_{REFP} - V_{REFN}, T_A ≥ +25°C	0.98	1.024	1.07	V
REFIN Resistance	R_{REFIN}			>50		MΩ
Maximum REFP, COM Source Current	I_{SOURCE}			5		mA

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.0V, OV_{DD} = 2V, 0.1µF and 1µF capacitors from REFP, REFN, and COM to GND, V_{REFIN} = 2.048V, REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential with respect to COM), C_L = 10pF at digital outputs, f_{CLK} = 83.3MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization; typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum REFP, COM Sink Current	I_{SINK}			-250		µA
Maximum REFN Source Current	I_{SOURCE}			250		µA
Maximum REFN Sink Current	I_{SINK}			-5		mA
UNBUFFERED EXTERNAL REFERENCE (V_{REFIN} = AGND, reference voltage applied to REFP, REFN, and COM)						
REFP, REFN Input Resistance	R_{REFP}, R_{REFN}	Measured between REFP and COM and REFN and COM		4		kΩ
REFP, REFN, COM Input Capacitance	C_{IN}			15		pF
Differential Reference Input Voltage Range	ΔV_{REF}	$\Delta V_{REF} = V_{REFP} - V_{REFN}$		1.024 ± 10%		V
COM Input Voltage Range	V_{COM}			V_{DD} / 2 ± 10%		V
REFP Input Voltage	V_{REFP}			V_{COM}+ ΔV_{REF} / 2		V
REFN Input Voltage	V_{REFN}			V_{COM} - ΔV_{REF} / 2		V
DIGITAL INPUTS (CLK, PD, $\overline{OE}$)						
Input High Threshold	V_{IH}	CLK	0.8 x V_{DD}			V
		PD, $\overline{OE}$	0.8 x OV_{DD}			
Input Low Threshold	V_{IL}	CLK			0.2 x OV_{DD}	V
		PD, $\overline{OE}$			0.2 x OV_{DD}	
Input Capacitance	C_{IN}			5		pF
Input Hysteresis	V_{HYST}			0.1		V
Input Leakage	I_{IH}	$V_{IH} = V_{DD} = 0V_{DD}$			±5	µA
	I_{IL}	V_{IL} = 0			±5	
DIGITAL OUTPUTS (D9–D0)						
Output Voltage Low	V_{OL}	I_{SINK} = 200µA			0.2	V
Output Voltage High	V_{OH}	I_{SOURCE} = 200µA	OV_{DD} - 0.2			V
Three-State Leakage Current	I_{LEAK}	$\overline{OE} = OV_{DD}$			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{OE} = OV_{DD}$		5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.0V, OV_{DD} = 2V, 0.1µF and 1µF capacitors from REFP, REFN, and COM to GND, V_{REFIN} = 2.048V, REFOUT connected to REFIN through a 10kΩ resistor, V_{IN} = $2V_{P-P}$ (differential with respect to COM), C_L = 10pF at digital outputs, f_{CLK} = 83.3MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥ +25°C guaranteed by production test, < +25°C guaranteed by design and characterization; typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		2.7	3.0	3.6	V
Output Supply Voltage	OV_{DD}		1.7	3.0	3.6	V
Analog Supply Current	I_{VDD}	Operating, f_{IN} = 20MHz at -0.5dB FS		40	47	mA
		Shutdown, clock idle, PD = $\overline{OE}$ = OV_{DD}		4	15	µA
Output Supply Current	I_{OVDD}	Operating, C_L = 15pF, f_{IN} = 20MHz at -0.5dB FS		8		mA
		Shutdown, clock idle, PD = $\overline{OE}$ = OV_{DD}		1	20	µA
Power-Supply Rejection	PSRR	Offset		±0.2		mV/V
		Gain		±0.1		%/V
TIMING CHARACTERISTICS						
CLK Rise to Output Data Valid	t_{DO}	Figure 6 (Note 3)		5	8	ns
$\overline{OE}$ Fall to Output Enable	t_{ENABLE}	Figure 5		10		ns
$\overline{OE}$ Rise to Output Disable	$t_{DISABLE}$	Figure 5		15		ns
CLK Pulse Width High	t_{CH}	Figure 6, clock period 12ns		6±1		ns
CLK Pulse Width Low	t_{CL}	Figure 6, clock period 12ns		6±1		ns
Wake-Up Time	t_{WAKE}	(Note 4)		1.5		µs

Note 1: SNR, SINAD, THD, SFDR, and HD3 are based on an analog input voltage of -0.5dB FS referenced to a 1.024V full-scale input voltage range.

Note 2: Intermodulation distortion is the total power of the intermodulation products relative to the individual carrier. This number is 6dB better if referenced to the two-tone envelope.

Note 3: Digital outputs settle to V_{IH},V_{IL}.

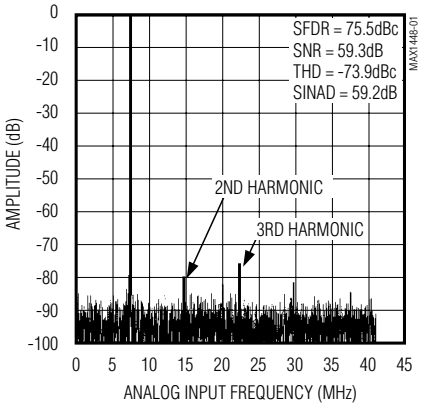
Note 4: With REFIN driven externally, REFP, COM, and REFN are left floating while powered down.

10-Bit, 80Msps, Single 3.0V, Low-Power ADC with Internal Reference

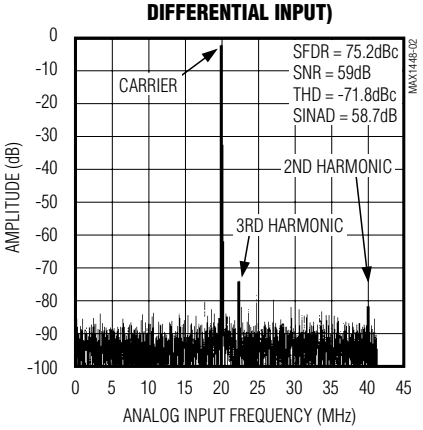
Typical Operating Characteristics

(V_{DD} = 3.0V, OV_{DD} = 2.7V, internal reference, differential input at -0.5dB FS, f_{CLK} = 83.3MHz, $C_L \approx$ 10pF, T_A = +25°C, unless otherwise noted.)

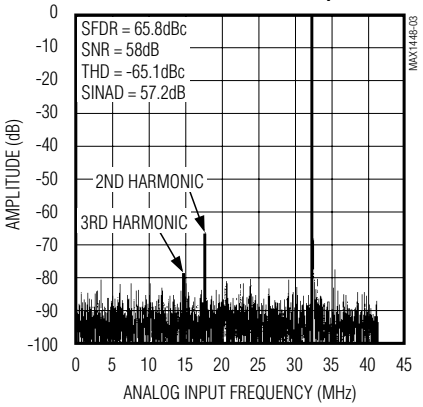
FFT PLOT (f_{IN} = 7.5MHz, 8192-POINT FFT, DIFFERENTIAL INPUT)



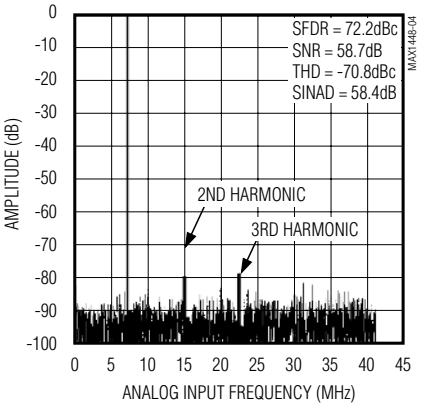
FFT PLOT (f_{IN} = 20MHz, 8192-POINT FFT, DIFFERENTIAL INPUT)



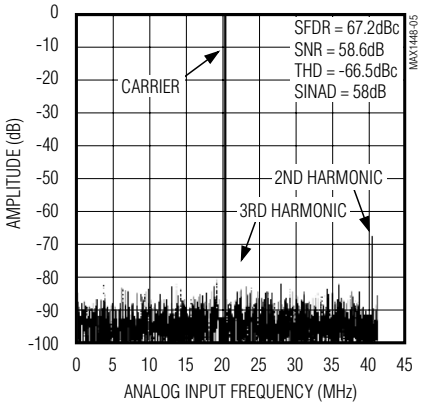
UNDERSAMPLING FFT PLOT (f_{IN} = 50MHz, 8192-POINT FFT, DIFFERENTIAL INPUT)



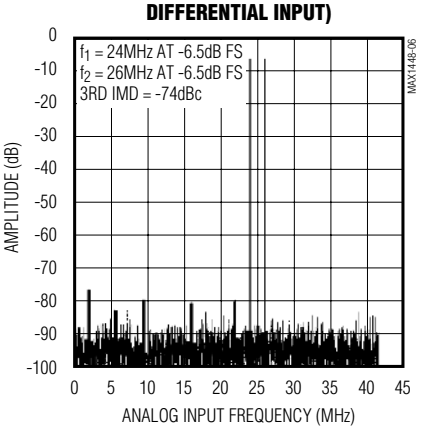
FFT PLOT (f_{IN} = 7.5MHz, 8192-POINT FFT, SINGLE-ENDED INPUT)



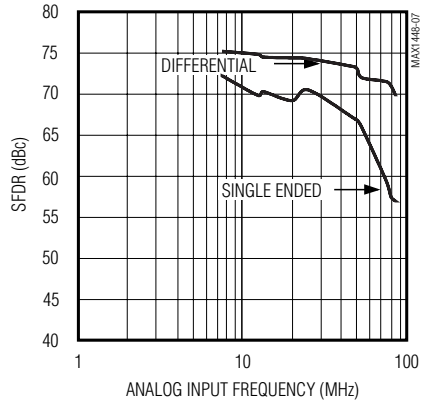
FFT PLOT (f_{IN} = 20MHz, 8192-POINT FFT, SINGLE-ENDED INPUT)



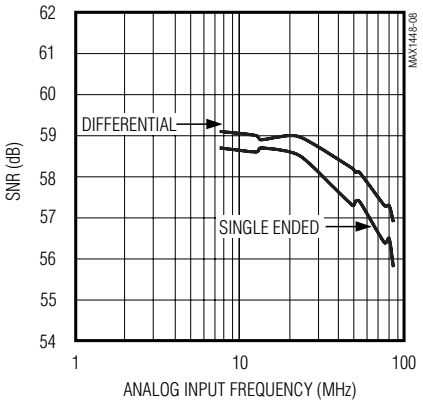
TWO-TONE INTERMODULATION (8192-POINT IMD, DIFFERENTIAL INPUT)



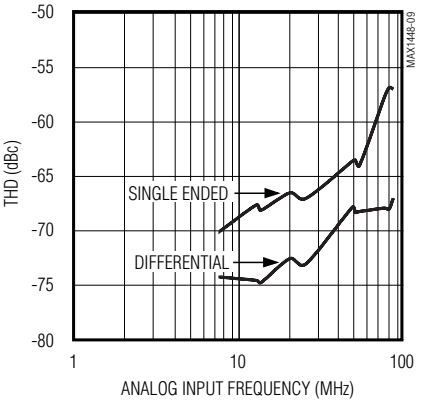
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



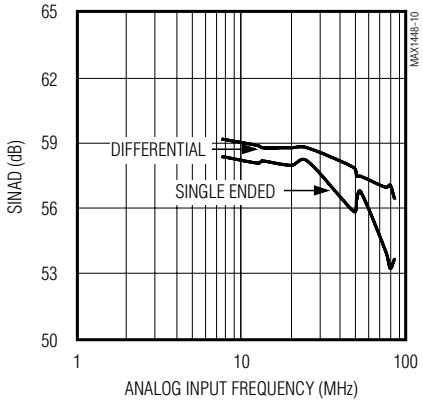
TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



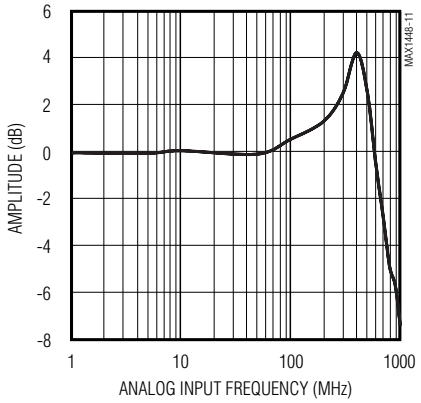
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 2.7V, internal reference, differential input at -0.5dB FS, f_{CLK} = 83.3MHz, $C_L \approx$ 10pF, T_A = +25°C, unless otherwise noted.)

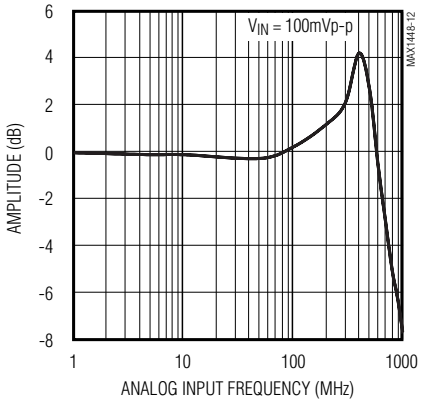
SIGNAL-TO-NOISE + DISTORTION vs. ANALOG INPUT FREQUENCY



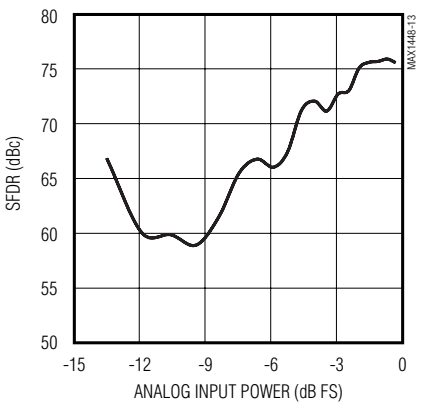
FULL-POWER INPUT BANDWIDTH vs. ANALOG INPUT FREQUENCY (SINGLE-ENDED)



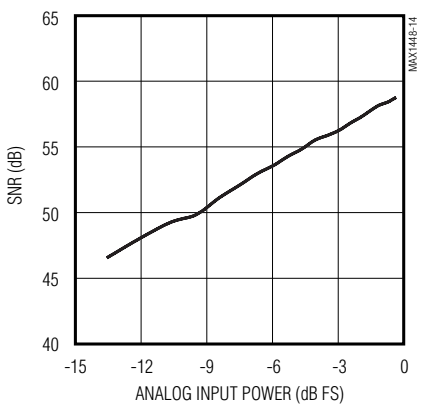
SMALL-SIGNAL INPUT BANDWIDTH vs. ANALOG INPUT FREQUENCY (SINGLE-ENDED)



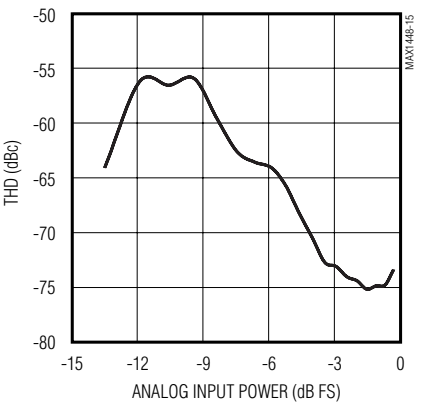
SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT POWER (f_{IN} = 20MHz)



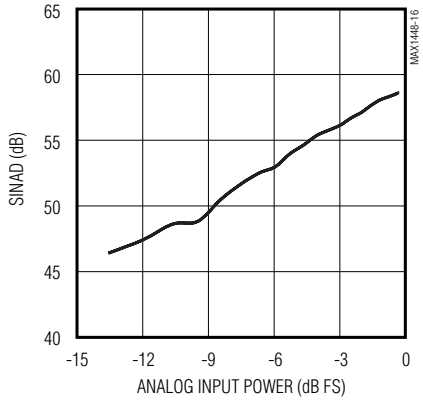
SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT POWER (f_{IN} = 20MHz)



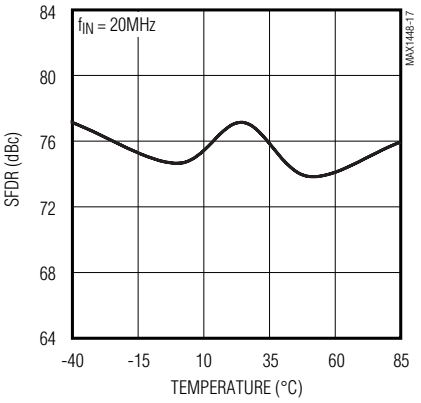
TOTAL HARMONIC DISTORTION vs. ANALOG INPUT POWER (f_{IN} = 20MHz)



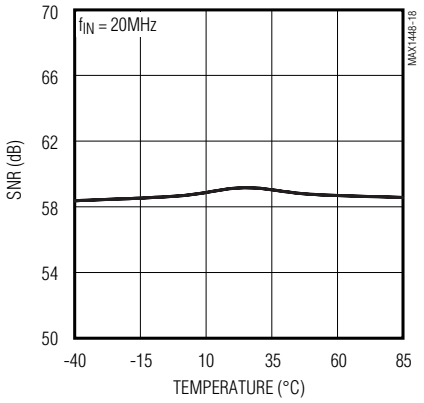
SIGNAL-TO-NOISE + DISTORTION vs. ANALOG INPUT POWER (f_{IN} = 20MHz)



SPURIOUS-FREE DYNAMIC RANGE vs. TEMPERATURE



SIGNAL-TO-NOISE RATIO vs. TEMPERATURE

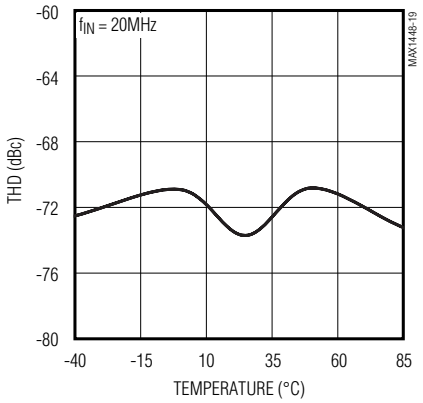


10-Bit, 80Msps, Single 3.0V, Low-Power ADC with Internal Reference

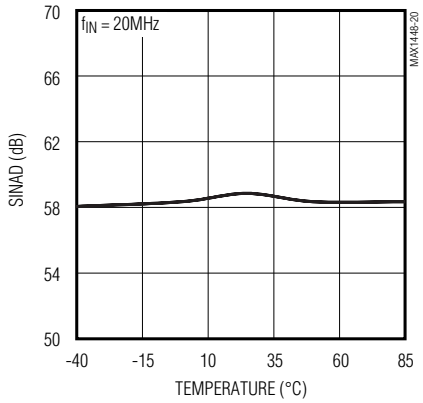
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 2.7V, internal reference, differential input at -0.5dB FS, f_{CLK} = 83.3MHz, $C_L \approx$ 10pF, T_A = +25°C, unless otherwise noted.)

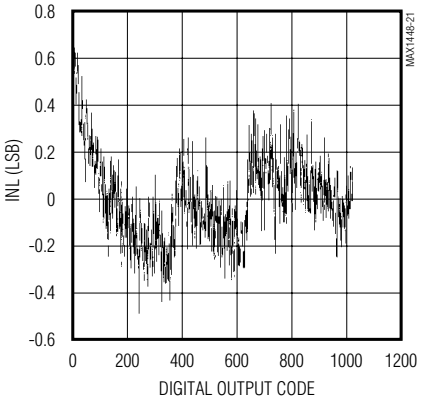
TOTAL HARMONIC DISTORTION vs. TEMPERATURE



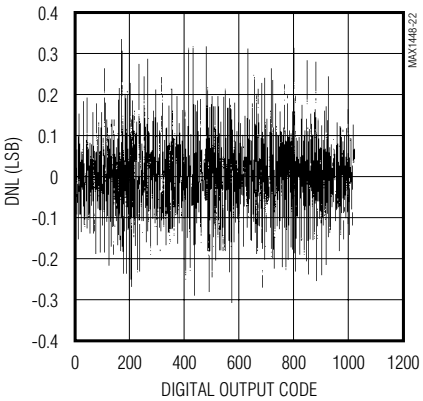
SIGNAL-TO-NOISE + DISTORTION vs. TEMPERATURE



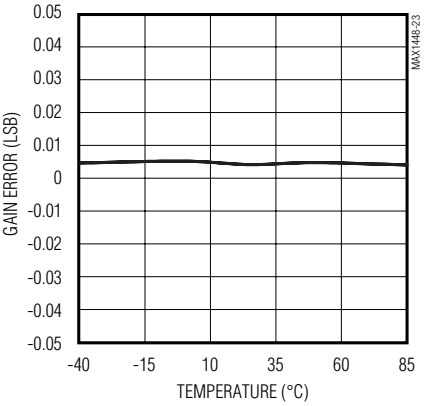
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE (BEST STRAIGHT LINE)



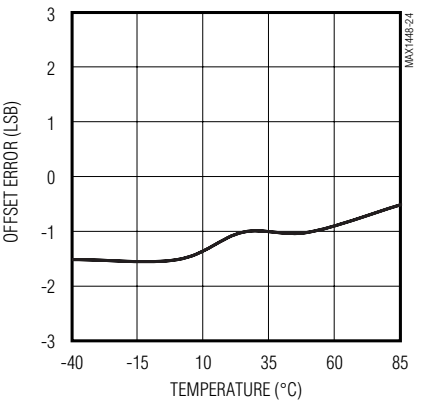
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



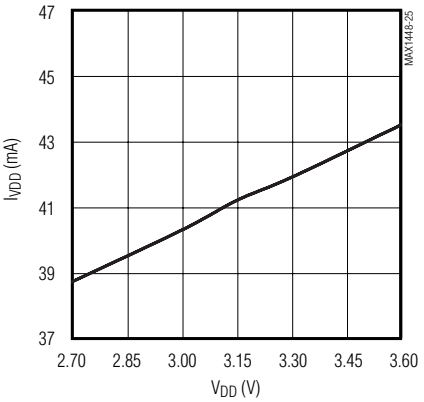
GAIN ERROR vs. TEMPERATURE EXTERNAL REFERENCE (V_{REFIN} = 2.048V)



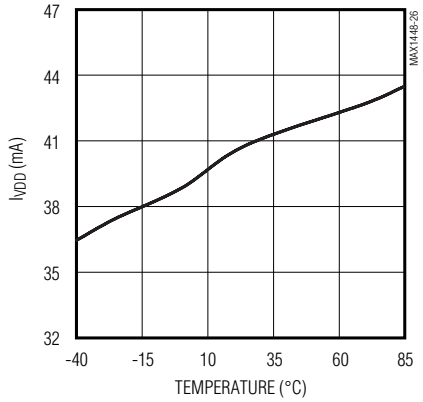
OFFSET ERROR vs. TEMPERATURE, EXTERNAL REFERENCE (V_{REFIN} = 2.048V)



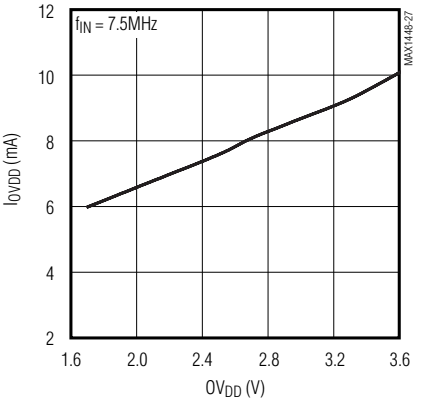
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



ANALOG SUPPLY CURRENT vs. TEMPERATURE



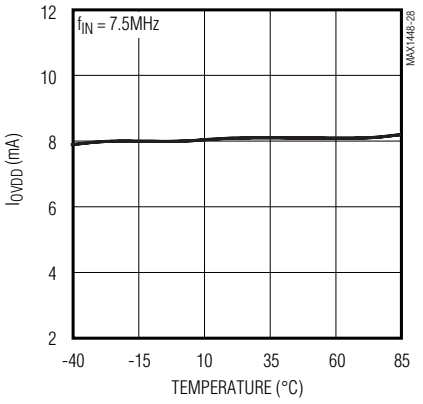
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



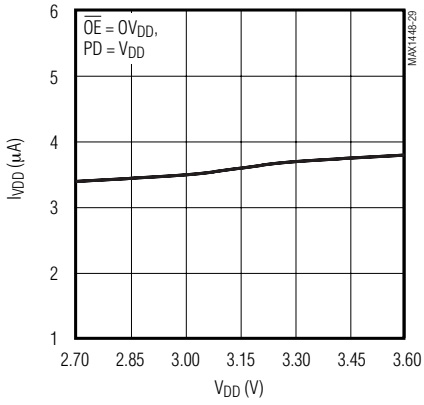
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, OV_{DD} = 2.7V, internal reference, differential input at -0.5dB FS, f_{CLK} = 83.3MHz, C_L ≈ 10pF, T_A = +25°C, unless otherwise noted.)

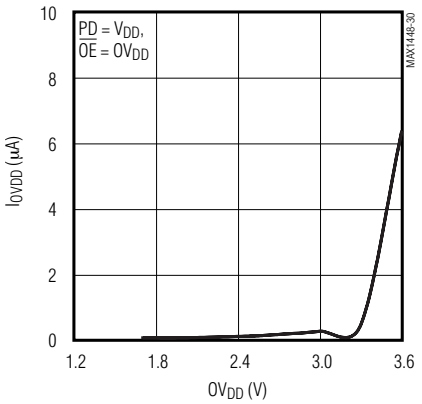
DIGITAL SUPPLY CURRENT vs. TEMPERATURE



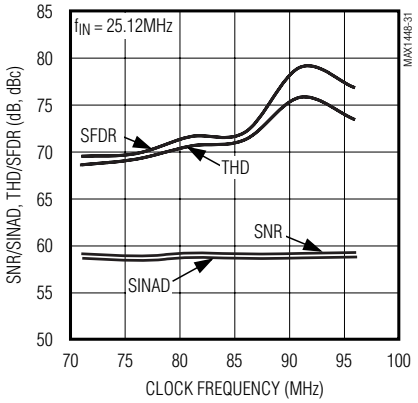
ANALOG POWER-DOWN CURRENT vs. ANALOG POWER SUPPLY



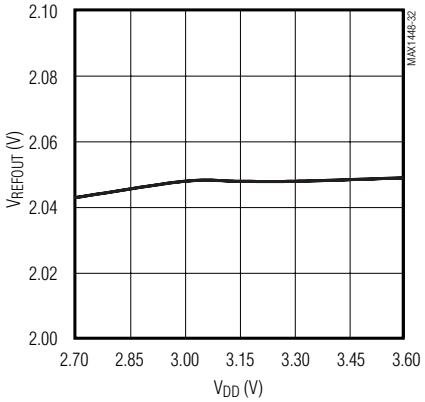
DIGITAL POWER-DOWN CURRENT vs. DIGITAL POWER SUPPLY



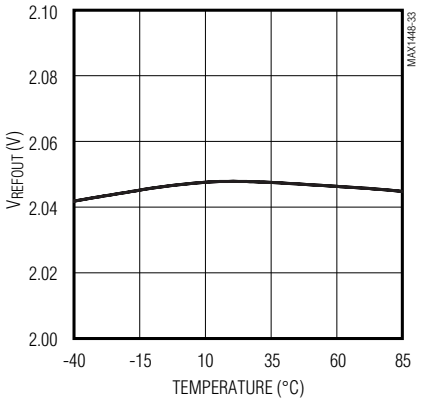
SNR/SINAD, THD/SFDR vs. CLOCK FREQUENCY



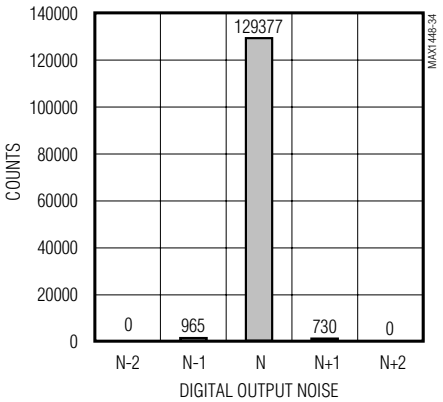
INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



OUTPUT NOISE HISTOGRAM (DC INPUT)



10-Bit, 80Msps, Single 3.0V, Low-Power ADC with Internal Reference

Pin Description

PIN	NAME	FUNCTION
1	REFN	Lower Reference. Conversion range is ±(V_{REFP} - V_{REFN}). Bypass to GND with a >0.1µF capacitor.
2	COM	Common-Mode Voltage Output. Bypass to GND with a >0.1µF capacitor.
3, 9, 10	V_{DD}	Analog Supply Voltage. Bypass to GND with a capacitor combination of 2.2µF in parallel with 0.1µF.
4, 5, 8, 11, 14, 30	GND	Analog Ground
6	IN+	Positive Analog Input. For single-ended operation, connect signal source to IN+.
7	IN-	Negative Analog Input. For single-ended operation, connect IN- to COM.
12	CLK	Conversion Clock Input
13	PD	Power-Down Input High: power-down mode Low: normal operation
15	$\overline{OE}$	Output Enable Input High: digital outputs disabled Low: digital outputs enabled
16–20	D9–D5	Three-State Digital Outputs D9–D5. D9 is the MSB.
21	OV_{DD}	Output Driver Supply Voltage. Bypass to GND with a capacitor combination of 2.2µF in parallel with 0.1µF.
22	T.P.	Test Point. **Do not connect.**
23	OGND	Output Driver Ground
24–28	D4–D0	Three-State Digital Outputs D4–D0. D0 is the LSB.
29	REFOUT	Internal Reference Voltage Output. May be connected to REFIN through a resistor or a resistor-divider.
31	REFIN	Reference Input. $V_{REFIN} = 2 \times (V_{REFP} - V_{REFN})$. Bypass to GND with a >0.1µF capacitor.
32	REFP	Upper Reference. Conversion range is ±(V_{REFP} - V_{REFN}). Bypass to GND with a >0.1µF capacitor.

Detailed Description

The MAX1448 uses a 10-stage, fully differential, pipelined architecture (Figure 1) that allows for high-speed conversion while minimizing power consumption. Each sample moves through a pipeline stage every half clock-cycle. Counting the delay through the output latch, the clock-cycle latency is 5.5.

A 1.5-bit (2-comparator) flash ADC converts the held input voltage into a digital code. The following digital-to-analog converter (DAC) converts the digitized result back into an analog voltage, which is then subtracted from the original held input signal. The resulting error signal is then multiplied by two, and the product is passed along to the next pipeline stage where the process is repeated. Each stage provides a 1-bit resolution. Digital error correction compensates for ADC comparator offsets in each pipeline stage and ensures no missing codes.

Input Track-and-Hold Circuit

Figure 2 displays a simplified functional diagram of the input track-and-hold (T/H) circuit in both track and hold mode. In track mode, switches S1, S2a, S2b, S4a, S4b, S5a, and S5b are closed. The fully differential circuit samples the input signal onto the two capacitors (C2a and C2b) through S4a and S4b. S2a and S2b set the common mode for the amplifier input and open simultaneously with S1, sampling the input waveform. S4a and S4b are then opened before S3a and S3b connect capacitors C1a and C1b to the amplifier output, and S4c is closed. The resulting differential voltage is held on C2a and C2b. The amplifier is used to charge C1a and C1b to the same values originally held on C2a and C2b. This value is then presented to the first-stage quantizer and isolates the pipeline from the fast-changing input. The wide-input-bandwidth T/H amplifier allows the MAX1448 to track and sample/hold analog inputs of high frequencies beyond Nyquist. Analog inputs (IN+ and IN-) can be driven either differentially or single-ended. It is recommended to match the impedance of IN+ and IN- and set the common-mode voltage to midsupply ($V_{DD}/2$) for optimum performance.

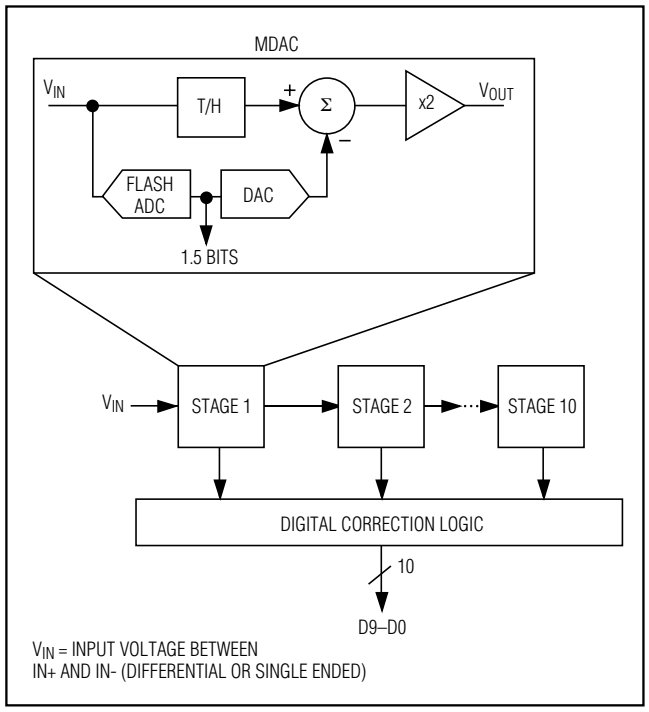


Figure 1. Pipelined Architecture—Stage Blocks

Analog Input and Reference Configuration

The MAX1448 full-scale range is determined by the internally generated voltage difference between REFP ($V_{DD}/2 + V_{REFIN}/4$) and REFN ($V_{DD}/2 - V_{REFIN}/4$). The ADC's full-scale range is user-adjustable through the REFIN pin, which provides a high input impedance for this purpose. REFOUT, REFP, COM ($V_{DD}/2$), and REFN are internally buffered, low-impedance outputs.

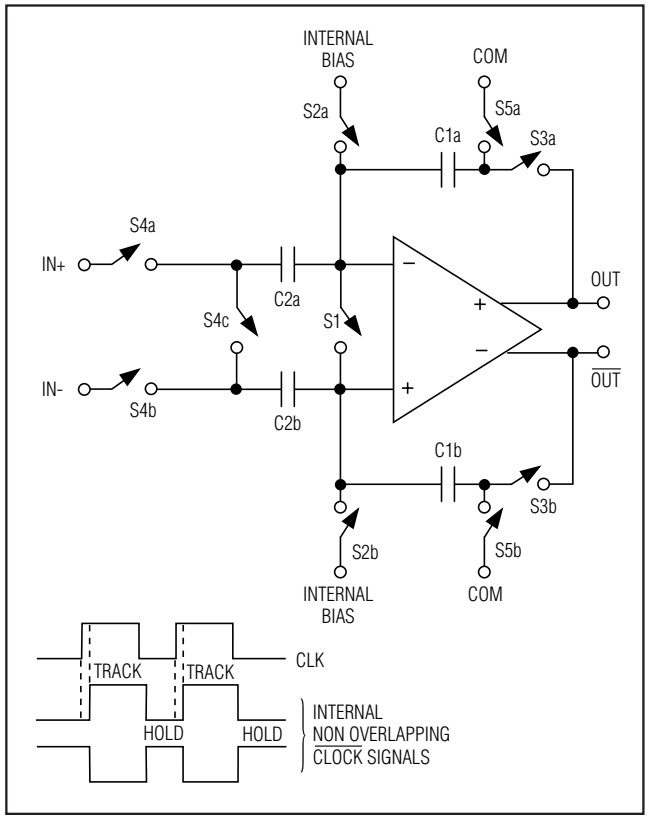


Figure 2. Internal Track-and-Hold Circuit

10-Bit, 80Msps, Single 3.0V, Low-Power ADC with Internal Reference

The MAX1448 provides three modes of reference operation:

- Internal reference mode
- Buffered external reference mode
- Unbuffered external reference mode

In internal reference mode, the internal reference output (REFOUT) can be tied to the REFIN pin through a resistor (e.g., 10kΩ) or resistor-divider if an application requires a reduced full-scale range. For stability purposes, it is recommended to bypass REFIN with a >10nF capacitor to GND.

In buffered external reference mode, the reference voltage levels can be adjusted externally by applying a stable and accurate voltage at REFIN. In this mode, REFOUT may be left open or connected to REFIN through a >10kΩ resistor.

In unbuffered external reference mode, REFIN is connected to GND, thereby deactivating the on-chip buffers of REFP, COM, and REFN. With their buffers shut down, these pins become high impedance and can be driven by external reference sources.

Clock Input (CLK)

The MAX1448 CLK input accepts CMOS-compatible clock signals. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (<2ns). In particular, sampling occurs on the falling edge of the clock signal, mandating this edge to provide lowest possible jitter. Any significant aperture jitter would limit the SNR performance of the ADC as follows:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times f_{IN} \times t_{AJ}}\right)$$

where f_{IN} represents the analog input frequency, and t_{AJ} is the time of the aperture jitter.

Clock jitter is especially critical for undersampling applications. The clock input should always be considered as an analog input and routed away from any analog input or other digital signal lines.

The MAX1448 clock input operates with a voltage threshold set to $V_{DD}/2$. Clock inputs with a duty cycle other than 50% must meet the specifications for high and low periods as stated in the *Electrical Characteristics*. See Figures 3a, 3b, 4a, and 4b for the relationship between spurious-free dynamic range (SFDR), signal-to-noise ratio (SNR), total harmonic distortion (THD), or signal-to-noise plus distortion (SINAD) versus duty cycle.

Output Enable ($\overline{OE}$), Power Down (PD), and Output Data (D0–D9)

All data outputs, D0 (LSB) through D9 (MSB), are TTL/CMOS-logic compatible. There is a 5.5 clock-cycle latency between any particular sample and its valid output data. The output coding is straight offset binary (Table 1). With $\overline{OE}$ and PD high, the digital outputs enter a high-impedance state. If $\overline{OE}$ is held low with PD high, the outputs are latched at the last value prior to the power down.

The capacitive load on the digital outputs D0–D9 should be kept as low as possible (<15pF) to avoid large digital currents that could feed back into the analog portion of the MAX1448, degrading its dynamic performance. Using buffers on the ADC's digital outputs can further isolate the digital outputs from heavy capacitive loads. To further improve the MAX1448's dynamic performance, small series resistors (e.g., 100Ω) may be added to the digital output paths, close to the ADC.

Figure 5 displays the timing relationship between output enable and data output valid as well as power-down/wake-up and data output valid.

Table 1. MAX1448 Output Code for Differential Inputs

DIFFERENTIAL INPUT VOLTAGE*	DIFFERENTIAL INPUT	STRAIGHT OFFSET BINARY
$V_{REF} \times 511/512$	+Full Scale -1LSB	11 1111 1111
$V_{REF} \times 510/512$	+Full Scale -2LSB	11 1111 1110
$V_{REF} \times 1/512$	+1LSB	10 0000 0001
0	Bipolar Zero	10 0000 0000
$- V_{REF} \times 1/512$	-1LSB	01 1111 1111
$- V_{REF} \times 511/512$	Negative Full Scale + 1LSB	00 0000 0001
$- V_{REF} \times 512/512$	Negative Full Scale	00 0000 0000

*$V_{REF} = V_{REFP} = V_{REFN}$

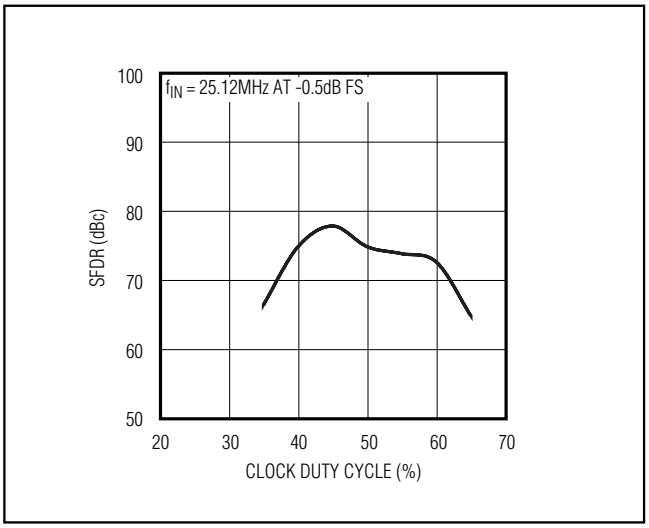


Figure 3a. Spurious Free Dynamic Range vs. Clock Duty Cycle (Differential Input)

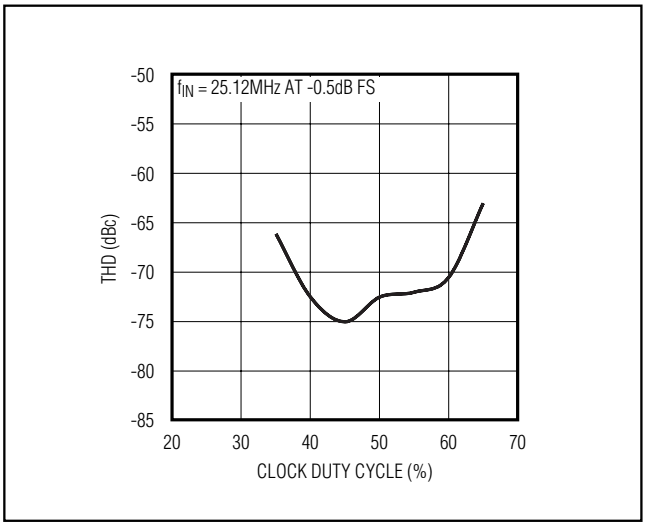


Figure 4a. Total Harmonic Distortion vs. Clock Duty Cycle (Differential Input)

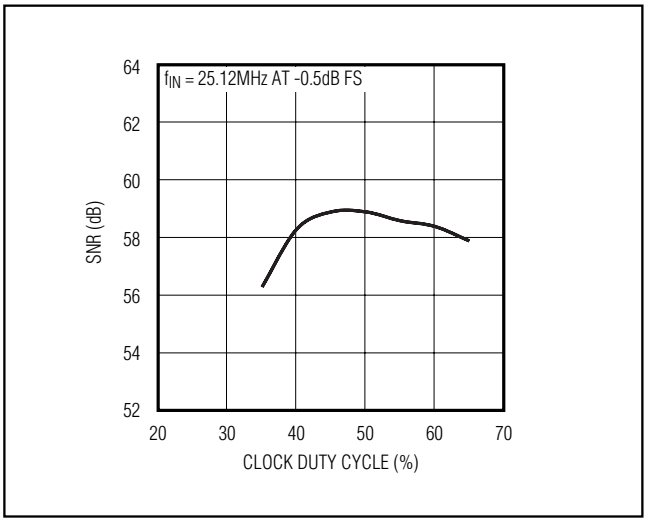


Figure 3b. Signal-to-Noise Ratio vs. Clock Duty Cycle (Differential Input)

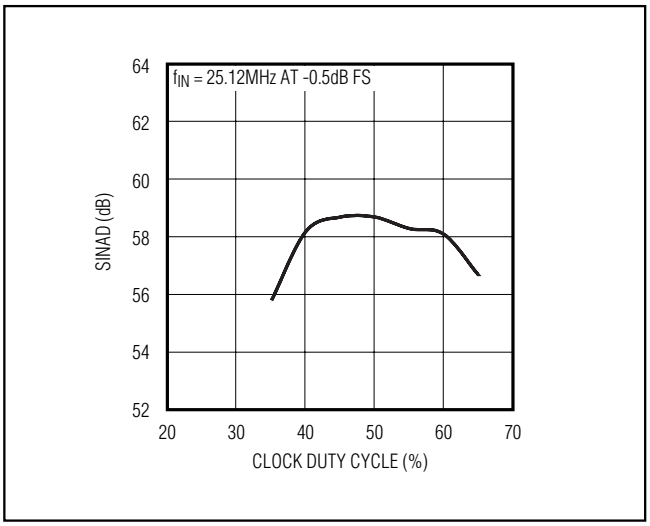


Figure 4b. Signal-to-Noise Plus Distortion vs. Clock Duty Cycle (Differential Input)

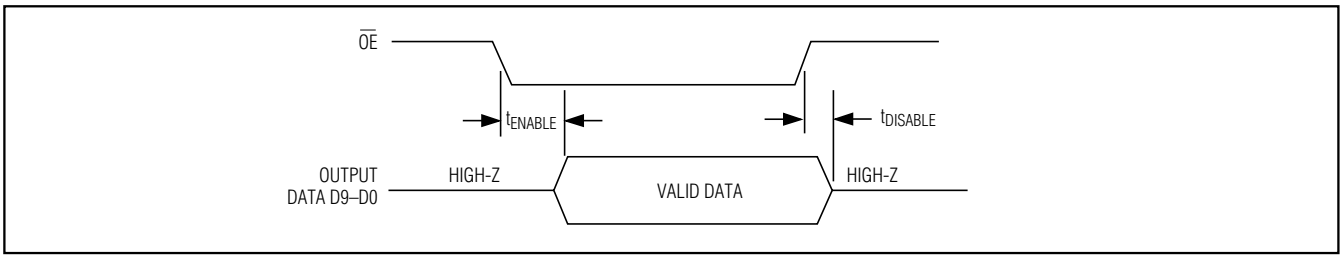


Figure 5. Output Enable Timing

10-Bit, 80Msps, Single 3.0V, Low-Power ADC with Internal Reference

System Timing Requirements

Figure 6 shows the relationship between the clock input, analog input, and data output. The MAX1448 samples at the falling edge of the input clock. Output data is valid on the rising edge of the input clock. The output data has an internal latency of 5.5 clock cycles. Figure 6 also shows the relationship between the input clock parameters and the valid output data.

Applications Information

Figure 7 shows a typical application circuit containing a single-ended to differential converter. The internal reference provides a $V_{DD}/2$ output voltage for level shifting purposes. The input is buffered and then split to a voltage follower and inverter. A lowpass filter follows the op amps to suppress some of the wideband noise associated with high-speed op amps. The user may select the R_{ISO} and C_{IN} values to optimize the filter performance to suit a particular application. For the application in Figure 7, an RISO of 50Ω is placed before the capacitive load to prevent ringing and oscillation. The 22pF C_{IN} capacitor acts as a small bypassing capacitor.

Using Transformer Coupling

An RF transformer (Figure 8) provides an excellent solution for converting a single-ended source signal to a fully differential signal, required by the MAX1448 for optimum performance. Connecting the transformer's center tap to COM provides a $V_{DD}/2$ DC level shift to the input. Although a 1:1 transformer is shown, a step-up transformer may be selected to reduce the drive requirements. A reduced signal swing from the input driver, such as an op amp, may also improve the overall distortion.

In general, the MAX1448 provides better SFDR and THD with fully differential input signals than single-ended drive, especially for very high input frequencies. In differential input mode, even-order harmonics are lower since both inputs (IN+, IN-) are balanced, and each of the inputs only requires half the signal swing compared to single-ended mode.

Single-Ended AC-Coupled Input Signal

Figure 9 shows an AC-coupled, single-ended application. The MAX4108 op amp provides high speed, high bandwidth, low noise, and low distortion to maintain the integrity of the input signal.

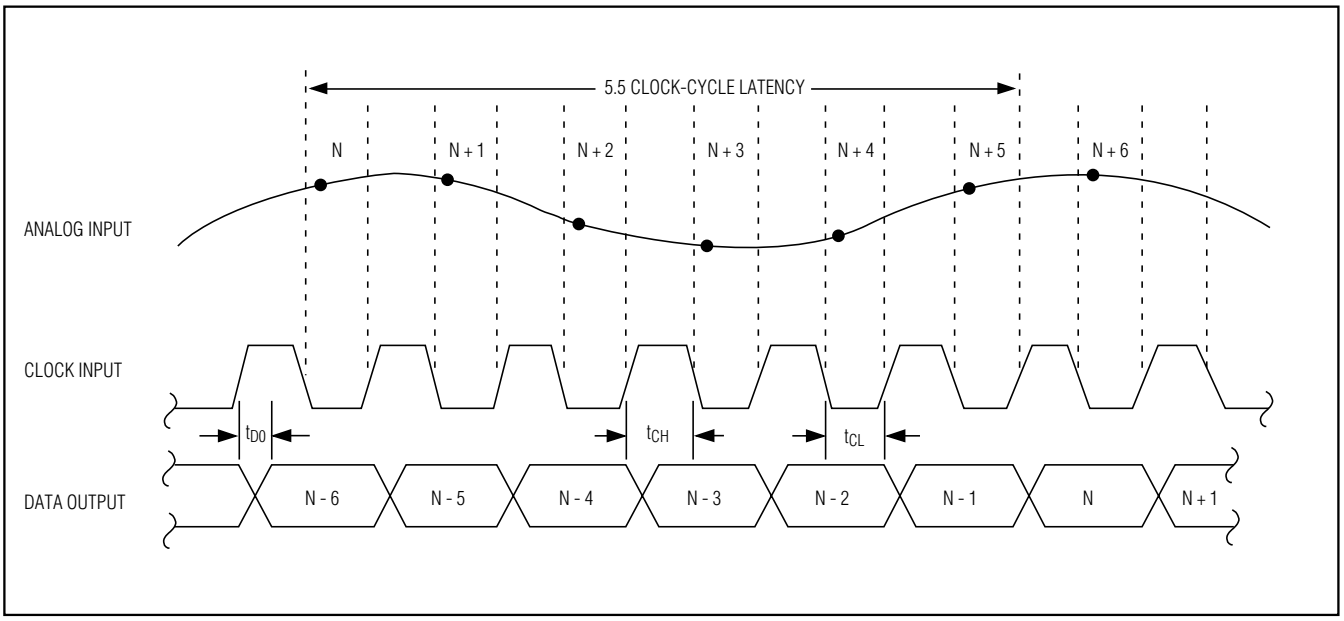


Figure 6. System and Output Timing Diagram

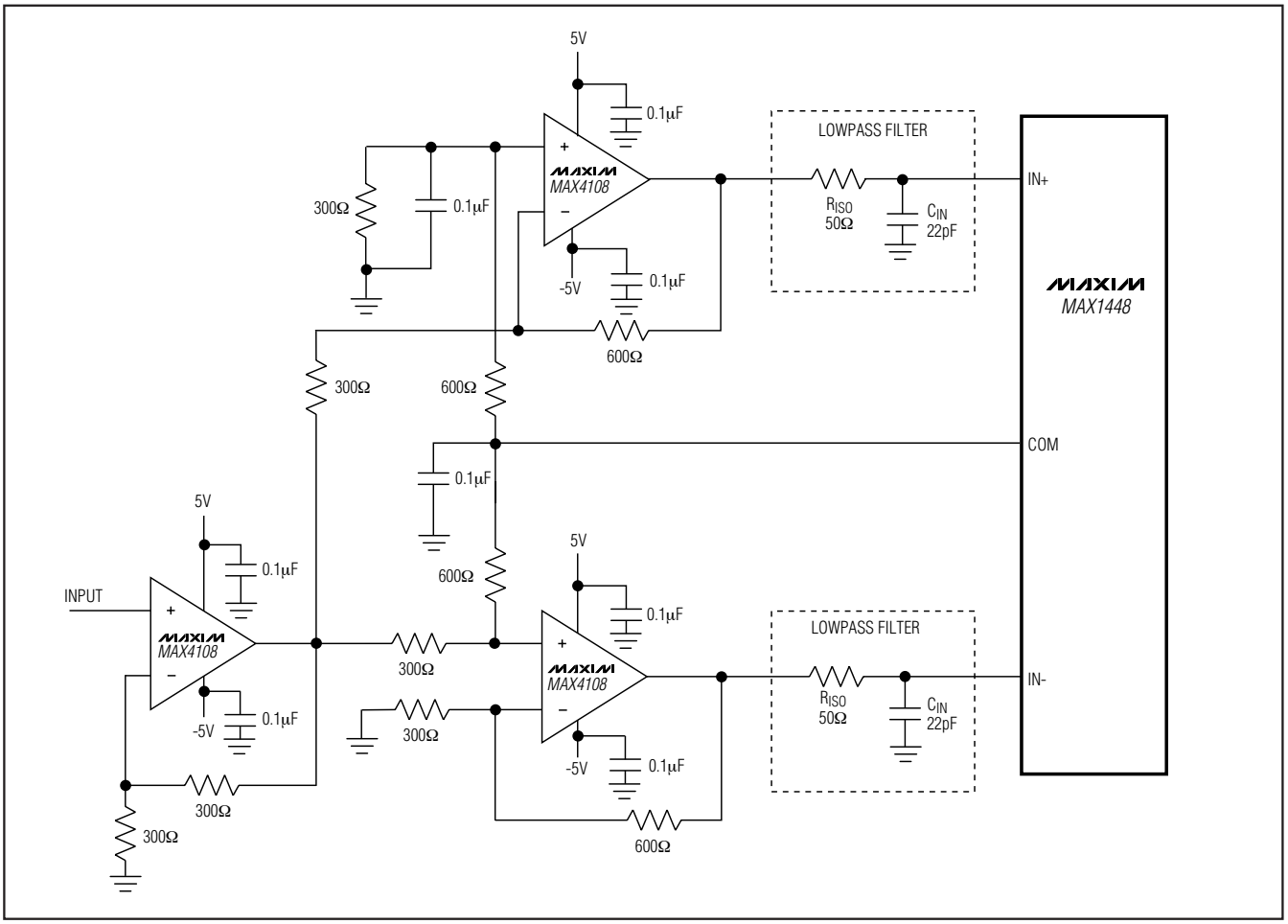


Figure 7. Typical Application Circuit Using the Internal Reference

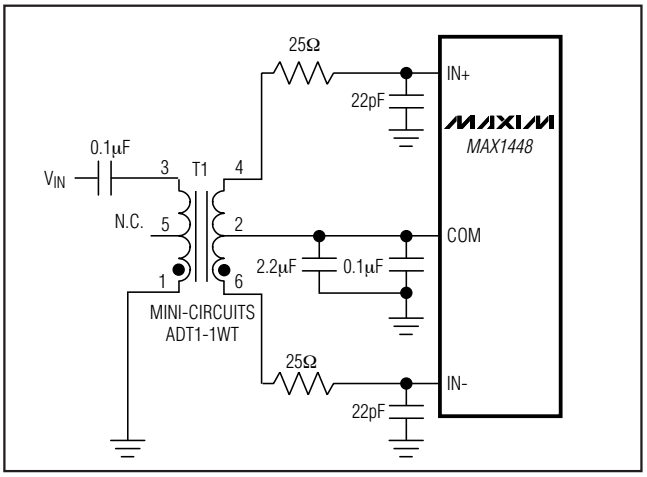


Figure 8. Using a Transformer for AC-Coupling

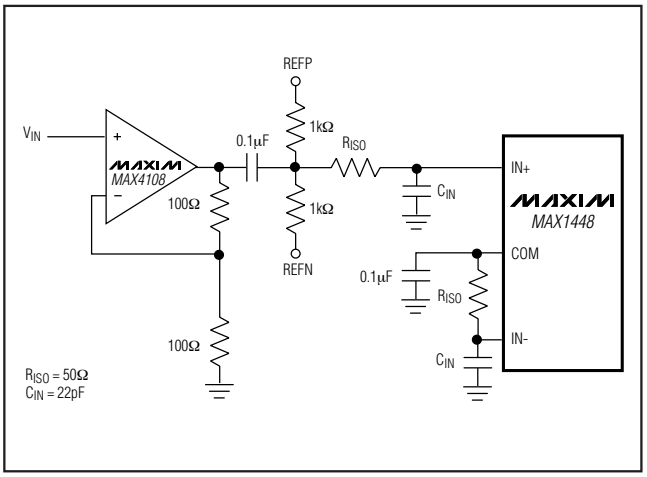
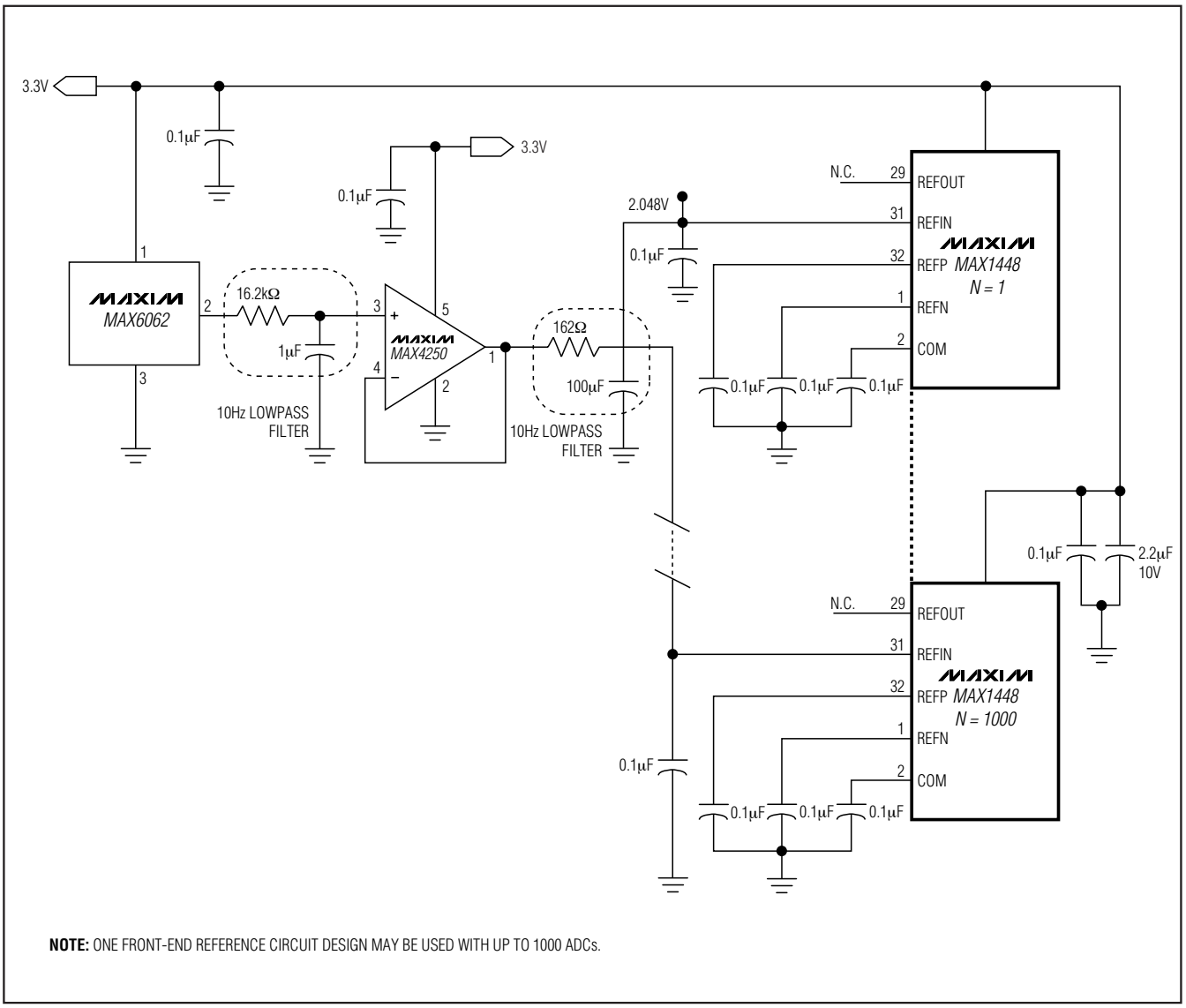


Figure 9. Single-Ended AC-Coupled Input

10-Bit, 80Msps, Single 3.0V, Low-Power ADC with Internal Reference



NOTE: ONE FRONT-END REFERENCE CIRCUIT DESIGN MAY BE USED WITH UP TO 1000 ADCs.

Figure 10. Buffered External Reference Drives Up to 1000 ADCs

Buffered External Reference Drives Multiple ADCs

Multiple-converter systems based on the MAX1448 are well suited for use with a common reference voltage. The REFIN pin of those converters can be connected directly to an external reference source. A precision bandgap reference like the MAX6062 generates an external DC level of 2.048V (Figure 10), and exhibits a noise voltage density of 150nV/√Hz. Its output passes through a 1-pole lowpass filter (with 10Hz cutoff frequency) to the MAX4250, which buffers the reference before its output is applied to a second 10Hz lowpass filter. The MAX4250 provides a low offset voltage (for high-gain accuracy) and a low noise level. The passive 10Hz filter following the buffer attenuates noise produced in the voltage reference and buffer stages. This filtered noise density, which decreases for higher frequencies, meets the noise levels specified for precision ADC operation.

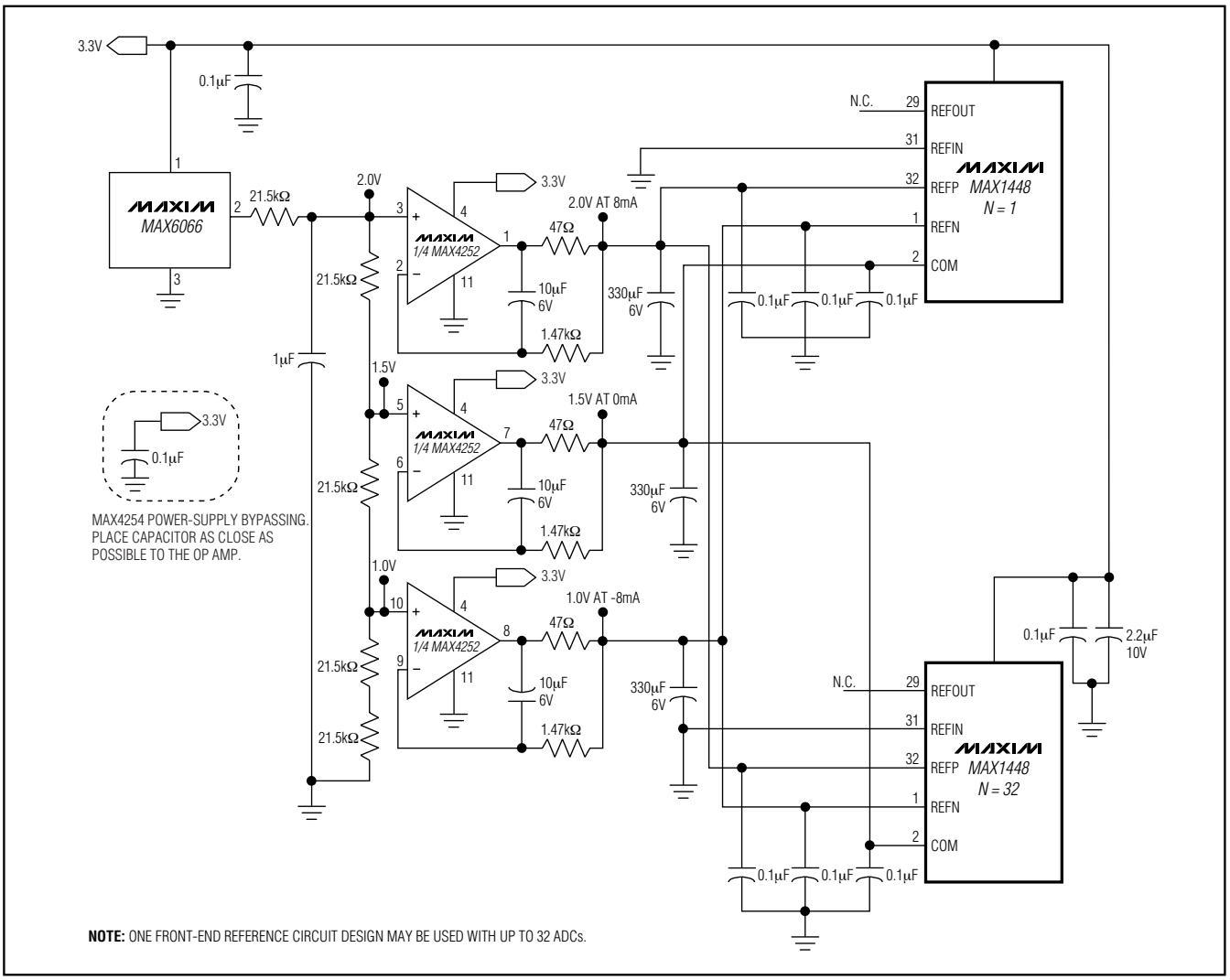


Figure 11. Unbuffered External Reference Drives Up to 32 ADCs

Unbuffered External Reference Drives Multiple ADCs

Connecting each REFIN to analog ground disables the internal reference of each device, allowing the internal reference ladders to be driven directly by a set of external reference sources. Followed by a 10Hz lowpass filter and precision voltage-divider (Figure 11), the MAX6066 generates a DC level of 2.500V. The buffered outputs of this divider are set to 2.0V, 1.5V, and 1.0V, with an accuracy that depends on the tolerance of the divider resistors. The three voltages are buffered by the MAX4252, which provides low noise and low DC offset. The individual voltage followers are connected to 10Hz lowpass filters, which filter both the reference voltage and amplifier noise to a level of $3nV/\sqrt{Hz}$. The 2.0V and 1.0V reference voltages set the differential full-scale range of the associated ADCs at $2V_{P-P}$. The 2.0V and 1.0V buffers drive the ADC's internal ladder resistances between them. Note that the common power supply for all active components removes any concern regarding power-supply sequencing when powering up or down. With the outputs of the MAX4252 matching better than 0.1%, the buffers and subsequent lowpass filters can be replicated to support as many as 32 ADCs. For applications that require more than 32 matched ADCs, a voltage reference and divider string common to all converters is highly recommended.

10-Bit, 80Msps, Single 3.0V, Low-Power ADC with Internal Reference

Grounding, Bypassing, and Board Layout

The MAX1448 requires high-speed board layout design techniques. Locate all bypass capacitors as close to the device as possible, preferably on the same side as the ADC, using surface-mount devices for minimum inductance. Bypass V_{DD}, REFP, REFN, and COM with two parallel 0.1µF ceramic capacitors and a 2.2µF bipolar capacitor to GND. Follow the same rules to bypass the digital supply (OV_{DD}) to OGND. Multilayer boards with separated ground and power planes produce the highest level of signal integrity. Consider using a split ground plane arranged to match the physical location of the analog ground (GND) and the digital output driver ground (OGND) on the ADC's package.

The two ground planes should be joined at a single point so that the noisy digital ground currents do not interfere with the analog ground plane. The ideal location of this connection can be determined experimentally at a point along the gap between the two ground planes that produces optimum results. Make this connection with a low-value, surface-mount resistor (1Ω to 5Ω), a ferrite bead, or a direct short. Alternatively, all ground pins could share the same ground plane if the ground plane is sufficiently isolated from any noisy, digital systems ground plane (e.g., downstream output buffer or DSP ground plane). Route high-speed digital signal traces away from sensitive analog traces. Keep all signal lines short and free of 90° turns.

Static Parameter Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the endpoints of the transfer function once offset and gain errors have been nullified. The MAX1448's static linearity parameters are measured using the best straight-line fit method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of less than 1LSB guarantees no missing codes and a monotonic transfer function.

Dynamic Parameter Definitions

Aperture Jitter

Figure 12 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken (Figure 12).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum A/D noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{(MAX)} = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components minus the fundamental and the DC offset.

Effective Number of Bits (ENOB)

ENOB specifies the dynamic performance of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. ENOB is computed from:

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

Total Harmonic Distortion (THD)

THD is typically the ratio of the RMS sum of the input signal's first five harmonics to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2)}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

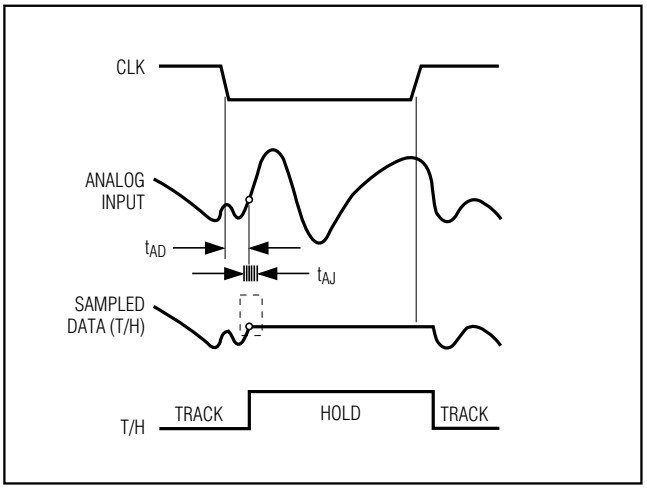


Figure 12. Track-and-Hold Aperture Timing

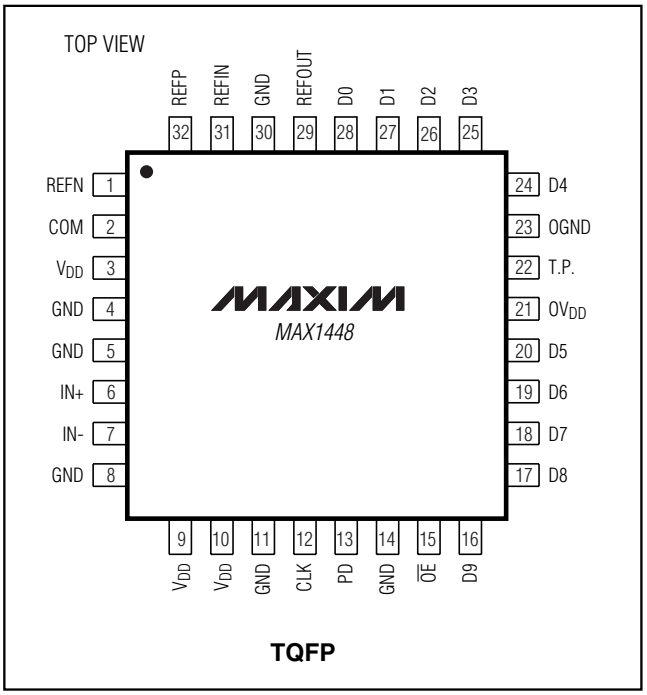
Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio expressed in decibels of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) intermodulation products. The individual input tone levels are at -6.5dB full scale, and their envelope is at -0.5dB full scale.

Pin Configuration



TQFP

Chip Information

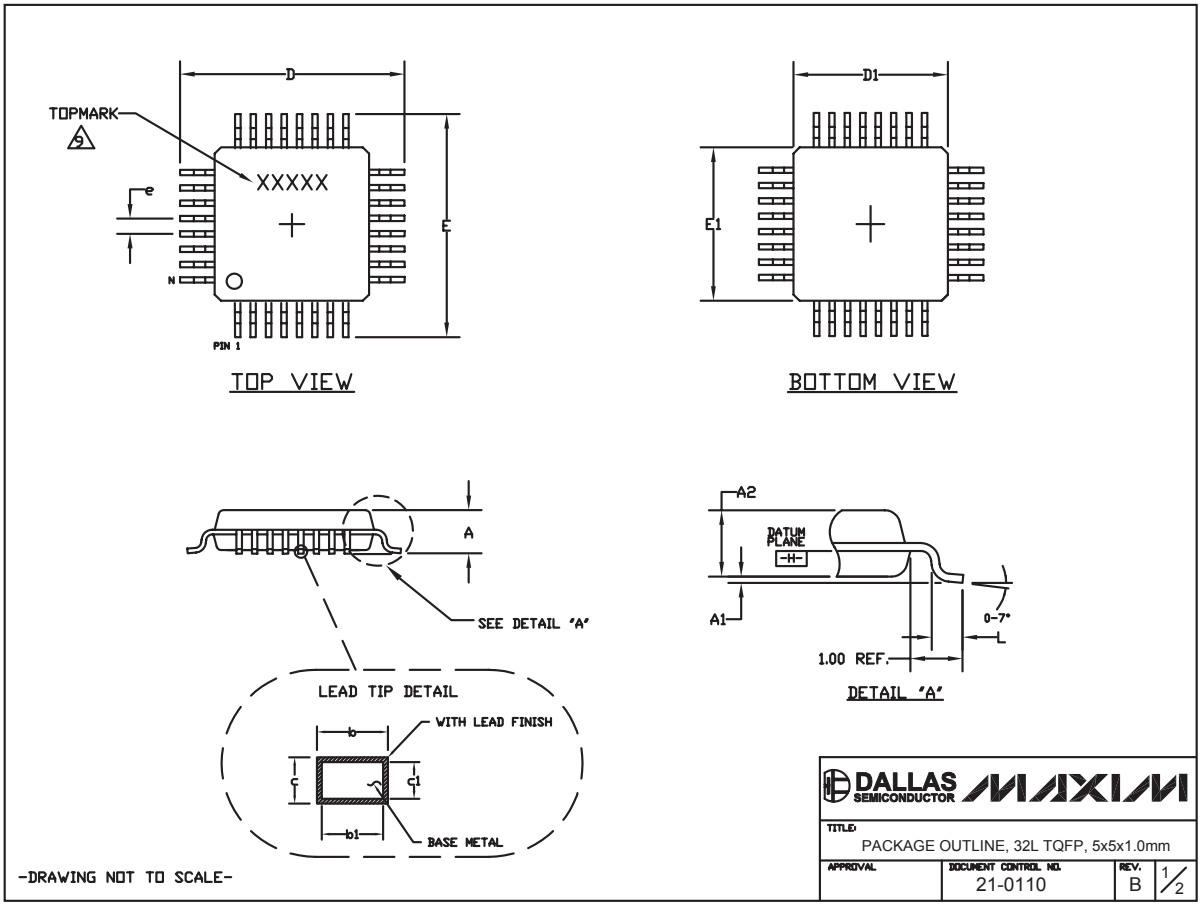
TRANSISTOR COUNT: 5684

PROCESS: CMOS

10-Bit, 80Msps, Single 3.0V, Low-Power ADC with Internal Reference

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE ⊟H⊟ IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. ALL DIMENSIONS ARE IN MILLIMETERS.
7. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95, REGISTRATION MS-026.
8. LEADS SHALL BE COPLANAR WITHIN .004 INCH.
9. TOPMARK SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

	JEDEC VARIATIONS DIMENSIONS IN MILLIMETERS	
	AAA	
	5x5x1.0 MM	
	MIN.	MAX.
A	—	1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	6.80	7.20
D_1	4.80	5.20
E	6.80	7.20
E_1	4.80	5.20
L	0.45	0.75
N	32	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23
c	0.09	0.20
c1	0.09	0.16

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 32L TQFP, 5x5x1.0mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0110	B	2/2