ANALOG DEVICES

18-Bit PCM Audio DAC

AD1860

FEATURES
0.002% THD + Noise
Fast Settling Permits 8× Oversampling
±3V Output
Optional Trim Allows Superlinear Performance
±5V to ±12V Operation
16-Pin Plastic DIP and SOIC Packages
Industry Standard Pinout
2s Complement, Serial Input

APPLICATIONS
High End Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

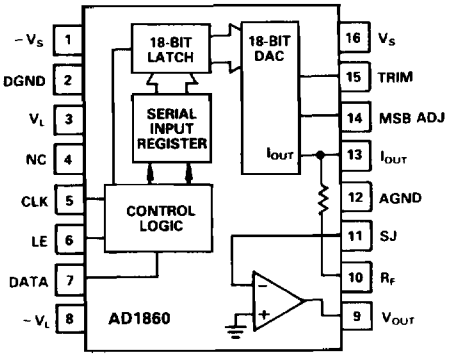
PRODUCT DESCRIPTION

The AD1860 is a monolithic 18-bit PCM Audio DAC. Each device provides a voltage output amplifier, 18-bit DAC, 18-bit serial to parallel input register and voltage reference. The digital portion of the AD1860 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1860 is fabricated with bipolar and MOS devices as well as thin film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser trimming of the linearity error affords extremely low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reproductions of low amplitude signals. Output glitch is also small contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3V signal at load currents up to 8mA. When used in current output mode, the AD1860 provides a ±1mA output signal. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external data clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The input clock can support a 12.5MHz data rate. This serial input port is compatible with second generation digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4× and 8× sampling frequencies.

FUNCTIONAL BLOCK DIAGRAM



The AD1860 can operate with ±5V to ±12V power supplies making it suitable for both the portable and home use markets. The digital supplies, V_L and $-V_L$, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided.

Power dissipation is 110mW typical with ±5V supplies and is 225mW typical when +5V/−12V supplies are used.

The AD1860 is available in either a 16-pin plastic DIP or a 16-pin plastic SOIC surface mount package. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 to ±13.2V.

PRODUCT HIGHLIGHTS

1. 18-bit resolution provides 108dB dynamic range.
2. No external components are required.
3. Operates with ±5V to ±12V supplies.
4. 16-pin DIP or space saving SOIC package.
5. 110mW power dissipation.
6. 1.5μs settling time permits 2×, 4× and 8× oversampling.
7. ±3V or ±1mA output capability.
8. THD + Noise is 100% tested.

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AD1860—SPECIFICATIONS (T_A at +25°C and ±5V supplies unless otherwise noted)

	Min	Typ	Max	Units
RESOLUTION			18	Bits
DIGITAL INPUTS V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH} = V_L$			1.0	µA
I_{IL}, $V_{IL} = 0.4$			−10	µA
Clock Input Frequency	12.5			MHz
ACCURACY				
Gain Error		±2.0		%
Midscale Output Voltage		±30		mV
Differential Linearity Error		±0.001		% of FSR
TOTAL HARMONIC DISTORTION + NOISE				
0dB, 990.5Hz AD1860N-K, R-K		0.002	0.0025	%
AD1860N-J, R-J		0.002	0.004	%
AD1860N, R		0.004	0.008	%
−20dB, 990.5Hz AD1860N-K, R-K		0.006	0.020	%
AD1860N-J, R-J		0.010	0.020	%
AD1860N, R		0.010	0.040	%
−60dB, 990.5Hz AD1860N-K, R-K		0.9	2.0	%
AD1860N-J, R-J		0.9	2.0	%
AD1860N, R		0.9	4.0	%
SIGNAL TO NOISE RATIO (A-Weight Filter)	102	108		dB
DRIFT (0 to +70°C)				
Total Drift		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (to ±0.0015% of FSR)				
Voltage Output, 6V Step		1.5		µs
1LSB Step		1.0		µs
Slew Rate		9		V/µs
Current Output 1mA Step 10Ω to 100Ω Load		350		ns
1kΩ Load		350		ns
MONOTONICITY		15		Bits
OUTPUT				
Voltage Output Configuration				
Bipolar Range	±2.88	±3.0	±3.12	V
Output Current	±8			mA
Output Impedance		0.1		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
Voltage V_L and V_S	4.75		13.2	V
Voltage $-V_L$ and $-V_S$	−13.2		−4.75	V
Current +I, V_L and $V_S = 5V$, 10MHz Clock		10.0	13.0	mA
−I, $-V_L$ and $-V_S = -5V$, 10MHz Clock		12.0	−15.0	mA
Current +I, V_L and $V_S = 12V$, 10MHz Clock		10.5		mA
−I, $-V_L$ and $-V_S = -12V$, 10MHz Clock		13.5		mA
Current +I, V_L and $+V_S = +5V$, 10MHz Clock		10		mA
−I, $-V_L$ and $-V_S = -12V$, 10MHz Clock		14		mA
POWER DISSIPATION				
V_S and $V_L = \pm 5V$, 10MHz Clock		110		mW
V_S and $V_L = \pm 12V$, 10MHz Clock		288		mW
V_S and $V_L = +5V$, $-V_S$ and $-V_L = -12V$, 10MHz Clock		318		mW

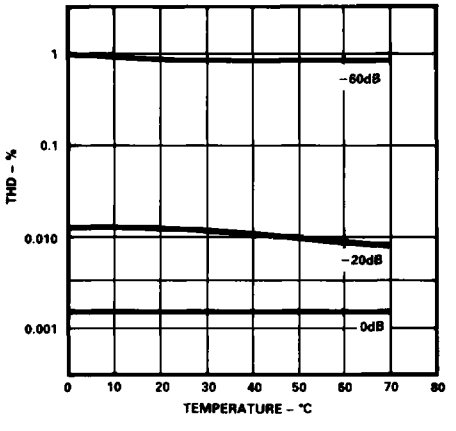
	Min	Typ	Max	Units
TEMPERATURE RANGE				
Specification	0	+25	+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C
WARMUP TIME	1			min

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

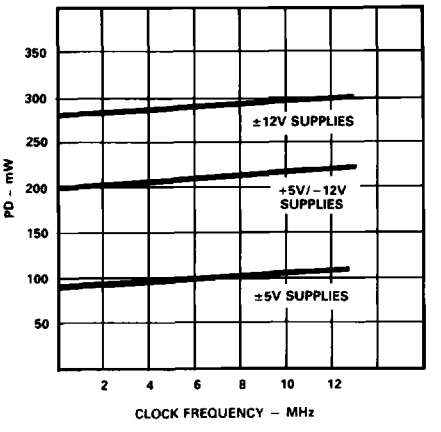
V_L to DGND . . . . . 0 to 13.2V
V_S to AGND . . . . . 0 to 13.2V
$-V_L$ to DGND . . . . . −13.2 to 0V
$-V_S$ to AGND . . . . . −13.2 to 0V
Digital Inputs to DGND . . . . . −0.3 to V_L
AGND to DGND . . . . . ± 0.3V
Short Circuit . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10sec
Storage Temperature . . . . . −60°C to +100°C

Note
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

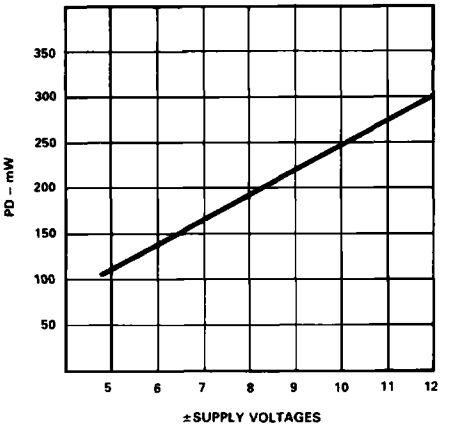


THD vs. Temperature

TYPICAL PERFORMANCE



Power Dissipation vs. Clock Frequency



Power Dissipation vs. Supply Voltages

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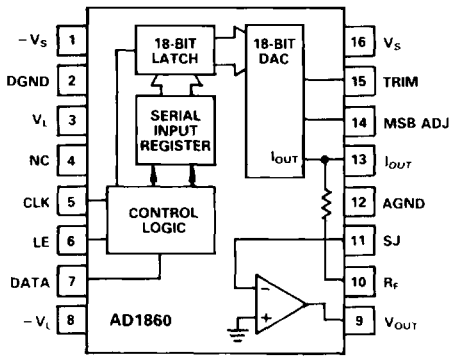
CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.



Functional Block Diagram

PIN ASSIGNMENTS

1	$-V_S$	Analog Negative Power Supply
2	DGND	Logic Ground
3	V_L	Logic Positive Power Supply
4	NC	No Connection
5	CLK	Data Clock Input
6	LE	Latch Enable Input
7	DATA	Serial Data Input
8	$-V_L$	Logic Negative Power Supply
9	V_{OUT}	Voltage Output
10	R_F	Feedback Resistor
11	SJ	Summing Junction
12	AGND	Analog Ground
13	I_{OUT}	Current Output
14	MSB ADJ	MSB Adjustment Terminal
15	TRIM	MSB Trimming Potentiometer Terminal
16	V_S	Analog Positive Power Supply

ORDERING GUIDE

Model	THD @ FS	Package Option*
AD1860N	0.008%	N-16
AD1860R	0.008%	R-16A
AD1860N-J	0.004%	N-16
AD1860R-J	0.004%	R-16A
AD1860N-K	0.0025%	N-16
AD1860R-K	0.0025%	R-16A

*N = Plastic DIP; R = Small Outline IC (Surface Mount Package). For outline information see Package Information section.

TOTAL HARMONIC DISTORTION + NOISE

Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental input frequency. It is usually expressed in percent (%).

THD+N is a measure of the magnitude and distribution of linearity error, differential linearity error, quantization error and noise. The distribution of these errors may be different, depending on the amplitude of the output signal. Therefore, to be most useful, THD+N should be specified for both large and small signal amplitudes.

SETTLING TIME

Settling Time is the time required for the output to reach and remain within a specified error band about its final value, measured from the digital input transition. It is a primary measure of dynamic performance.

DYNAMIC RANGE

Dynamic Range is the specification that indicates the ratio of the smallest signal the converter can resolve to the largest signal it is able to produce. As a ratio, it is usually expressed in decibels (dBs). The theoretical dynamic range of an n-bit converter is (6×n) dB. In the case of the 18-bit AD1860, that is 108dB. The actual dynamic range of a converter is less than the theoretical value due to limitations imposed by noise and other errors.

MIDSCALE ERROR

Midscale Error, or bipolar zero error, is the deviation of the actual analog output from the ideal output (0V) when the 2s complement input code representing half scale is loaded in the input register.

DIFFERENTIAL LINEARITY ERROR

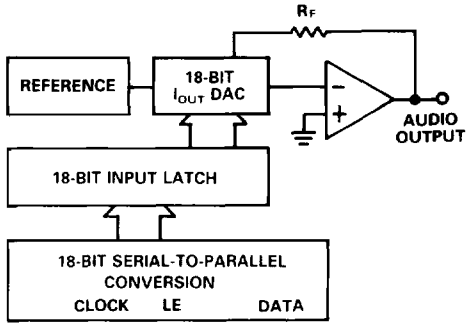
Differential Linearity Error is the measure of the variation in analog value, normalized to full scale, associated with a 1LSB change in the digital input. Monotonic behavior requires that the differential linearity error not exceed 1LSB in the negative direction.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

SIGNAL-TO-NOISE RATIO

The Signal-to-Noise Ratio is defined as the ratio of the amplitude of the output with a full-scale output present to the amplitude of the output when no signal is present. This is measured with a standard A-Weight filter.



AD1860 Block Diagram

FUNCTIONAL DESCRIPTION

The AD1860 is a complete monolithic 18-bit PCM Audio DAC. No additional external components are required for operation. As shown in the block diagram, each chip contains a voltage reference, an output amplifier, an 18-bit DAC, an 18-bit input latch and an 18-bit serial to parallel input register.

The voltage reference consists of a bandgap circuit and buffer amplifier. This combination of elements produces a reference voltage that is unaffected by changes in temperature and age. The DAC output voltage, which is derived from the reference voltage, is also unaffected by these environmental changes.

The output amplifier uses both MOS and bipolar devices to produce low offset, high slew rate and optimum settling time. When combined with the on chip feedback resistor, the output op amp converts the output current of the AD1860 to a voltage output.

The 18-bit D/A converter uses a combination of segmented decoder and R-2R architecture to achieve consistent linearity and differential linearity. The resistors which form the ladder structure are fabricated with silicon chromium thin film. Laser trimming of these resistors further reduces linearity error resulting in low output distortion.

The input register and serial to parallel converter are fabricated with CMOS logic gates. These gates allow the achievement of fast switching speeds and low power consumption. This contributes to the overall low power dissipation of the AD1860.

AD1860—Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1860 has two ground pins, designated Analog and Digital ground. The analog ground pin is the "high quality" ground reference point for the device. The analog ground pin should be connected to the analog common point in the system. The output load should also be connected to that same point.

The digital ground pin returns ground current from the digital logic portions of the AD1860 circuitry. This pin should be connected to the digital common point in the system.

As illustrated in Figure 1, the analog and digital grounds should be connected together at one point in the system.

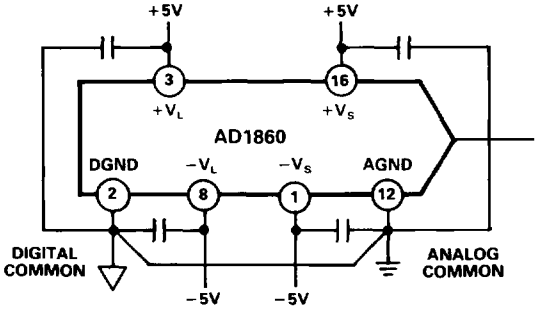


Figure 1. Recommended Circuit Schematic

POWER SUPPLIES AND DECOUPLING

The AD1860 has four power supply input pins. $\pm V_S$ provide the supply voltages to operate the linear portions of the DAC including the voltage reference, output amplifier and control amplifier. The $\pm V_S$ supplies are designed to operate from $\pm 5V$ to $\pm 12V$.

The $\pm V_L$ supplies operate the digital portions of the chip including the input shift register and the input latching circuitry. The $\pm V_L$ supplies are also designed to be operated from $\pm 5V$ to ± 12 V subject only to the limitation that $-V_L$ may not be more negative than $-V_S$.

Decoupling capacitors should be used on all power supply pins. Furthermore, good engineering practice suggests that these capacitors be placed as close as possible to the package pins as well as the common points. The logic supplies, $\pm V_L$, should be decoupled to digital common; and the analog supplies, $\pm V_S$, should be decoupled to analog common.

The use of four separate power supplies will reduce feedthrough from the digital portion of the system to the linear portion of the system, thus contributing to good performance. However, four separate voltage supplies are not necessary for good circuit performance. For example, Figure 2 illustrates a system where only a single positive and a single negative supply are available.

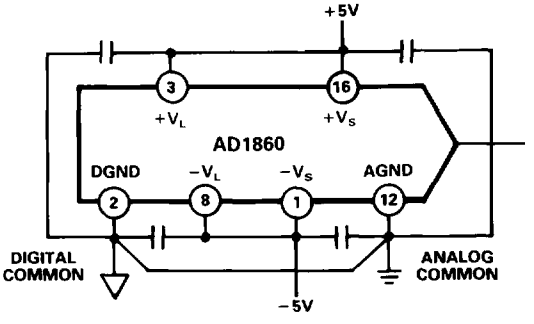


Figure 2. Typical Power Supply Sensitivity

Given that these two supplies are within the range of $\pm 5V$ to $\pm 12V$, they may be used to power the AD1860. In this case, the positive logic and positive analog supplies may both be connected to the single positive supply. The negative logic and negative analog supplies may both be connected to the single negative supply. Performance would benefit from a measure of isolation between the supplies introduced by using simple low pass filters in the individual power supply leads.

As with most linear circuits, changes in the power supplies will affect the output of the DAC. Analog Devices recommends that well regulated power supplies with less than 1% ripple be incorporated into the design of any system using these devices.

TOTAL HARMONIC DISTORTION + NOISE

The THD figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. The THD specification, therefore, provides a direct method to classify and choose an audio DAC for a desired level of performance.

By combining noise measurement with THD measurement, a THD+N specification is produced. This specification measures all undesirable signal produced by the DAC, including harmonic products of the test tone as well as noise.

Analog Devices tests and grades all AD1860s on the basis of THD+N performance. A block diagram of the test setup is shown in Figure 3. In this test setup, a digital data stream representing a 0dB, -20dB or -60dB sinewave is sent to the device under test. The frequency of this waveform in 990.5 Hz.

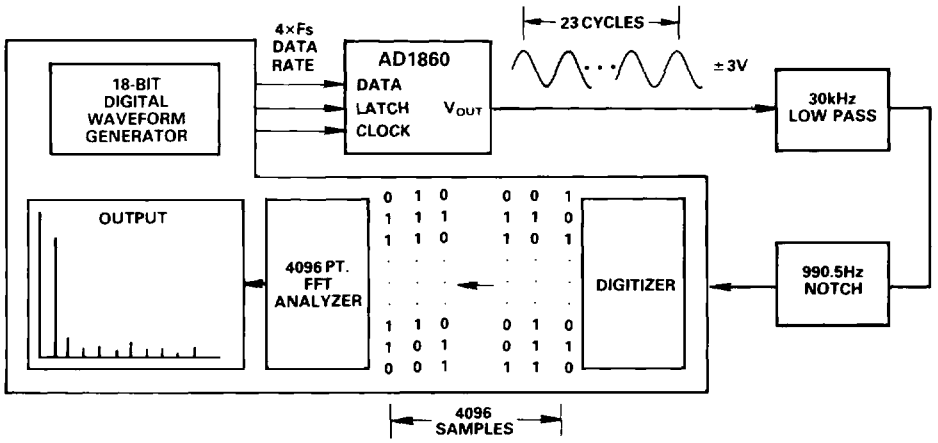


Figure 3. Block Diagram of DistortionTest Circuit

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Input data is sent to the AD1860 at a $4\times F_S$ rate (176.4kHz). The AD1860 under test produces an output signal with its onboard op amp. The automatic test equipment digitizes 4096 samples of the output test waveform, incorporating 23 complete cycles of the sinewave. A 4096 point FFT is performed on the results of the test. Based on the harmonics of the fundamental 990.5Hz test tone and the noise components, the total harmonic distortion + noise of the device is calculated. Neither a deglitcher nor an MSB trim is used during this test.

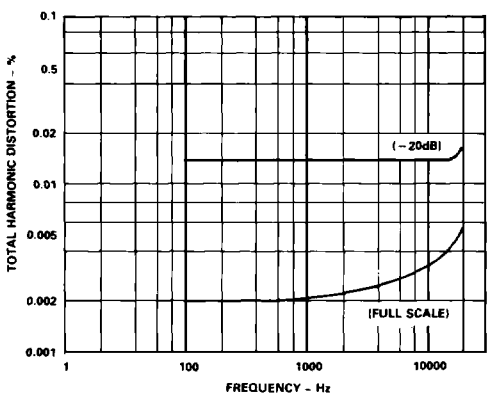

Figure 4. Typical THD vs Frequency

The circuit design, layout and manufacturing techniques employed in the production of the AD1860 result in excellent THD performance. Figure 4 shows the typical unadjusted THD performance of the AD1860 for various amplitudes and frequencies of output signals. As can be seen, the AD1860 offers excellent performance, even at low amplitudes.

OPTIONAL MSB ADJUSTMENT

Use of an optional adjust circuitry allows residual differential linearity error around midscale to be eliminated. This error is especially important when low amplitude signals are being reproduced. In those cases, as the signal amplitude decreases, the ratio of the midscale differential linearity error to the signal amplitude increases, thereby increasing THD.

Therefore, for best performance at low output levels, the optional MSB adjust circuitry shown in Figure 5 may be used to improve performance.

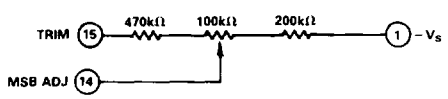

Figure 5. Optional THD Adjust Circuit

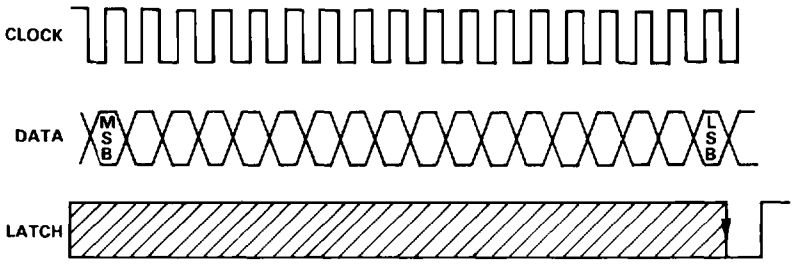

Figure 6. Signal Requirements for AD1860

DIGITAL CIRCUIT CONSIDERATIONS

Input Data

Data is transmitted to the AD1860 in a bit stream composed of 18-bit words with a serial, MSB first format. Three signals must be present to achieve proper operation. They are the Data, Clock and Latch Enable signals. Input data bits are clocked into the input register on the rising edge of the Clock signal. The LSB is clocked in on the 18th clock pulse. When all data bits are loaded, a low-going Latch Enable pulse updates the DAC input. Figure 6 illustrates the general signal requirements for data transfer for the AD1860.

Timing

Figure 7 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1860 are both TTL and 5V CMOS compatible, independent of the power supplies used. The input requirements illustrated in Figures 6 and 7 are compatible with the data outputs provided by popular DSP filter chips used in digital audio playback systems. The AD1860 input clock can run at a 12.5MHz rate. This clock rate will allow data transfer rates for 2×, 4× or 8× oversampling reconstruction. The application section of this datasheet contains additional guides for using the AD1860 with various DSP filter chips available from Sony, NPC and Yamaha.

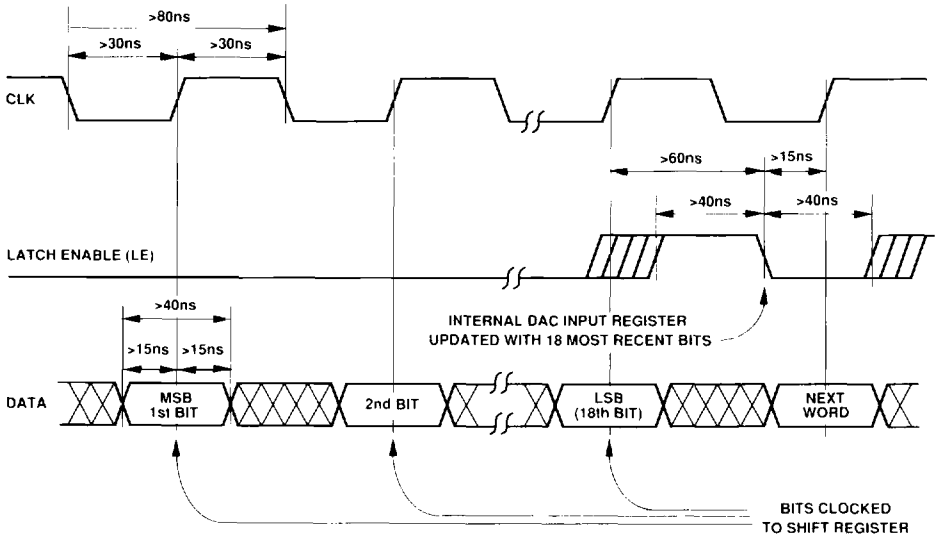

Figure 7. Timing Relationships of Input Signals

APPLICATIONS OF THE AD1860 PCM AUDIO DAC

The AD1860 is a versatile digital-to-analog converter designed for applications in consumer digital audio equipment. Portable, car and home compact disc player, digital audio amplifier and DAT schemes can all use the AD1860. Various circuit architectures are popular in these systems. They include stereo playback sections featuring one DAC per system, one DAC per audio channel (left/right) or multiple DACs per channel. Furthermore, these architectures use different output reconstruction rates to accomplish these functions including reproduction at the sample rate F_S (1×), at twice the sample rate (2×F_S), at four times the sample rate (4×F_S) and even at eight times the sample rate (8×F_S). F_S is 44.1kHz for CD and 48kHz for DAT applications.

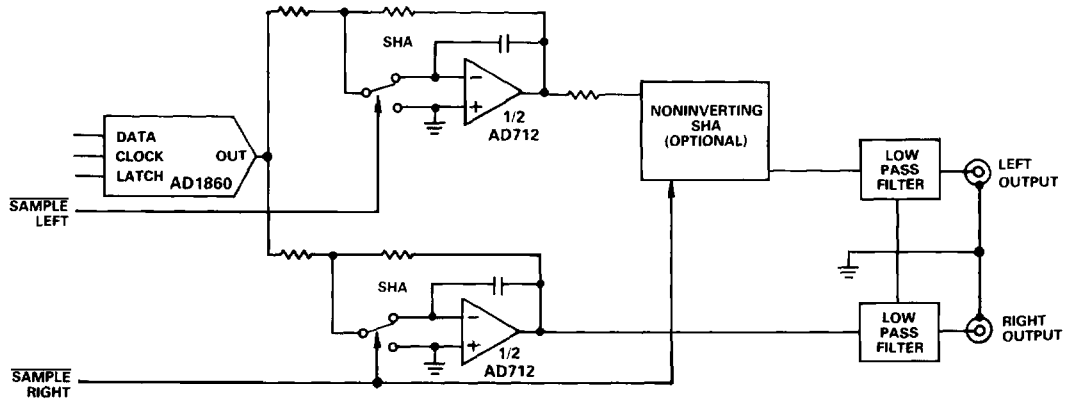

Figure 8. AD1860 in a One DAC per System Architecture

One DAC per System

Figure 8 shows a circuit using one AD1860 per system to reproduce both channels of a typical first generation stereo digital audio system. The input data is fed to the AD1860 in a format which alternates between left channel data and right channel data. The output of the AD1860 is switched between the left channel and right channel output sample/hold amplifiers (SHAs). The SHAs demultiplex and deglitch the output of the AD1860. The timing diagram for the control signals for this circuit are shown in Figure 9.

However, when only two SHAs are used, the actual system performance is limited by the phase delay introduced by the demultiplexed format. This undesirable phase delay is caused by the fact that the data words presented to the inputs of the DAC represent samples taken at precisely the same point in time. But when reconstructed and demultiplexed by a single DAC, these same outputs occur at slightly different times.

By incorporating a noninverting SHA into the circuit, the phase delay can be eliminated. In Figure 8, the optional SHA ensures that the left channel output appears at the same time as the right channel output. This minor change to the circuit eliminates the artificially induced phase delay by restoring simultaneous outputs.

Following the outputs of the SHAs are low pass filters. These filters are required in any sampled data system to remove unwanted aliased components introduced by the sample and reconstruction operations.

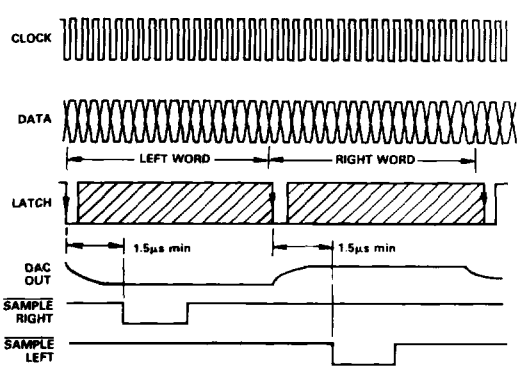

Figure 9. Control Signals for One DAC Circuit

One DAC per Channel

A second approach used to eliminate phase delay between left and right channels employs one DAC per channel. In this architecture, the input data bitstream for each channel is transmitted and then latched into the input register of each DAC. This "second generation" approach is illustrated in Figure 10. A standard implementation of a low pass filter is shown at the output of each DAC. An optional sample/hold amplifier could be connected between the DACs and the LPFs to deglitch the outputs. This is not required, however, to achieve the specified performance.

Two DACs per Channel

Another architecture uses two DACs per channel. In this scheme each DAC reproduces one half of the output waveform. The advantage obtained with this structure is that midscale differential linearity error no longer affects the zero crossing points of the waveforms. Its effects are shifted to the points where the output waveform crosses 1/2 ± 1/4 full scale. The result is that THD performance for low amplitude signals is greatly improved.

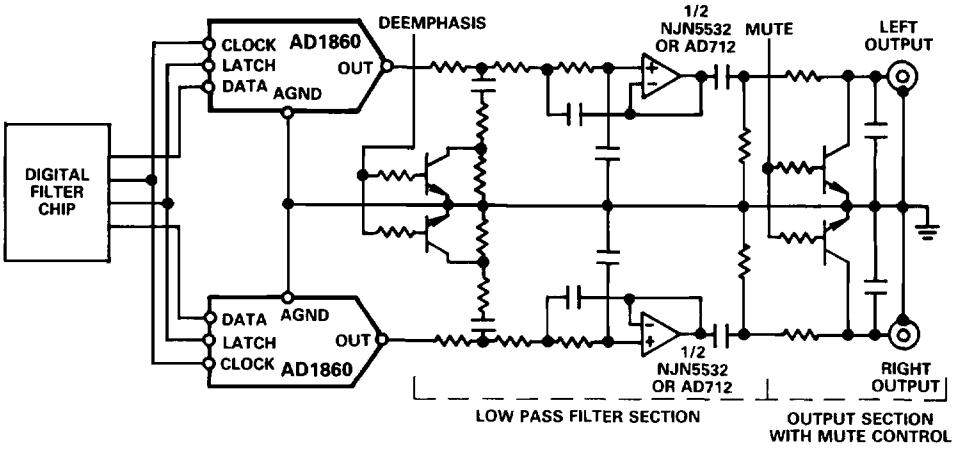

Figure 10. One DAC per Channel Architecture with LPF

DIGITAL FILTERING AND OVERSAMPLING

Oversampling is a term which refers to playback techniques in which the reconstruction frequency used is an integral (2 or more) multiple of the original quantized data rate. For example, in compact disc stereo digital audio playback units, the original quantized data sample rate is 44.1kHz. Popular oversampling rates are 2× or 4×F_S, yielding reconstruction rates of 88.2 and 176.4kHz, respectively.

Oversampling is used to ease the performance constraints of the low pass filters which follow the reconstruction DAC. In any signal reconstructed from sampled data, unwanted frequency components are introduced in the output spectrum; these components are centered at the reconstruction frequency. When a 44.1kHz reconstruction frequency is used, the actual frequency band of interest is 20Hz to 20kHz, and the band of unwanted "image" frequency components extends from 44.1kHz to approximately 24kHz. These unwanted components must be removed with a low-pass filter of very high order. First generation digital audio systems often used low-pass filters of 9, 11 and even 13 poles. Linear implementations of these filters are expensive, difficult to manufacture and can produce distortion due to varying group delay characteristics.

When a 2×reconstruction frequency (88.2kHz) is used, the lowest frequency components now extend down to approximately 68kHz. A 4×rate (176.4kHz) has unwanted components extending down to approximately 156kHz. The filter response needed to remove these frequency components can now be less steep. This means that a lower order filter may be used resulting in less distortion at lower cost. Linear filters with 3 or 5 poles, as shown in Figure 10, are adequate to do the job and are quite common in digital audio products employing oversampling techniques.

Oversampling techniques require the serial input data stream to run at the same integral multiple of the original data rate. So, while the constraints on the output low-pass filter are eased, the constraints on the serial digital input port and the settling time of the output stage are not.

The actual oversampling operation takes place in the digital filter chip (DSP) which is located "upstream" from the DAC. The digital filter accepts data from the media and adds the additional reconstruction points according to the algorithm and coefficients stored in the filter chip. Since the digital filters actually interpolate these additional reconstruction points, they have earned the name "interpolation filters".

The AD1860 is compatible with popular digital filter chips used in digital audio products such as the Sony CXD1088, the Yamaha YM3434 and the NPC SM5813.

Figure 11 illustrates the combination of a second generation digital filter chip, the Sony CXD1088, and the AD1860 audio DAC. The digital filter chip provides 18-bit data words to the DACs at $4\times F_S$. Very high performance can be achieved.

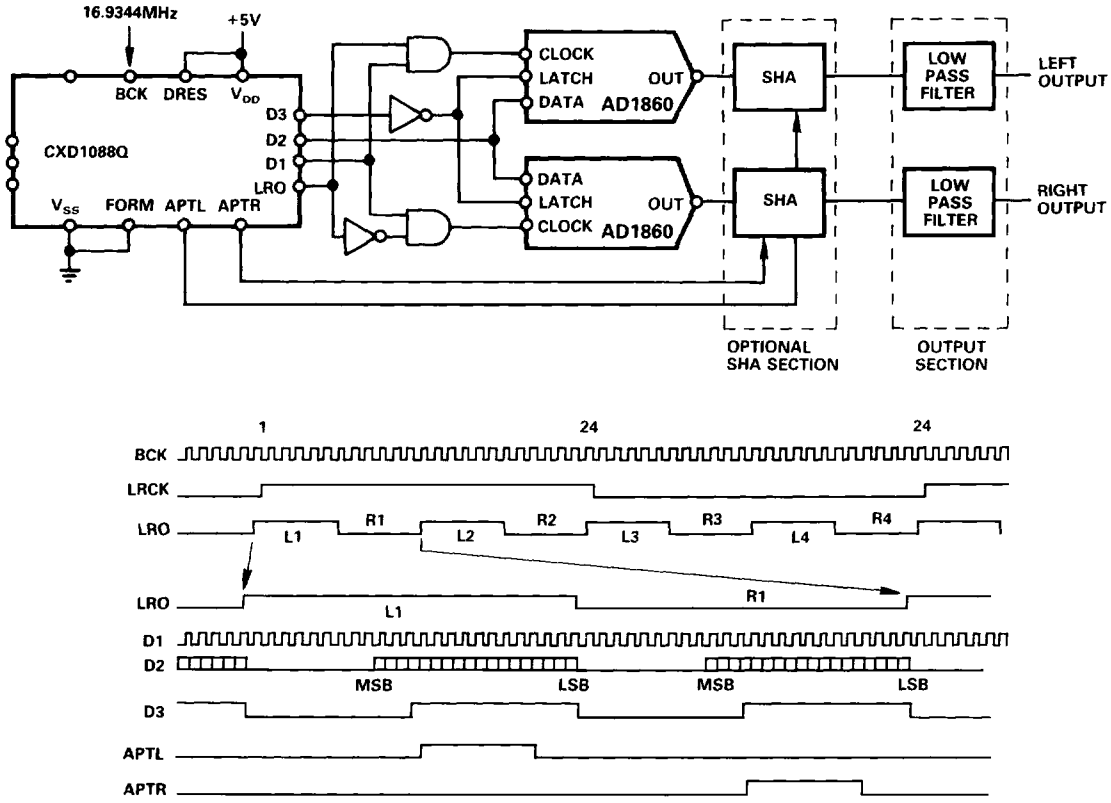

Figure 11. $4\times F_S$ with the CXD1088Q

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Figure 12 illustrates the combination of a Yamaha YM3434 digital filter chip and two AD1860 audio DACs. This combination of components results in $8\times F_S$ oversampling reconstruction rates. This rate allows the use of lower order output low pass filters than would be required with lower oversampling rates, without sacrificing performance. In this high performance CD player application, the DAC input data is simultaneously transmitted to the input registers of the DACs through dedicated left and right channel output pins on the YM3434. This implementation does not require any external components to achieve the full 108dB dynamic range afforded by the 18-bit AD1860 audio DAC. As before, optional sample/hold signals are provided.

Figure 13 shows the schematic for $8\times F_S$ when two AD1860s are used with an NPC SM5813AP/APT digital filter chip. As can be seen, this application is very similar to the one shown in Figure 12. See Figure 10 for an example of a typical LPF.

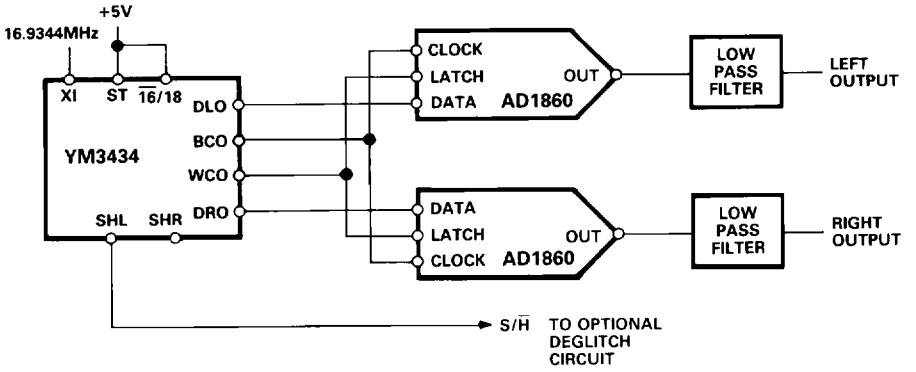

Figure 12. YM3434 and AD1860 Achieve $8\times F_S$

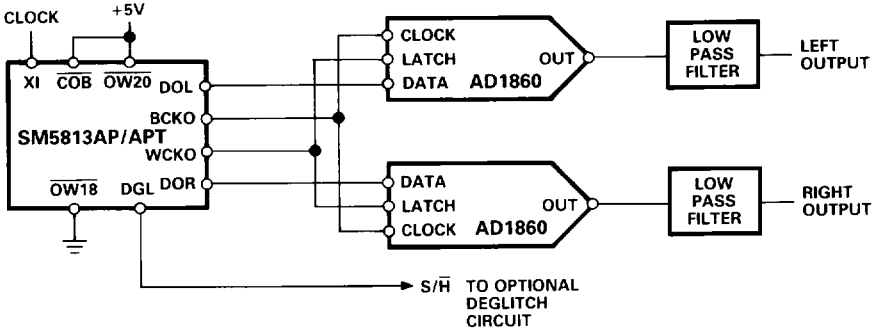

Figure 13. SM5813AP/APT and AD1860 Achieve $8\times F_S$