

## 74F139 Dual 1-of-4 Decoder/Demultiplexer

### General Description

The F139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the F139 can be used as a function generator providing all four minterms of two variables.

### Features

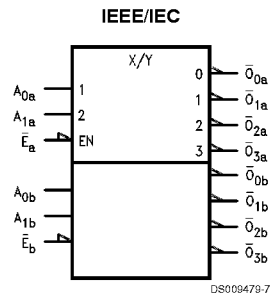
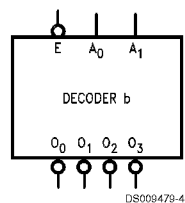
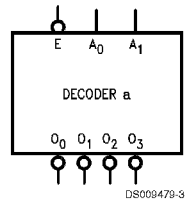
- Multifunction capability
- Two completely independent 1-of-4 decoders
- Active LOW mutually exclusive outputs
- Guaranteed 4000V minimum ESD protection

### Ordering Code:

Commercial	Package Number	Package Description
74F139PC	N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
74F139SC (Note 1)	M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F139SJ (Note 1)	M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ

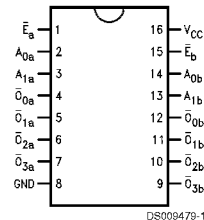
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

### Logic Symbols



### Connection Diagram

#### Pin Assignment DIP and SOIC



## Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$A_0, A_1$	Address Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
$\bar{E}$	Enable Inputs (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\bar{O}_0-\bar{O}_3$	Outputs (Active LOW)	50/33.3	-1 mA/20 mA

## Functional Description

The F139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs ( $A_0-A_1$ ) and provides four mutually exclusive active LOW Outputs ( $\bar{O}_0-\bar{O}_3$ ). Each decoder has an active LOW enable ( $\bar{E}$ ). When  $\bar{E}$  is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the F139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in *Figure 1*, and thereby reducing the number of packages required in a logic network.

## Truth Table

Inputs			Outputs			
$\bar{E}$	$A_0$	$A_1$	$\bar{O}_0$	$\bar{O}_1$	$\bar{O}_2$	$\bar{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

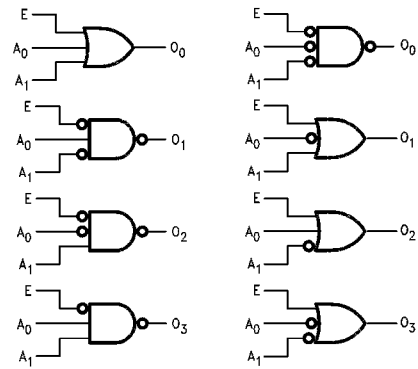
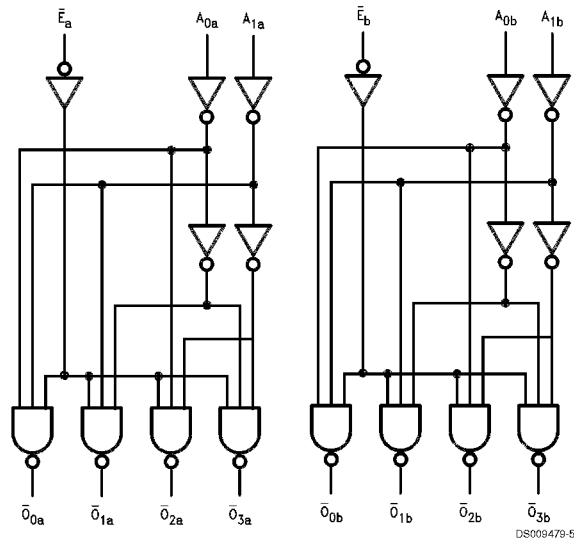


FIGURE 1. Gate Functions (each half)

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3 STATE Output	-0.5V to +5.5V
Current Applied to Output	

in LOW State (Max) twice the rated I<sub>OL</sub> (mA)  
ESD Last Passing Voltage (Min) 4000V

## Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

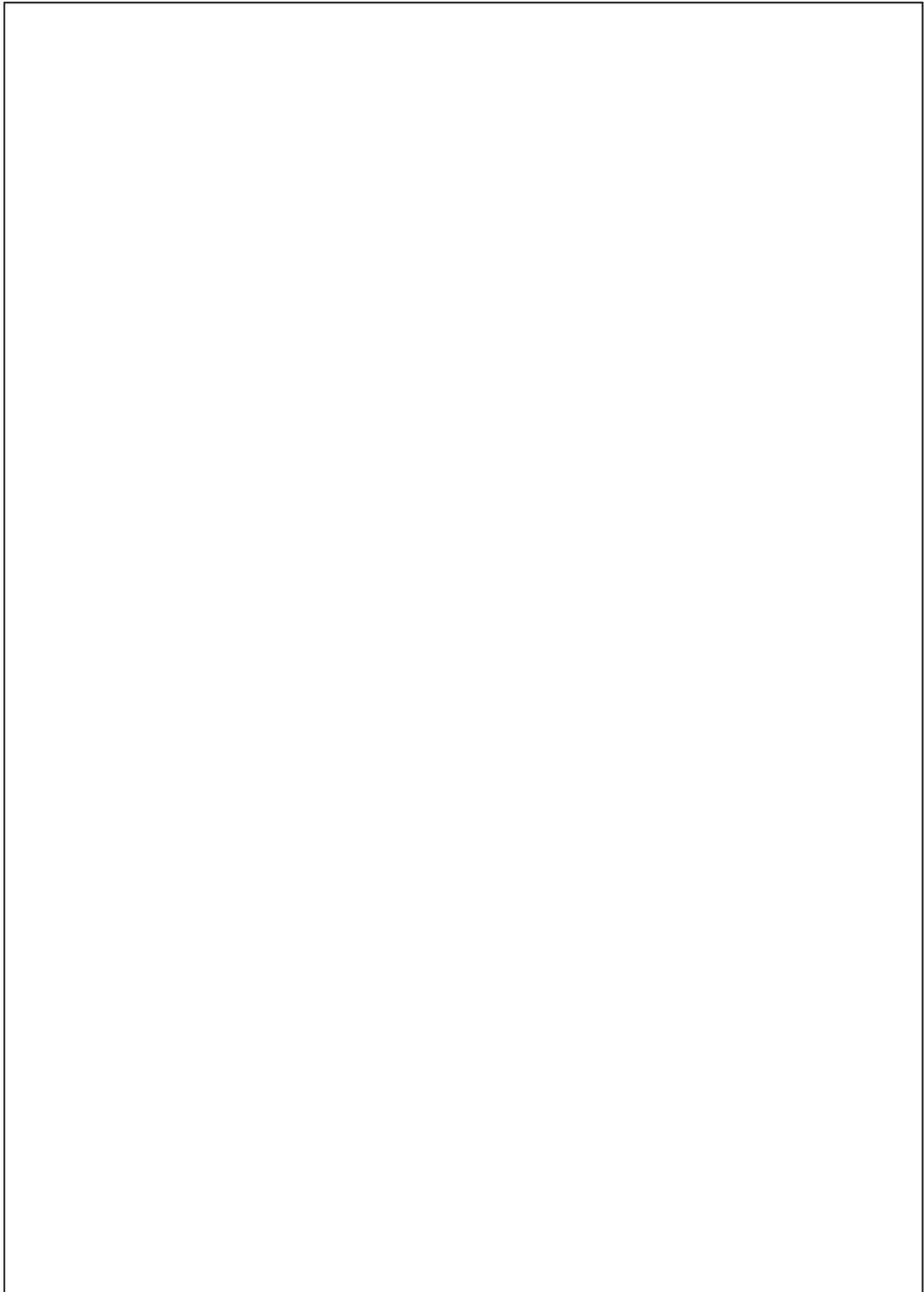
**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

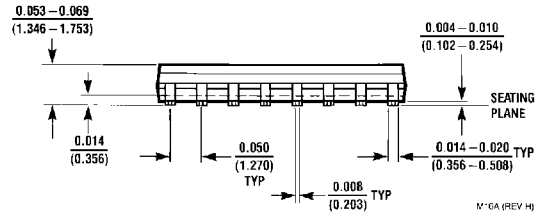
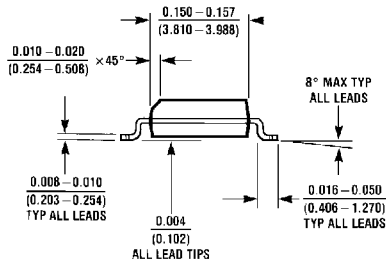
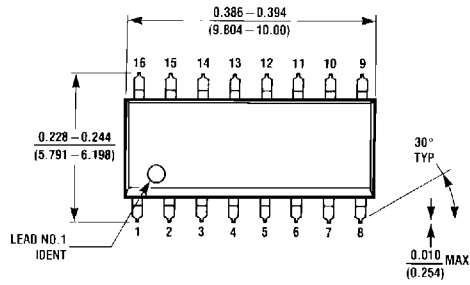
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub>	2.5		V	Min	I <sub>OH</sub> = -1 mA
		5% V <sub>CC</sub>	2.7				I <sub>OH</sub> = -1 mA
V <sub>OL</sub>	Output LOW Voltage			0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>CC</sub>	Power Supply Current		13	20	mA	Max	

## AC Electrical Characteristics

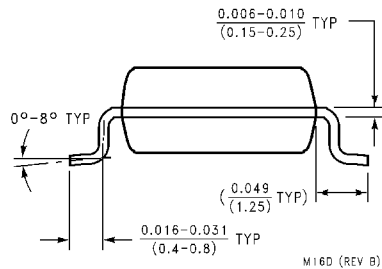
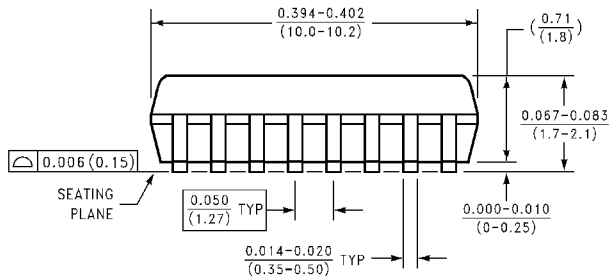
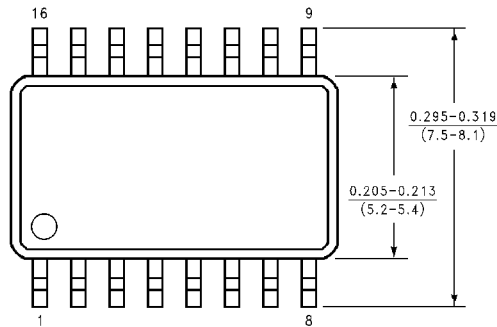
Symbol	Parameter	74F					Units
		T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> , V <sub>CC</sub> = Com C <sub>L</sub> = 50 pF		
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	3.5	5.3	7.5	3.0	8.5	ns
t <sub>PHL</sub>	A <sub>0</sub> or A <sub>1</sub> to $\overline{O}_n$	4.0	6.1	8.0	4.0	9.0	
t <sub>PLH</sub>	Propagation Delay	3.5	5.4	7.0	3.5	8.0	ns
t <sub>PHL</sub>	$\overline{E}_1$ to $\overline{O}_n$	3.0	4.7	6.5	3.0	7.5	



**Physical Dimensions** inches (millimeters) unless otherwise noted

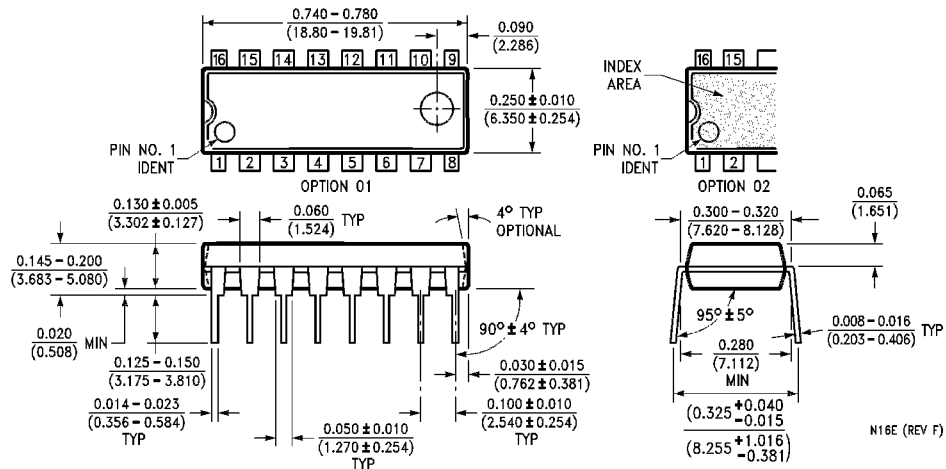


**16-Lead (0.150" Wide) Molded Small Outline Integrated Circuit (S)  
Package Number M16A**



**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)  
Package Number M16D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**16-Lead (0.300" Wide) Molded Dual In-Line Package (P)  
Package Number N16E**

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Fairchild Semiconductor Corporation  
Americas  
Customer Response Center  
Tel: 1-888-522-5372

Fairchild Semiconductor Europe  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 8 141-35-0  
English Tel: +44 (0) 1 793-85-68-56  
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: +852 2737-7200  
Fax: +852 2314-0061

National Semiconductor Japan Ltd.  
Tel: 81-3-5620-6175  
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