

SECTION 2 ELECTRICAL CHARACTERISTICS

2.1 ABSOLUTE MAXIMUM RATINGS (Voltage referenced to V_{SS} , see Notes 1 and 2)

Parameter	Symbol	Min	Max	Unit
DC Supply Voltage	V_{DD}	-0.5	7	V
Input Voltage, All Inputs	V_{in}	-0.5	$V_{DD} + 0.5$	V
Output Voltage, All Outputs	V_{out}	-0.5	$V_{DD} + 0.5$	V
Power Dissipation	PD	—	1	W
Storage Temperature	T_{stg}	-55	150	$^{\circ}C$
Electrostatic Discharge (All except SCSI pins) (Note 3)	ESD	± 4000	—	V
Electrostatic Discharge (All SCSI pins) (Note 3)	ESD	± 4000	—	V

NOTES:

- Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics table or pin descriptions section.
- These devices contain protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}), except for inputs with pullup devices. Unused outputs must be left open.
- Tested using human body model (100 pF @ 1.5 k Ω)

2.2 OPERATING CONDITIONS

Parameter	Test Condition	Symbol	Min	Max	Unit
DC Supply Voltage		V_{DD}	4.75	5.25	V
Supply Current	Static (Note 1)	I_{DD}	—	10	mA
Supply Current	Dynamic	I_{DD}	—	50	mA
Ambient Temperature		T_A	0	70	$^{\circ}C$

NOTE:

- Static conditions: All inputs at V_{SS} , all outputs floating, and all I/O pins configured as inputs.

2.3 DC ELECTRICAL CHARACTERISTICS (V_{DD} = 4.75 V to 5.25 V, T_A = 0°C to 70°C)

2.3.1 Bidirectional Pins with Pullup Resistors (DB0–DB7, DBP, see Note 1)

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	V _{out} = 0.1 V or V _{DD} – 0.1 V I _{out} ≤ 20 μA, V _{DD} = 4.75 or 5.25 V	V _{IH}	2	—	V
Maximum Input Low Voltage	V _{out} = 0.1 V or V _{DD} – 0.1 V I _{out} ≤ 20 μA, V _{DD} = 4.75 or 5.25 V	V _{IL}	—	0.8	V
Minimum Output High-Level Voltage	I _{OH} (Source) = – 2 mA V _{in} = V _{DD} or V _{SS} , V _{DD} = 4.75 V	V _{OH}	2.4	—	V
Maximum Output Low-Level Voltage	I _{OL} (Sink) = 4 mA, V _{in} = V _{DD} or V _{SS} , V _{DD} = 4.75 V	V _{OL}	—	0.4	V
Input Low Pullup Current	V _{in} = 0 V, V _{DD} = 5.25 V	I _{IL} (PU)	– 400	—	μA
Input High Pullup Current	V _{in} = V _{IH} min, V _{DD} = 5.25 V	I _{IH} (PU)	– 250	—	μA
Hi-Z Pullup Current	Output in High Impedance State, V _{out} = V _{DD} or V _{SS} , V _{in} = V _{DD} or V _{SS} , V _{DD} = 5.25 V	I _{OZ} (PU)	– 400	5	μA
Maximum I/O Pin Capacitance		C _{IO}	—	12	pF

NOTE:

1. The MCCS53C90A does not support the DBP signal.

2.3.2 Non-SCSI Input Pins (A0–A3, \overline{CS} , \overline{DACK} , \overline{RD} , \overline{WR} , DIFFM, RESET, CLOCK; see Note 1)

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	V _{out} = 0.1 V or V _{DD} – 0.1 V I _{out} ≤ 20 μA, V _{DD} = 4.75 or 5.25 V	V _{IH}	2	—	V
Maximum Input Low Voltage	V _{out} = 0.1 V or V _{DD} – 0.1 V I _{out} ≤ 20 μA, V _{DD} = 4.75 or 5.25 V	V _{IL}	—	0.8	V
Input Leakage Current	V _{in} = V _{DD} or V _{SS} , V _{DD} = 5.25 V	I _{in}	– 1	1	μA
Maximum Input Pin Capacitance		C _{in}	—	12	pF

NOTE:

1. The MCCS53C90B does not support the DIFFM signal.

2.3.3 Bidirectional TGS with Pullup Resistor

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	$V_{out} = 0.1 \text{ V or } V_{DD} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$, $V_{DD} = 4.75 \text{ or } 5.25 \text{ V}$	V_{IH}	3.1	—	V
Maximum Input Low Voltage	$V_{out} = 0.1 \text{ V or } V_{DD} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$, $V_{DD} = 4.75 \text{ or } 5.25 \text{ V}$	V_{IL}	—	0.8	V
Minimum Output High-Level Voltage	$I_{OH}(\text{Source}) = -4 \text{ mA}$, $V_{in} = V_{DD} \text{ or } V_{SS}$, $V_{DD} = 4.75 \text{ V}$	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{OL}(\text{Sink}) = 8 \text{ mA}$, $V_{in} = V_{DD} \text{ or } V_{SS}$, $V_{DD} = 4.75 \text{ V}$	V_{OL}	—	0.4	V
Input Low Pullup Current	$V_{in} = 0 \text{ Volts}$, $V_{DD} = 5.25 \text{ V}$	$I_{IL}(\text{PU})$	-400	—	μA
Input High Pullup Current	$V_{in} = V_{IH}(\text{min})$, $V_{DD} = 5.25 \text{ V}$	$I_{IH}(\text{PU})$	-250	—	μA
Hi-Z Pullup Current	Output in High Impedance State, $V_{out} = V_{DD} \text{ or } V_{SS}$, $V_{in} = V_{DD} \text{ or } V_{SS}$, $V_{DD} = 5.25 \text{ V}$	$I_{OZ}(\text{PU})$	-400	5	μA
Maximum I/O Pin Capacitance		$C_{I/O}$	—	12	pF

2.3.4 Outputs DREQ, IGS

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Output High-Level Voltage	$I_{OH}(\text{Source}) = -2 \text{ mA}$, $V_{in} = V_{DD} \text{ or } V_{SS}$, $V_{DD} = 4.75 \text{ V}$	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{OL}(\text{Sink}) = 4 \text{ mA}$, $V_{in} = V_{DD} \text{ or } V_{SS}$, $V_{DD} = 4.75 \text{ V}$	V_{OL}	—	0.4	V
Hi-Z Leakage Current	Output in High Impedance State, $V_{out} = V_{DD} \text{ or } V_{SS}$, $V_{in} = V_{DD} \text{ or } V_{SS}$, $V_{DD} = 5.25 \text{ V}$	I_{OZ}	-5	5	μA
Maximum Output Pin Capacitance		C_{out}	—	12	pF

2.3.5 Output RESETO

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Output High-Level Voltage	$I_{OH}(\text{Source}) = -4 \text{ mA}$, $V_{in} = V_{DD}$ or V_{SS} , $V_{DD} = 4.75 \text{ V}$	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{OL}(\text{Sink}) = 8 \text{ mA}$, $V_{in} = V_{DD}$ or V_{SS} , $V_{DD} = 4.75 \text{ V}$	V_{OL}	—	0.4	V
Hi-Z Leakage Current	Output in High Impedance State, $V_{out} = V_{DD}$ or V_{SS} , $V_{in} = V_{DD}$ or V_{SS} , $V_{DD} = 5.25 \text{ V}$	I_{OZ}	-5	5	μA
Maximum Output Pin Capacitance		C_{out}	—	12	pF

2.3.6 Output $\overline{\text{INT}}$ (Open Drain)

Parameter	Test Condition	Symbol	Min	Max	Unit
Maximum Output Low-Level Voltage	$I_{OL}(\text{Sink}) = 8 \text{ mA}$, $V_{in} = V_{DD}$ or V_{SS} , $V_{DD} = 4.75 \text{ V}$	V_{OL}	—	0.4	V
Hi-Z Leakage Current	Output in High Impedance State, $V_{out} = V_{DD}$ or V_{SS} , $V_{in} = V_{DD}$ or V_{SS} , $V_{DD} = 5.25 \text{ V}$	I_{OZ}	-5	5	μA
Maximum Output Pin Capacitance		C_{out}	—	12	pF

2.3.7 SCSI Control Input Pins ($\overline{\text{SEL}}$, $\overline{\text{BSY}}$, $\overline{\text{REQ}}$, $\overline{\text{ACK}}$, $\overline{\text{MSG}}$, $\overline{\text{C_DI}}$, $\overline{\text{I_OI}}$, $\overline{\text{ATN}}$, $\overline{\text{RST}}$)

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{DD} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$, $V_{DD} = 4.75$ or 5.25 V	V_{IH}	2	—	V
Maximum Input Low Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{DD} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$, $V_{DD} = 4.75$ or 5.25 V	V_{IL}	—	0.8	V
Minimum Hysteresis Voltage	$V_{out} = 0.1 \text{ V}$ or $V_{DD} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$, $V_{DD} = 4.75 \text{ V}$	V_H	200	—	mV
Input Leakage Current	$V_{in} = V_{DD}$ or V_{SS} , $V_{DD} = 5.25 \text{ V}$	I_{in}	-1	1	μA
Maximum Input Pin Capacitance		C_{in}	—	12	pF

2.3.8 SCSI Bidirectional Pins ($\overline{\text{SDI7}}\text{--}\overline{\text{SDI0}}$, $\overline{\text{SDIP}}$)

Parameter	Test Condition	Symbol	Min	Max	Unit
Minimum Input High Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{DD}} - 0.1 \text{ V}$ $ I_{\text{out}} \leq 20 \mu\text{A}$, $V_{\text{DD}} = 4.75 \text{ or } 5.25 \text{ V}$	V_{IH}	2	—	V
Maximum Input Low Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{DD}} - 0.1 \text{ V}$ $ I_{\text{out}} \leq 20 \mu\text{A}$, $V_{\text{DD}} = 4.75 \text{ or } 5.25 \text{ V}$	V_{IL}	—	0.8	V
Minimum Hysteresis Voltage	$V_{\text{out}} = 0.1 \text{ V or } V_{\text{DD}} - 0.1 \text{ V}$ $ I_{\text{out}} \leq 20 \mu\text{A}$, $V_{\text{DD}} = 4.75 \text{ V}$	V_{H}	200	—	mV
Minimum Output High-Level Voltage	$I_{\text{OH}}(\text{Source}) = -2 \text{ mA}$, $V_{\text{in}} = V_{\text{DD}} \text{ or } V_{\text{SS}}$, $V_{\text{DD}} = 4.75 \text{ V}$	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{\text{OL}}(\text{Sink}) = 4 \text{ mA}$ $V_{\text{in}} = V_{\text{DD}} \text{ or } V_{\text{SS}}$, $V_{\text{DD}} = 4.75 \text{ V}$	V_{OL}	—	0.4	V
Hi-Z Leakage Current	Output in High Impedance State, $V_{\text{out}} = V_{\text{DD}} \text{ or } V_{\text{SS}}$, $V_{\text{in}} = V_{\text{DD}} \text{ or } V_{\text{SS}}$, $V_{\text{DD}} = 5.25 \text{ V}$	I_{OZ}	-5	5	μA
Maximum I/O Pin Capacitance		$C_{\text{I/O}}$	—	12	pF

2.3.9 SCSI Output Pins ($\overline{\text{SDO0}}\text{--}\overline{\text{SDO7}}$, $\overline{\text{SDOP}}$, $\overline{\text{SELO}}$, $\overline{\text{BSYO}}$, $\overline{\text{REQO}}$, $\overline{\text{ACKO}}$, $\overline{\text{MSGO}}$, $\overline{\text{C_DO}}$, $\overline{\text{I_OO}}$, $\overline{\text{ATNO}}$, $\overline{\text{RSTO}}$)

Parameter	Test Condition	Symbol	Min	Max	Unit
Maximum Output High-Level Voltage	$I_{\text{OH}}(\text{Source}) = 16 \text{ mA}$, $V_{\text{in}} = V_{\text{DD}} \text{ or } V_{\text{SS}}$, $V_{\text{DD}} = 4.75 \text{ V}$	V_{OH}	2.4	—	V
Maximum Output Low-Level Voltage	$I_{\text{OL}}(\text{Sink}) = 48 \text{ mA}$, $V_{\text{in}} = V_{\text{DD}} \text{ or } V_{\text{SS}}$, $V_{\text{DD}} = 4.75 \text{ V}$	V_{OL}	—	0.5	V
Hi-Z Leakage Current	Output in High Impedance State, $V_{\text{out}} = V_{\text{DD}} \text{ or } V_{\text{SS}}$, $V_{\text{in}} = V_{\text{DD}} \text{ or } V_{\text{SS}}$, $V_{\text{DD}} = 5.25 \text{ V}$	I_{OZ}	-5	5	μA
Maximum Output Pin Capacitance		C_{out}	—	12	pF

2.4 AC ELECTRICAL CHARACTERISTICS (0°–70°C, V_{DD} = 4.75 to 5.25 V)

2.4.1 Pad Termination

Pin	Termination
RESET0, DREQ, TGS, IGS	50 pF
SDIP, SDI7 . . . SDI0	50 pF
INT	50 pF 1 kΩ pullup
DB7 . . . DB0, DBP	85 pF
RST0, SEL0, BSY0, ATN0, MSG0, CD0, I00, REQ0, ACK0, SDO7 . . . SDO0, SDOP	200 pF 110 Ω pullup, 165 Ω pulldown

2.4.2 Clock

Time	Parameter	Symbol	Min	Max	Unit	Notes
t ₁	Clock Period	t _{CP}	25	—	ns	
t ₂	Clock Frequency	f _{CP}	—	40	MHz	1, 3
t ₃	Clock High Time	t _{CH}	0.4 × t _{CP}	—	ns	2
t ₄	Clock Low Time	t _{CL}	0.4 × t _{CP}	—	ns	2

NOTES:

1. There are no minimum frequency requirements. 40 MHz is recommended for FAST SCSI synchronous mode.
2. For synchronous mode and an odd sync period, |t_{CL} – t_{CH}| ≤ 5 nanoseconds.
3. For f_{CP} > 25 MHz set prescale bit (clock conversion register).

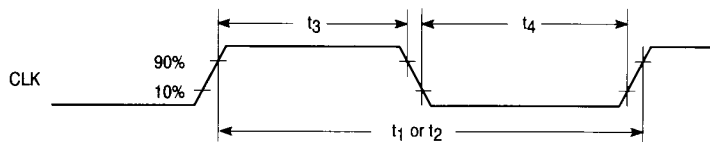


Figure 2.1. Clock Timing

2.4.3 Reset Input

Time	Parameter	Symbol	Min	Max	Unit
t ₅	RESET Pulse Width	t _w (RST)	80	—	ns
t ₆	RESET High to RESETO High	t _{RH}	—	50	ns
t ₇	RESET Low to RESETO Low	t _{RL}	—	55	ns

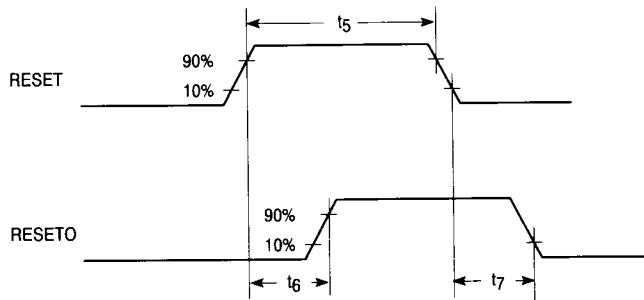


Figure 2.2. Reset Input Timing

2.4.4 Interrupt Output

Time	Parameter	Symbol	Min	Max	Unit	Notes
t_8	\overline{INT} to \overline{RD} (Interrupt Reg read)	t_{IR}	0	—	ns	1, 2
t_9	\overline{RD} Low to \overline{INT} High (\overline{CS} active)	t_{RI}	—	100	ns	1, 2
t_{10}	\overline{RD} High to \overline{INT} Low (\overline{CS} active)	t_{RDI}	—	100	ns	1, 2

NOTES:

1. All timing based on an Interrupt Register read. Reference Register Read timing information for control line timing information.
2. The Interrupt register should not be read when \overline{INT} is inactive.

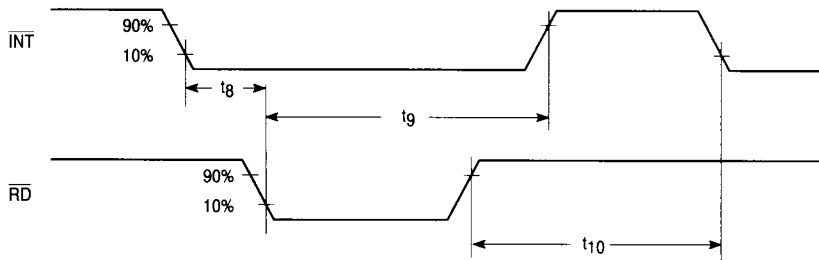


Figure 2.3. Interrupt Output Timing

2.4.5 Register Write

Time	Parameter	Symbol	Min	Max	Unit	Notes
t ₁₁	Address Setup to \overline{CS} Low	t _{su(AD)}	0	—	ns	1, 2
t ₁₂	\overline{CS} Setup to \overline{WR}	t _{su(WR)}	0	—	ns	1, 3
t ₁₃	\overline{WR} Pulse Width	t _{w(WR)}	40	—	ns	1
t ₁₄	Data Setup to \overline{WR} High	t _{su(DW)}	11	—	ns	1, 3
t ₁₅	Address Hold Time from \overline{CS}	t _{h(ACS)}	50	—	ns	1, 2
t ₁₆	Data Hold Time from \overline{WR} High	t _{h(DWR)}	2	—	ns	1, 3
t ₁₇	\overline{WR} High to \overline{CS} High	t _{wc}	0	—	ns	1, 3
t ₁₈	\overline{CS} High to \overline{CS} Low	t _{c(CS)}	40	—	ns	1, 3
t ₁₉	\overline{WR} High to \overline{WR} Low	t _{c(WR)}	60	—	ns	1

NOTES:

1. \overline{DACK} must be inactive during all register I/O cycles.
2. \overline{CS} must cycle to capture a new register address.
3. \overline{WR} edges may precede or follow \overline{CS} edges. If \overline{WR} is held low, data setup to \overline{CS} high is 25 ns minimum; data hold from \overline{CS} high is 60 ns minimum; and t_{c(CS)} is 60 ns minimum.

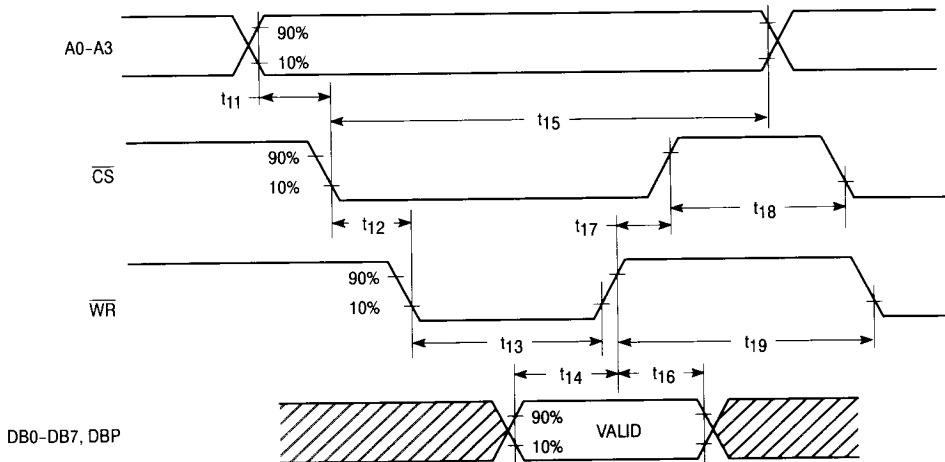


Figure 2.4. Register Write Timing

2.4.6 Register Read

Time	Parameter	Symbol	Min	Max	Unit	Notes
t ₂₀	Address Setup to \overline{CS} Low	t _{su} (AD)	0	—	ns	1, 2
t ₂₁	\overline{CS} Setup to \overline{RD}	t _{su} (RD)	0	—	ns	1, 3
t ₂₂	\overline{RD} Pulse Width	t _w (WR)	50	—	ns	1
t ₂₃	\overline{RD} to Data Valid	t _{su} (DW)	—	50	ns	1, 3
t ₂₄	\overline{CS} to Data Valid	t _h (CSD)	—	70	ns	1
t ₂₅	Address Hold Time from \overline{CS}	t _h (ACS)	50	—	ns	1, 2
t ₂₆	Data Release Time	t _h (D)	2	40	ns	1, 3
t ₂₇	\overline{RD} High to \overline{CS} High	t _c (RDCS)	0	—	ns	1, 3
t ₂₈	\overline{CS} High to \overline{CS} Low	t _c (CD)	40	—	ns	1

NOTES:

1. \overline{DACK} must be inactive during all register I/O cycles.
2. \overline{CS} must cycle to capture a new register address.
3. \overline{RD} edges may precede or follow \overline{CS} edges. If \overline{RD} is held low, the time from \overline{CS} low to stable data is t_h(CSD) and the data release time from \overline{CS} high is t_h(D).

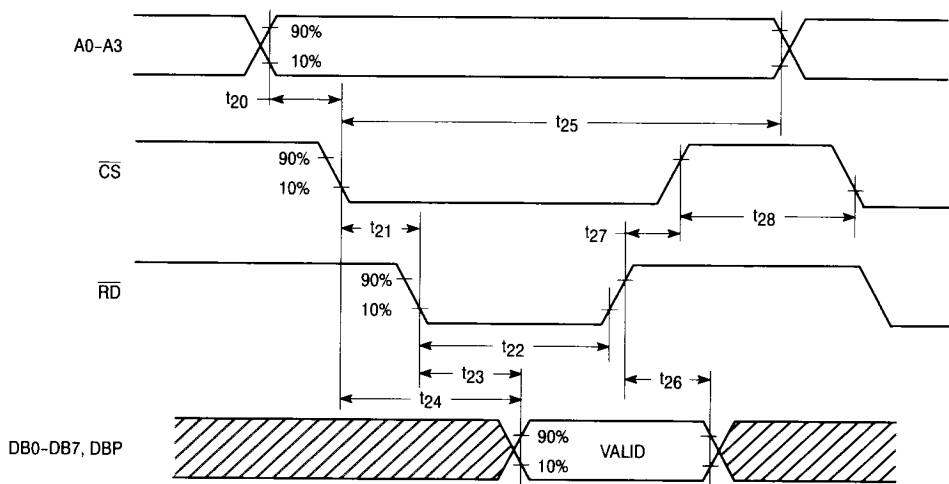


Figure 2.5. Register Read Timing

2.4.7 DMA Write

Time	Parameter	Symbol	Min	Max	Unit	Notes
t ₂₉	$\overline{\text{DACK}}$ Low to DREQ Low (Negation Pending)	t _{DADRL}	0	38	ns	1
t ₃₀	$\overline{\text{DACK}}$ Low to $\overline{\text{WR}}$ Low	t _{DAWR}	0	—	ns	1, 3
t ₃₁	$\overline{\text{WR}}$ Pulse Width	t _{w(WR)}	40	—	ns	1
t ₃₂	Data Setup to $\overline{\text{WR}}$ High	t _{DWR}	11	—	ns	1, 3
t ₃₃	$\overline{\text{WR}}$ High to $\overline{\text{DACK}}$ High	t _{WRDA}	0	—	ns	1, 3
t ₃₄	Data Hold Time to $\overline{\text{WR}}$ High	t _{h(D)}	2	—	ns	1, 3
t ₃₅	$\overline{\text{DACK}}$ High to $\overline{\text{DACK}}$ Low	t _{wh(DACK)}	12	—	ns	1, 2, 3
t ₃₆	$\overline{\text{DACK}}$ High to DREQ High (Assertion Pending)	t _{DADRH}	0	50	ns	1, 3
t ₃₇	$\overline{\text{DACK}}$ Pulse Width	t _{w(DACK)}	50	—	ns	1, 2, 3, 4
t ₃₈	$\overline{\text{WR}}$ High to $\overline{\text{WR}}$ Low	t _{w(WR)}	40	—	ns	1

NOTES:

1. $\overline{\text{CS}}$ must be inactive during all DMA accesses.
2. $\overline{\text{ACK}}$ must be cycled once for each DMA access.
3. $\overline{\text{WR}}$ may precede or follow $\overline{\text{DACK}}$ edges. If $\overline{\text{WR}}$ is held low, the data setup to $\overline{\text{DACK}}$ high is 15 ns and t_{wh(DACK)} is 40 ns minimum.
4. DREQ will remain true as long as the FIFO has room for at least one more byte. If the current write cycle fills the FIFO, DREQ will go false. If the SCSI bus then removes a byte from the FIFO, DREQ will not go true until $\overline{\text{DACK}}$ goes false.
5. For synchronous mode, there are no additional requirements as regards chip clock CLOCK.

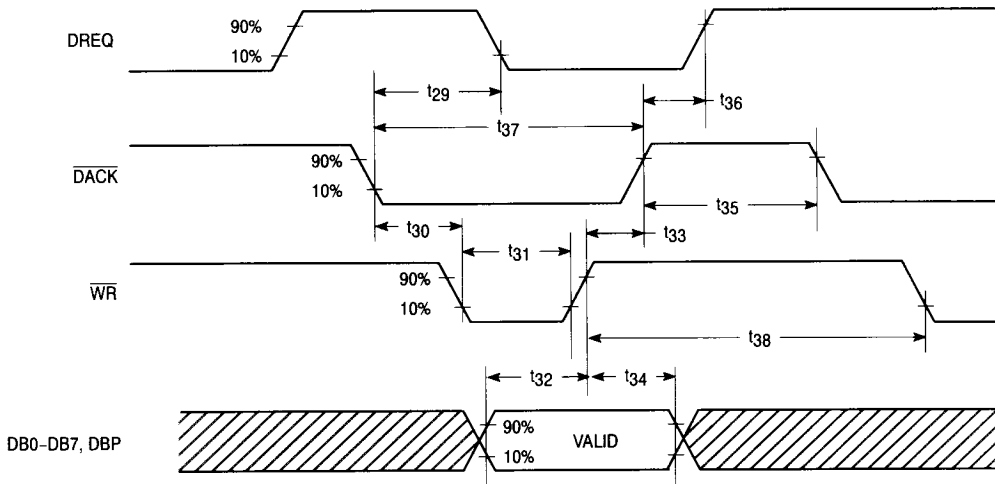


Figure 2.6. DMA Write Timing

2.4.8 DMA Read

Time	Parameter	Symbol	Min	Max	Unit	Notes
t ₃₉	$\overline{\text{DACK}}$ Low to DREQ Low (Negation Pending)	t _{DADRL}	0	38	ns	1
t ₄₀	$\overline{\text{DACK}}$ Low to $\overline{\text{RD}}$ Low	t _{DARD}	0	—	ns	1, 3
t ₄₁	$\overline{\text{RD}}$ Pulse Width	t _w ($\overline{\text{RD}}$)	50	—	ns	1
t ₄₂	$\overline{\text{RD}}$ to Data Valid	t _{DRD}	—	41	ns	1, 3
t ₄₃	$\overline{\text{DACK}}$ to Data Valid	t _{DAD}	—	41	ns	1, 3
t ₄₄	$\overline{\text{RD}}$ High to $\overline{\text{DACK}}$ High	t _{RDDA}	0	—	ns	1, 3
t ₄₅	Data Hold Time	t _h (D)	2	40	ns	1, 2, 3
t ₄₆	$\overline{\text{DACK}}$ High to $\overline{\text{DACK}}$ Low	t _{wh} ($\overline{\text{DACK}}$)	12	—	ns	1, 4
t ₄₇	$\overline{\text{DACK}}$ High to DREQ High (Assertion Pending)	t _{DADRH}	0	50	ns	1
t ₄₈	$\overline{\text{DACK}}$ Pulse Width	t _w ($\overline{\text{DACK}}$)	50	—	ns	1, 2

NOTES:

1. $\overline{\text{CS}}$ must be inactive during all DMA accesses.
2. $\overline{\text{ACK}}$ must be cycled once for each DMA access.
3. $\overline{\text{RD}}$ may precede or follow $\overline{\text{DACK}}$ edges. If $\overline{\text{RD}}$ is held low, the time from $\overline{\text{DACK}}$ low to stable data is t_{DAD} and data release time is t_h(D).
4. If t_{wh}($\overline{\text{DACK}}$) is ≤ 18 ns, then t_{DAD} is 45 ns max.
5. DREQ will remain true if there are more bytes in the FIFO. If the current read cycle empties the FIFO, DREQ will go false. If the SCSI bus then loads another byte into the FIFO, DREQ will not be asserted until $\overline{\text{DACK}}$ goes false.
6. For synchronous mode, there are no additional requirements as regards chip clock CLOCK.

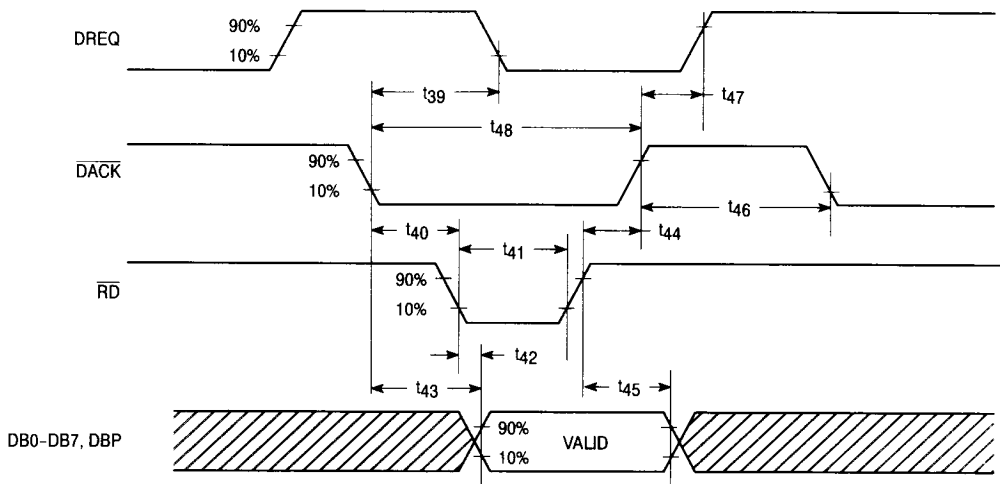


Figure 2.7. DMA Read Timing

2.4.9 Initiator Asynchronous Send

Time	Parameter	Symbol	Min	Max	Unit
t ₄₉	Data Out Stable to $\overline{\text{ACKO}}$ Low	t _{DACL}	55	—	ns
t ₅₀	$\overline{\text{REQI}}$ High to $\overline{\text{ACKO}}$ High	t _{REACH}	—	43	ns
t ₅₁	$\overline{\text{REQI}}$ High to Next Data Byte Valid (FIFO bottom full)	t _{RED}	—	75	ns
t ₅₂	$\overline{\text{REQI}}$ Low to $\overline{\text{ACKO}}$ Low (Data Previously Setup)	t _{REACL}	—	47	ns

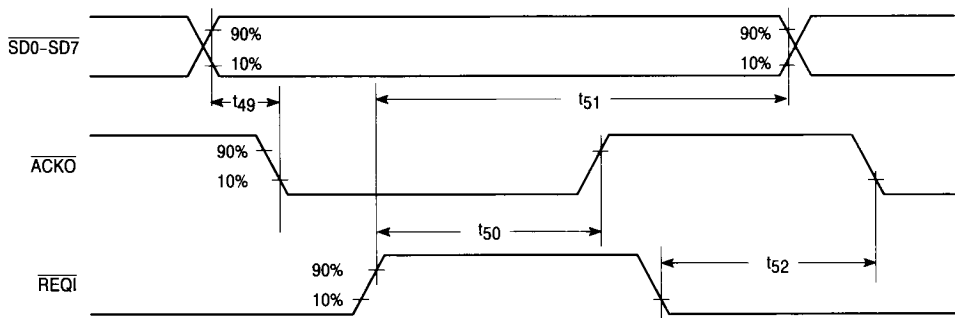


Figure 2.8. Initiator Asynchronous Send Timing

2.4.10 Initiator Asynchronous Read

Time	Parameter	Symbol	Min	Max	Unit
t ₅₃	Data Setup to $\overline{\text{REQI}}$ Low	t _{su} (SREQ)	20	—	ns
t ₅₄	$\overline{\text{REQI}}$ High to $\overline{\text{ACKO}}$ High	t _{REACH}	—	43	ns
t ₅₅	$\overline{\text{REQI}}$ Low to $\overline{\text{ACKO}}$ Low (FIFO not full)	t _{REACL}	—	47	ns

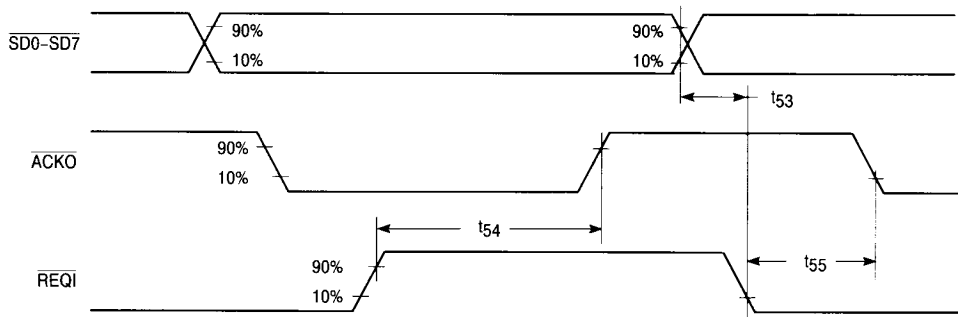


Figure 2.9. Initiator Asynchronous Receive Timing

2.4.11 Target Asynchronous Send

Time	Parameter	Symbol	Min	Max	Unit
t56	Data Out Stable to REQ0 Low	tDREL	55	—	ns
t57	ACKI Low to REQ0 High	tACREH	—	43	ns
t58	ACKI Low to Next Data Byte Valid (FIFO bottom full)	tACD	—	78	ns
t59	ACKI High to REQ0 Low (data previously setup)	tACREL	—	45	ns

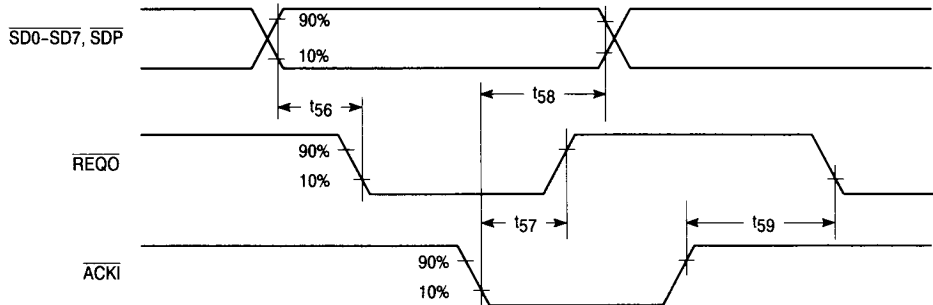


Figure 2.10. Target Asynchronous Send Timing

2.4.12 Target Asynchronous Receive

Time	Parameter	Symbol	Min	Max	Unit
t ₆₀	Data Setup to $\overline{\text{ACKI}}$ Low	t _{su} (SACK)	20	—	ns
t ₆₁	$\overline{\text{ACKI}}$ Low to $\overline{\text{REQO}}$ High	t _{ACREH}	—	43	ns
t ₆₂	$\overline{\text{ACKO}}$ High to $\overline{\text{REQO}}$ Low (FIFO not full)	t _{ACREL}	—	45	ns

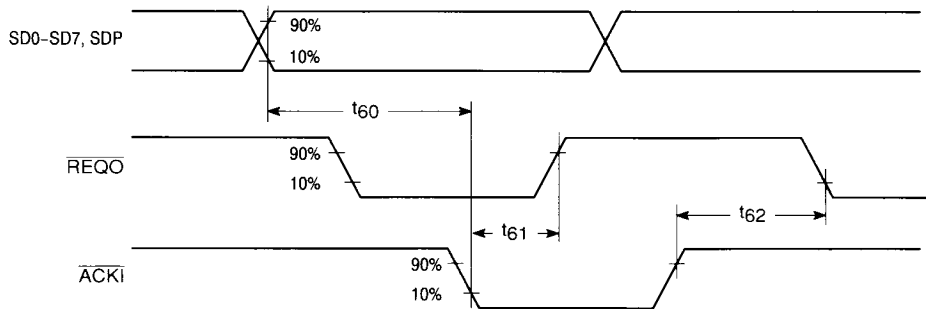


Figure 2.11. Target Asynchronous Receive Timing

2.4.13 Synchronous Receive

Time	Parameter	Symbol	Min	Max	Unit
t63	Data Setup to $\overline{\text{ACKI}}$ Low (Target Mode)	$t_{su}(\text{SACK})$	20	—	ns
t64	Data Hold to $\overline{\text{ACKI}}$ Low (Target Mode)	$t_h(\text{SACK})$	10	—	ns
t65	$\overline{\text{ACKI}}$ Low to $\overline{\text{ACKI}}$ Low Cycle Time (Target Mode)	$t_{cyc}(\text{SACK})$	100	—	ns
t66	$\overline{\text{ACKI}}$ Assertion Period (Target Mode)	$t_{ast}(\text{SACK})$	30	—	ns
t67	$\overline{\text{ACKI}}$ Negation Period (Target Mode)	$t_{neg}(\text{SACK})$	30	—	ns
t68	Data Setup to $\overline{\text{REQI}}$ Low (Initiator Mode)	$t_{su}(\text{SREQ})$	20	—	ns
t69	Data Hold to $\overline{\text{REQI}}$ Low (Initiator Mode)	$t_h(\text{SREQ})$	10	—	ns
t70	$\overline{\text{REQI}}$ Low to $\overline{\text{REQI}}$ Low Cycle Time (Initiator Mode)	$t_{cyc}(\text{SREQ})$	100	—	ns
t71	$\overline{\text{REQI}}$ Assertion Period (Initiator Mode)	$t_{ast}(\text{SREQ})$	30	—	ns
t72	$\overline{\text{REQI}}$ Negation Period (Initiator Mode)	$t_{neg}(\text{SREQ})$	30	—	ns

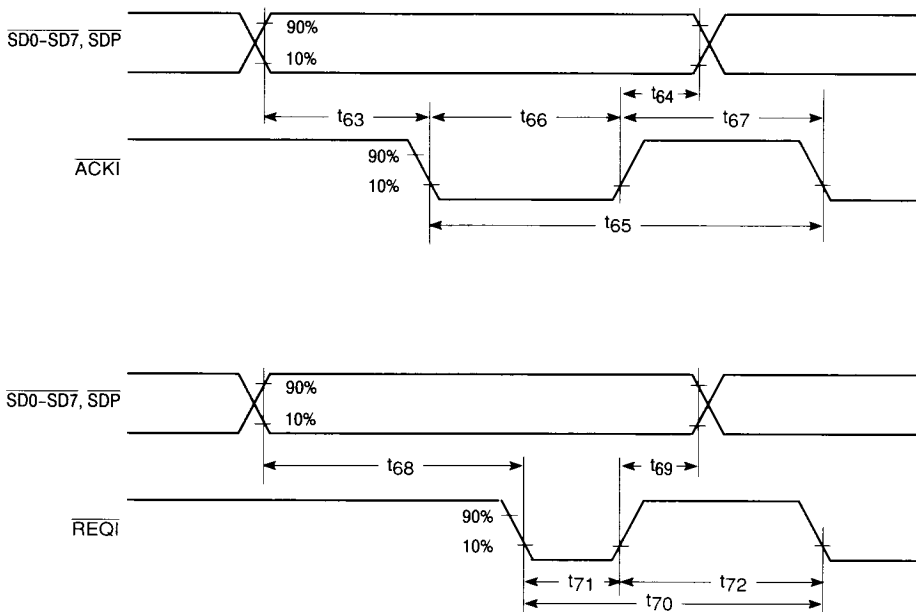


Figure 2.12. Synchronous Receive Timing

2.4.14 Synchronous Transmit (see Note 1)

Time	Parameter	Symbol	Min	Max	Unit
t73	Data Valid from CLOCK High	t _{DCK}	—	60	ns
t74	$\overline{\text{REQ0}}$ Low from CLOCK High (Target Mode)	t _{RELCKH}	—	42	ns
t75	$\overline{\text{REQ0}}$ High from CLOCK High (Target Mode)	t _{REHCKH}	—	42	ns
t76	$\overline{\text{REQ0}}$ Low from CLOCK Low (Target Mode)	t _{RELCKL}	—	42	ns
t77	$\overline{\text{ACK0}}$ Low from CLOCK High (Initiator Mode)	t _{ACLCKH}	—	42	ns
t78	$\overline{\text{ACK0}}$ High from CLOCK High (Initiator Mode)	t _{ACHCKK}	—	42	ns
t79	$\overline{\text{ACK0}}$ Low from CLOCK Low (Initiator Mode)	t _{ACLCKL}	—	42	ns

NOTE:

1. SCSI data setup and hold times are the same as asynchronous transfers.

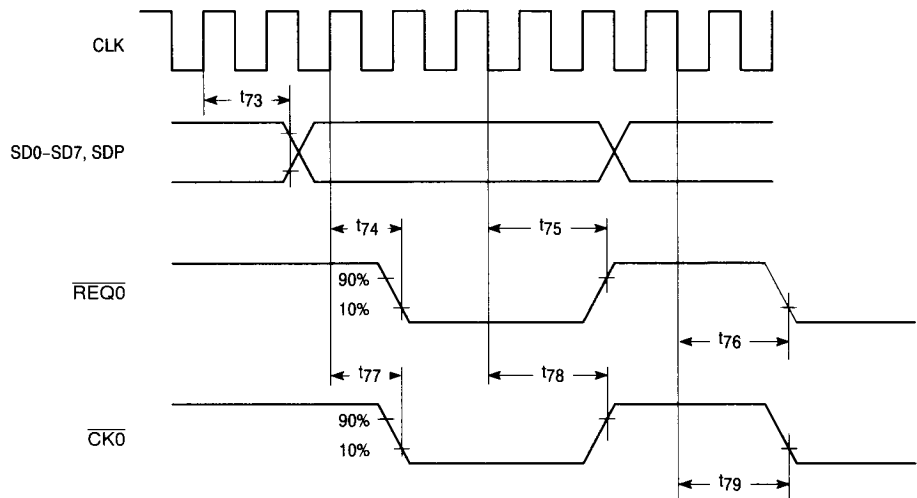


Figure 2.13. Synchronous Transmit Timing