BUK762R0-40C

N-channel TrenchMOS standard level FET

Rev. 02 — 20 August 2007 **Product data sheet**

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using Nexperia Ultra High-Performance Automotive (UHP) TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in Automotive critical applications.

1.2 Features

- 175 °C rated
- Q101 compliant
- Low on-state resistance
- Standard level compatible

1.3 Applications

- 12 V loads
- General purpose power switching
- Automotive systems
- Motors, lamps, solenoids

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; see Figure 1 and 4	[1][2]	-	-	100	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	-	333	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 13 and 12		-	1.7	2	mΩ
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \leq$ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; inductive load type unclamped inductive load		-	-	1.2	J

[1] Continuous current is limited by package.

[2] Refer to document 9397 750 12572 for further information.

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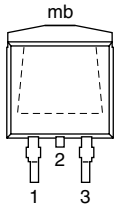
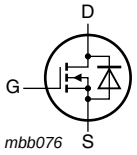
2. Pinning information

Table 2. Pinning

Pin	Symbol	Description	Simplified outline	Graphic Symbol
1	G	gate		
2	D	drain [1]		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK762R0-40C	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	40	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	40	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1 and 4	[1]	-	276	A
		T_{mb} = 100 °C; V_{GS} = 10 V; see Figure 1	[2][3]	-	100	A
		T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 1 and 4	[2][3]	-	100	A
I_{DM}	peak drain current	T_{mb} = 25 °C; $t_p \leq 10$ μs; duty type pulsed; see Figure 4		-	1104	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 2		-	333	W
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 100 A; $V_{sup} \leq 40$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; inductive load type unclamped inductive load		-	1.2	J
$E_{DS(AL)R}$	repetitive drain-source avalanche energy	see Figure 3	[4][5] [6][7]	-	-	J

Table 4. Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I_S	source current	T_{mb} = 25 °C	[1]	-	276	A
		T_{mb} = 25 °C	[2][3]	-	100	A
I_{SM}	peak source current	$t_p \leq 10$ μs; duty type pulsed; T_{mb} = 25 °C		-	1104	A

[1] Current is limited by power dissipation chip rating.

[2] Continuous current is limited by package.

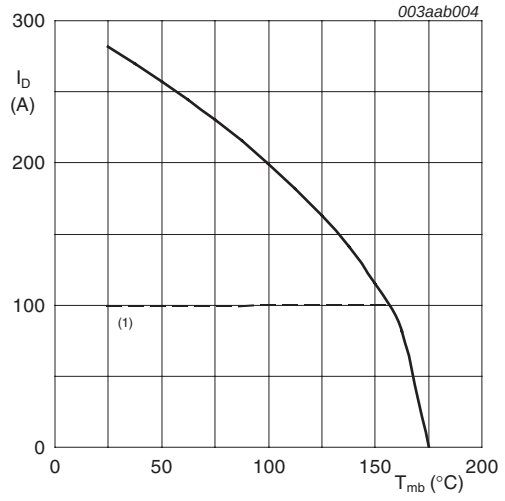
[3] Refer to document 9397 750 12572 for further information.

[4] Maximum value not quoted. Repetitive rating defined in avalanche rating figure.

[5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[6] Repetitive avalanche rating limited by an average junction temperature of 170 °C.

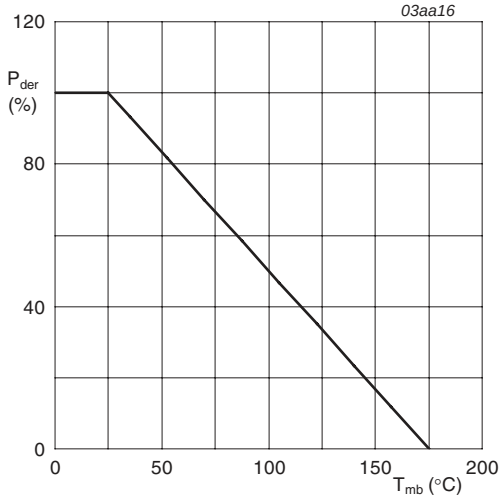
[7] Refer to application note AN10273 for further information.



$V_{GS} \geq 10$ V

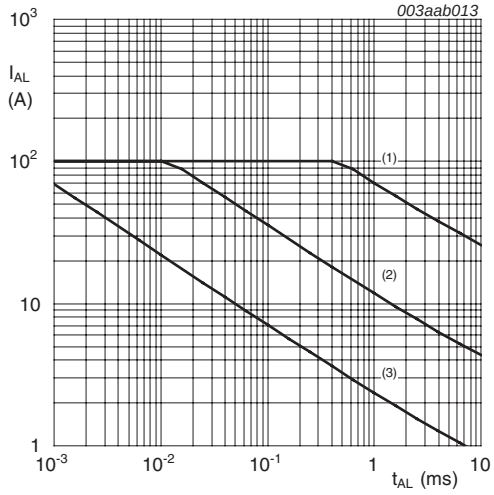
(1) Capped at 100 A due to package.

Fig 1. Continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25\,°C)}} \times 100\ \%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

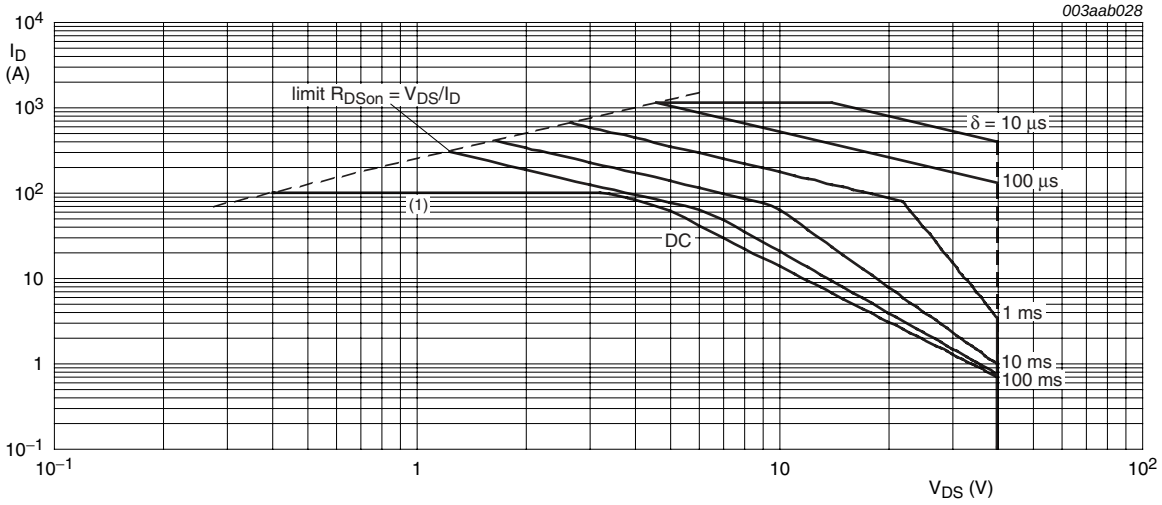


(1) Single−pulse; T_{mb} = 25 °C.

(2) Single−pulse; T_{mb} = 150 °C.

(3) Repetitive.

Fig 3. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time



T_{mb} = 25 °C; I_{DM} is single pulse

(1) Capped at 100 A due to package.

Fig 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; vertical in still air	-	50	-	K/W
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 5	-	-	0.45	K/W

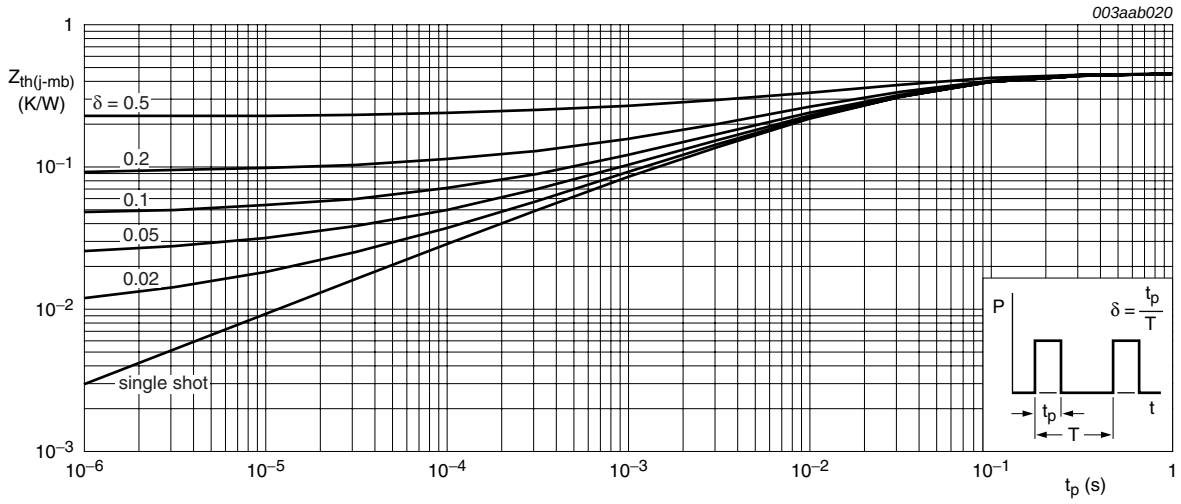


Fig 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

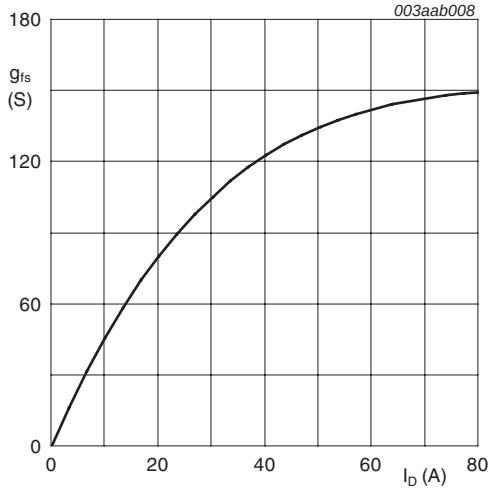
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	40	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	36	-	-	V
V_{GSth}	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10	2	3	4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 11	-	-	4.4	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 11	1	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	µA
		V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA

Table 6. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = 20 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = -20 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; see Figure 12 and 13	-	-	3.75	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 13 and 12	-	1.7	2	mΩ
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 16	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	75	-	ns
Q_r	recovered charge	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = -10 V; V_{DS} = 30 V; T_j = 25 °C	-	57	-	nC
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 14	-	175	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 14	-	38	-	nC
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; see Figure 14	-	67	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	8492	11323	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	1606	1927	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 15	-	1101	1508	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	65	-	ns
t_r	rise time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	133	-	ns
$t_{d(off)}$	turn-off delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	146	-	ns

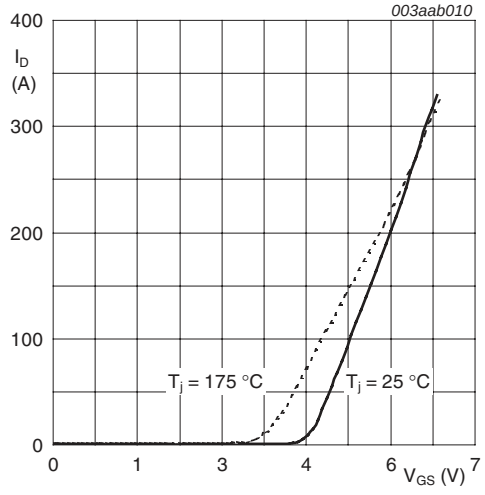
Table 6. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	119	-	ns
L_D	internal drain inductance	from upper edge of drain mounting base to centre of die; T_j = 25 °C	-	2.5	-	nH
L_S	internal source inductance	from source lead 6 mm from package to source bond pad; T_j = 25 °C	-	7.5	-	nH



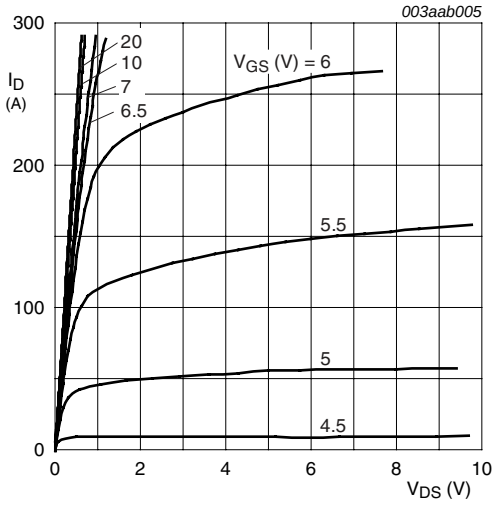
T_j = 25 °C; V_{DS} = 25 V

Fig 6. Forward transconductance as a function of drain current; typical values



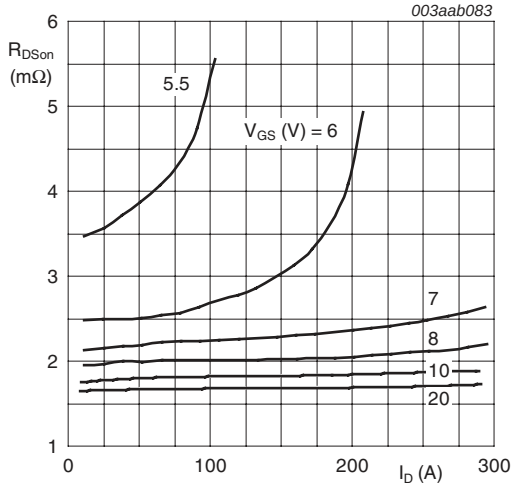
V_{DS} = 25 V

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



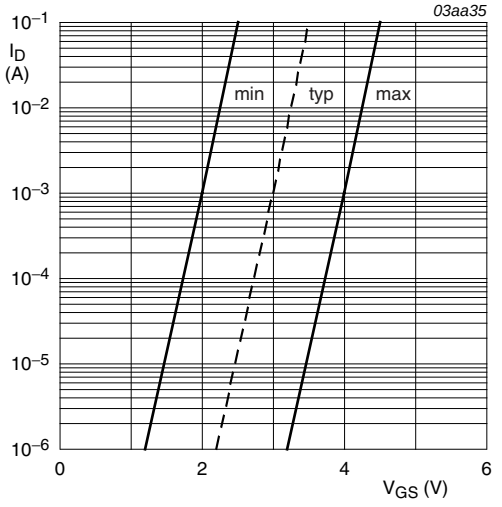
$T_j = 25\ °C$

Fig 8. Output characteristics: drain current as a function of drain-source voltage; typical values



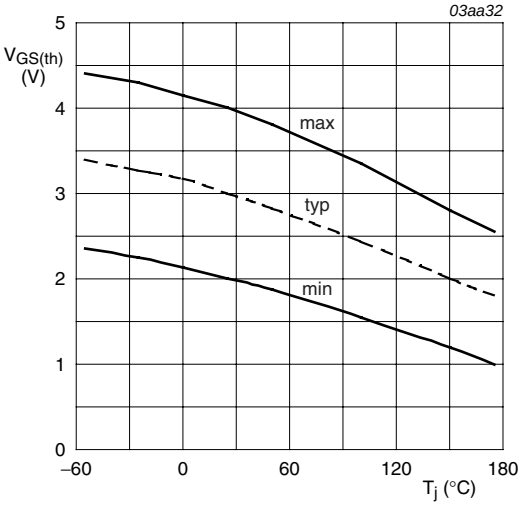
$T_j = 25\ °C$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



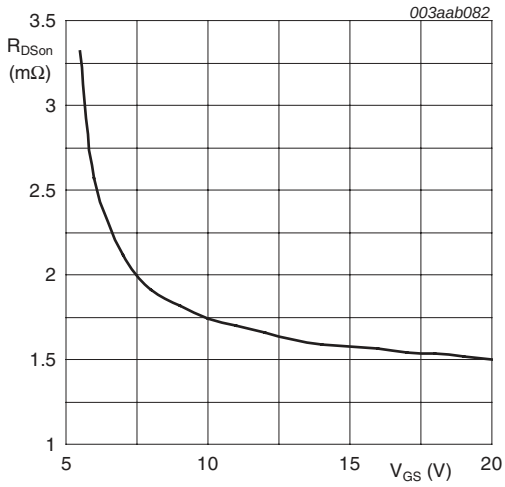
$T_j = 25\ °C; V_{DS} = V_{GS}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



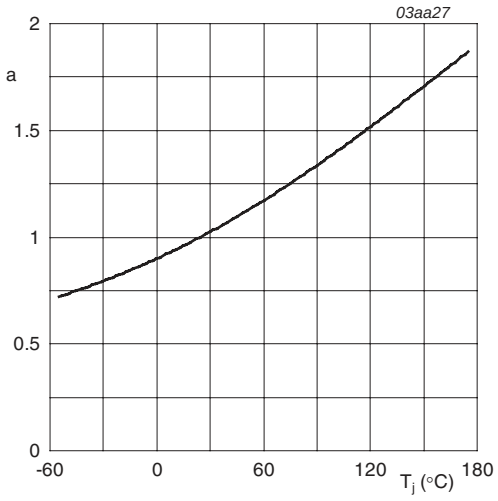
$I_D = 1\ mA; V_{DS} = V_{GS}$

Fig 11. Gate-source threshold voltage as a function of junction temperature



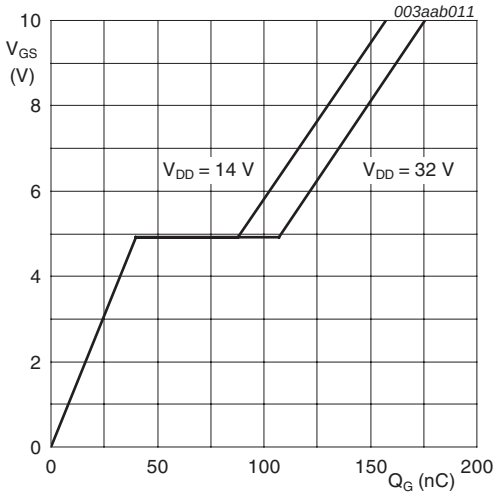
$T_j = 25\ °C$; $I_D = 25\ A$

Fig 12. Drain-source on-state resistance as a function of gate-source voltage; typical values



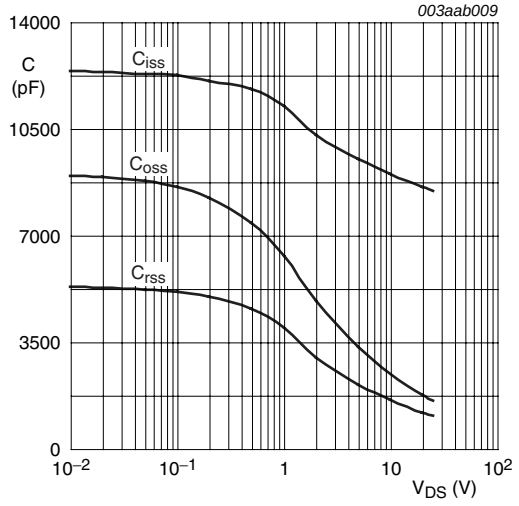
$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature



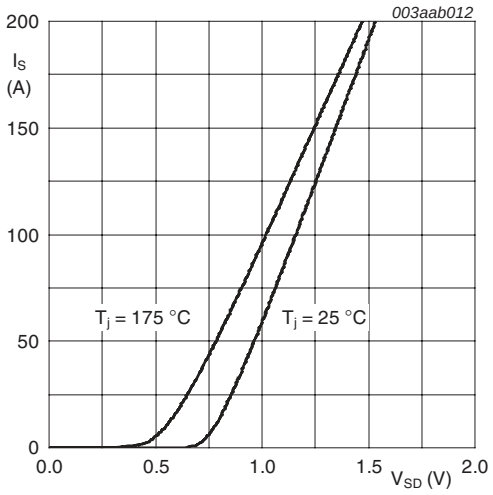
$T_j = 25\ °C$; $I_D = 25\ A$

Fig 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\ V$; $f = 1\ MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

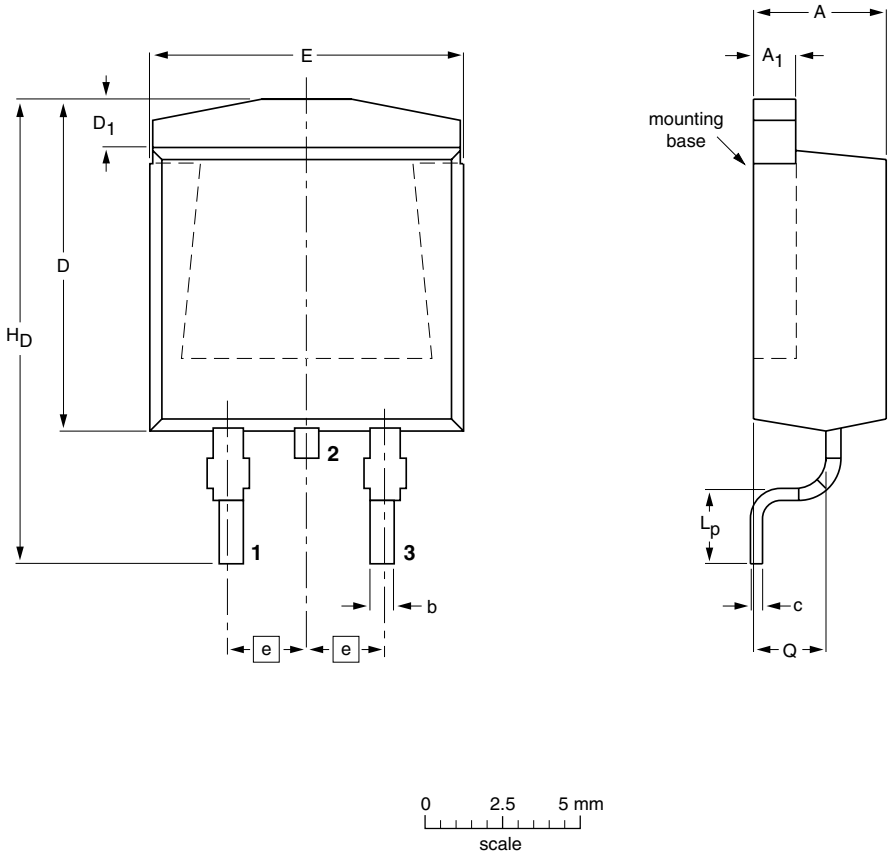


V_{GS} = 0 V

Fig 16. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						~~05-02-11~~ 06-03-16

Fig 17. Package outline SOT404 (D2PAK)

8. Soldering

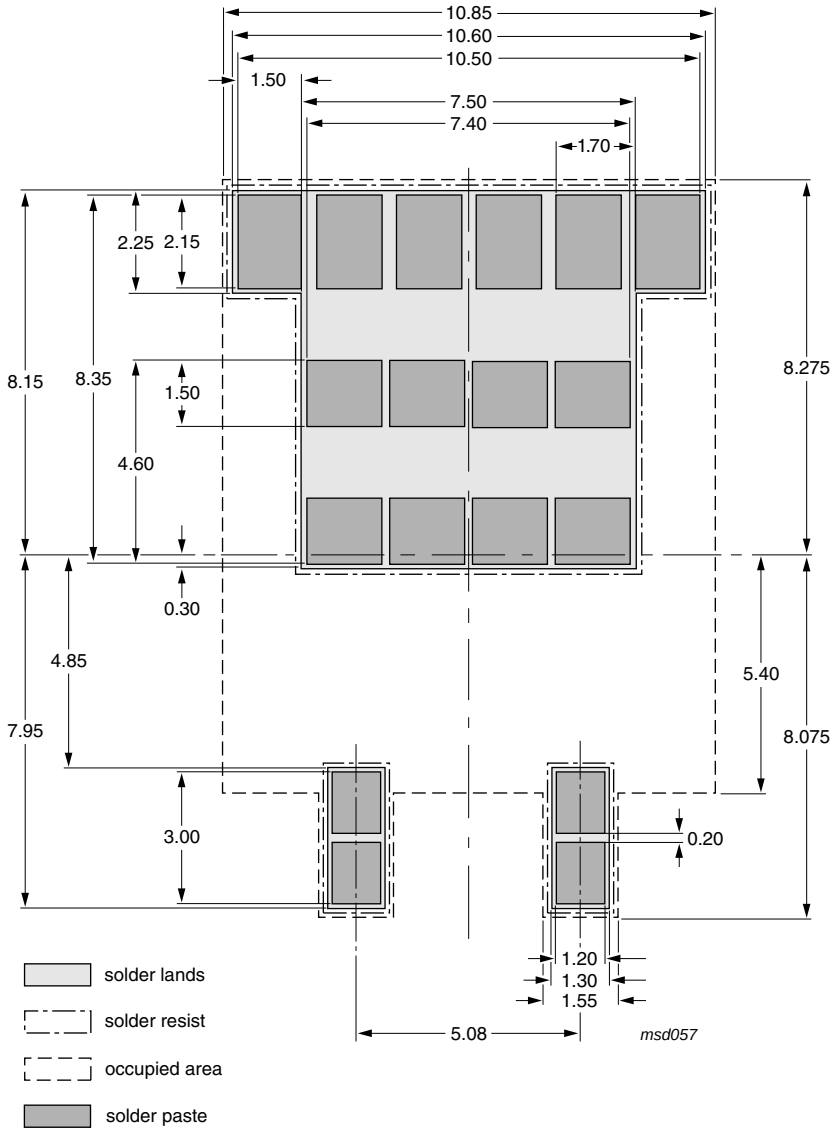


Fig 18. Reflow soldering footprint for SOT404

9. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK762R0-40C_2	20070820	Product data sheet	-	BUK762R0-40C_1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
BUK762R0-40C_1	20060810	Product data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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12. Contents

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Date of release: 20 August 2007