CAT874

Smart Phone Battery Switch Controller

Description

CAT874 is a switch controller designed to start/shut−off smart phones with the push button input or by phone microcontroller unit.

CAT874 monitors two inputs and outputs an active high output after PWR_ON input has been active (logic low) for a factory preset minimum time. Releasing input from its active state before the minimum timeout period resets the internal timer and must return to being active before the timer will restart with a fresh count down. The output remains high until the next PWR_ON high−to−low or V_{CHG} low−to−high transition.

CAT874's push pull output is capable of sinking up to 3 mA of current.

Features

- Operate on 1.8 V to 5.5 V Power Supplies
- Ultra Low Quiescent Current: 100 nA (typical)
- Schmitt Trigger Inputs
- Small µLLGA−6 Package: 1.45 x 1.0 x 0.4 mm
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Mobile Phones
- PDAs
- MP3 Players
- Personal Navigation Devices

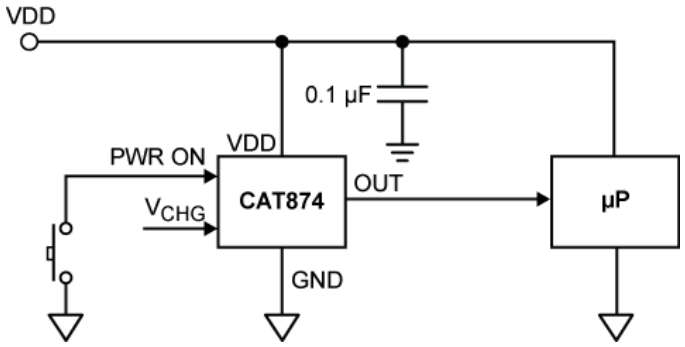

Figure 1. Application Schematic

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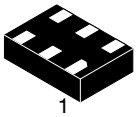
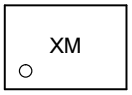


ULLGA−6
UL SUFFIX
CASE 613AF

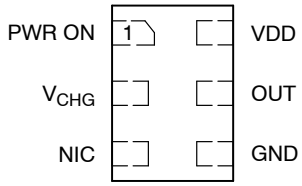
MARKING DIAGRAM



X = Specific Device Code
(d = CAT874)
M = Date Code

"P" written at 180° clockwise rotation

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

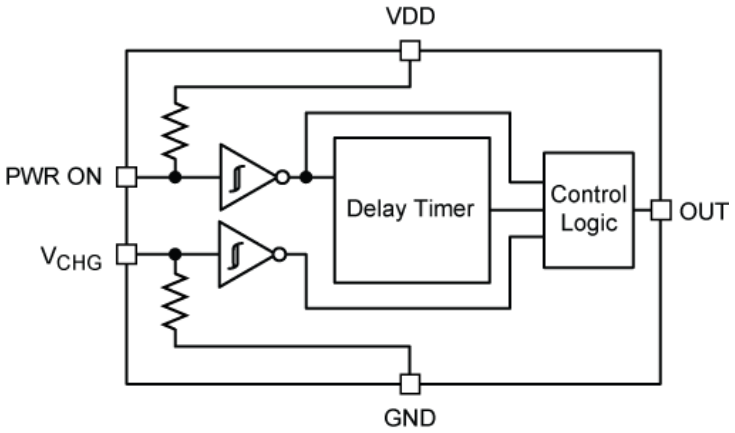


Figure 2. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	PWR_ON	Power ON, CMOS input.
2	V_{CHG}	Charger IN, CMOS input.
3	NIC	No Internal Connection. A voltage or signal applied to this pin will have no effect on device operation.
4	GND	System Ground.
5	OUT	Drive Output. Active−high push−pull output.
6	VDD	Positive Power Supply.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage Range	V_{DD}	−0.3 to 6	V
Output Voltage Range	V_{OUT}	−0.3 to 6 or (V_{DD} + 0.3), whichever is lower	V
Input Voltage; PWR_ON, V_{CHG}	V_{IN}	−0.3 to 6 or (V_{DD} + 0.3), whichever is lower	V
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Output Current; OUT	I_{OUT}	10	mA
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2	kV
ESD Capability, Machine Model (Note 2)	ESD_{MM}	150	V
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 2)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latch−up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

Table 3. RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Input Voltage; VDD	V_{DD}	1.8	5.5	V
Input Voltage; PWR_ON, V_{CHG}	V_{IN}	0	V_{DD}	V
Output Current; OUT	I_{OUT}	0	3	mA
Ambient Temperature	T_A	−40	85	°C

Table 4. ELECTRICAL OPERATING CHARACTERISTICS
(V_{DD} = 1.8 V to 5.5 V. For typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
POWER						
V_{DD} Supply Voltage		V_{DD}	1.8		5.5	V
Quiescent Supply Current	PWR_ON = VDD, V_{CHG} = 0 V	I_{DD}		100	1000	nA
Operating Supply Current	PWR_ON = 0 V, V_{CHG} = 0 V Measured during setup period. Measurement includes current through internal 200 kΩ pull−up resistor on PWR_ON				50	μA
LOGIC INPUTS AND OUTPUTS						
Input Voltage; HIGH	PWR_ON, V_{CHG}	V_{IH}	0.7 x V_{DD}			V
Input Voltage; LOW	PWR_ON, V_{CHG}	V_{IL}			0.25 x V_{DD}	V
Hysteresis		V_{HYS}		250		mV
Input Current V_{CHG}	V_{CHG} = 0 V; V_{DD} = 5 V (internal pull−down)	I_{IL1}		50	300	nA
Input Current V_{CHG}	V_{CHG} = 5 V; V_{DD} = 5 V (internal pull−down)	I_{IH1}		25		μA
Input Current PWR_ON	PWR_ON = 0 V; V_{DD} = 5 V (internal 200 kΩ pull−up resistor)	I_{IL2}		25		μA
Input Current PWR_ON	PWR_ON = 5 V; V_{DD} = 5 V (internal 200 kΩ pull−up resistor)	I_{IH2}		50	300	nA
Output Voltage; HIGH	I_{SOURCE} = −0.1 mA, V_{DD} = 1.8 V	V_{OH}	V_{DD} − 0.2			V
Output Voltage; LOW	I_{SINK} = 3 mA, V_{DD} = 1.8 V	V_{OL}		0.1	0.4	V
TIMING						
Input Delay PWR_ON	T_A = 25°C	t_{low_delay}	6.56	8.00	9.44	s
	T_A = −40°C to +85°C		6.00		10.00	
TEST MODE (V_{DD} = 5 V, T_A = 25°C) (Note 3)						
Start TEST Window		t_{ST}			35	μs
Test Mode Delay	PWR_ON = 0 V, V_{CHG} → 7 cycles, delay measured after 8th rising edge of V_{CHG} clock pulse	t_D		250		μs
Test Mode Clock Frequency	Clock applied to V_{CHG}	f_{tm}		1		MHz
PWR_ON Test Mode Clock Setup Time	Measured from PWR_ON falling edge to first falling edge of V_{CHG}	t_P	1			μs
V_{CHG} Input Voltage; LOW	V_{CHG}, Test Mode Operation	V_{IL_TM}			0.2 x V_{DD}	V
V_{CHG} Pulse Width		t_{pw}		500		ns

3. “Test Mode” parameters are not tested in production.

TIMING WAVEFORMS

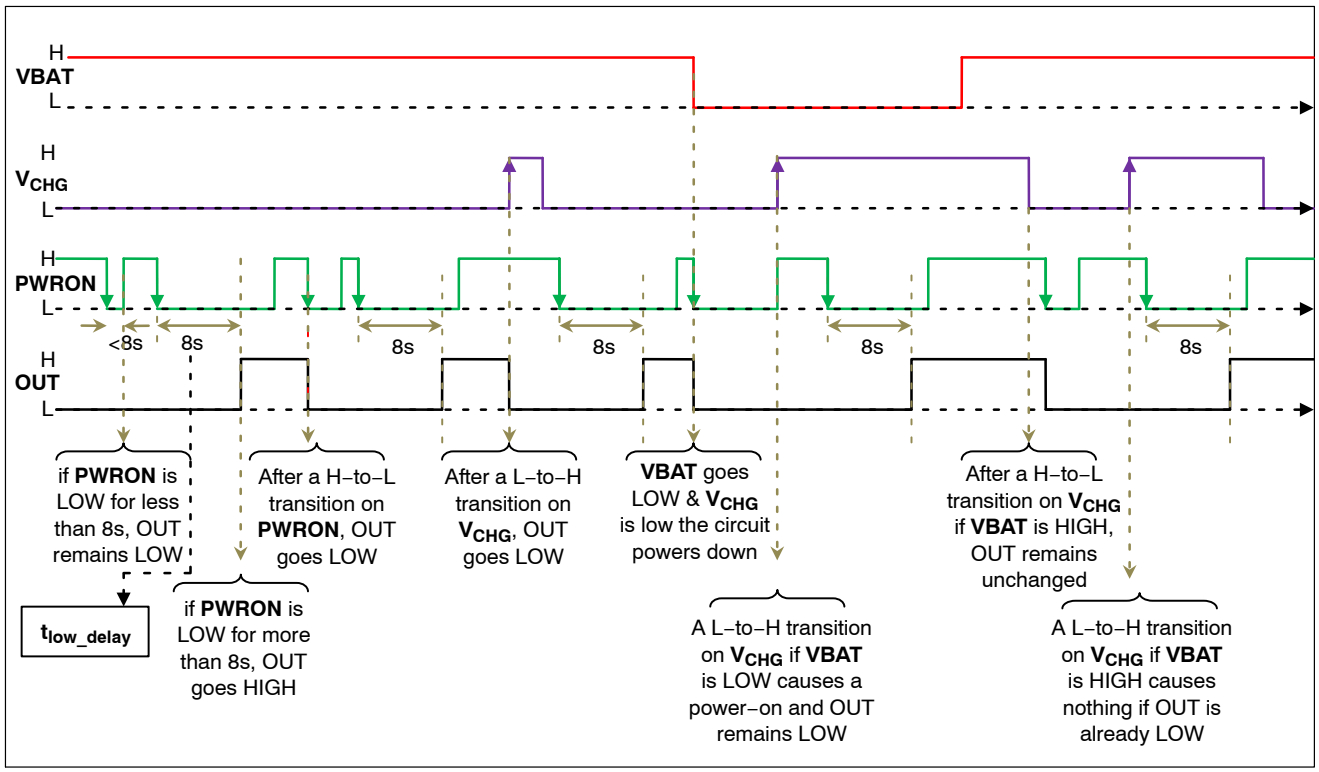


Figure 3. Timing Waveforms

SYSTEM DESCRIPTION AND APPLICATIONS INFORMATION

General

CAT874 is designed for the manual switching of microprocessors and microcontrollers. To prevent accidental resets, CAT874 requires PWR_ON input be held low for a prescribed period before an Active high output is issued to the system processor.

PWR_ON and V_{CHG} Inputs

PWR_ON and V_{CHG} are Schmitt trigger CMOS inputs. PWR_ON must go low and stay low for a predetermined period (t_{LOW_DELAY}) to generate an Active high on the output.

V_{CHG} is a standard CMOS input with internal pull down resistor 200 kΩ to keep the input low when charger is not plugged in and PWR_ON is also a CMOS input with an internal 200 kΩ pull−up resistor, thus PWR_ON can be left floating.

When PWR_ON goes low, an internal timing cycle is initiated. If it goes high before the countdown timer has concluded its cycle, the timer will reset and will restart from the beginning when PWR_ON returns to being low.

Output (OUT)

CAT874 provides an active−high push pull output. This output will sink up to 3 mA.

Delay Timer Testing:

A user test mode is provided to reduce the system test time after the CAT874 is mounted on the board. Instead of waiting t_{LOW_DELAY} for the output to go active.

The user brings PWR_ON low, and sends seven positive edges on the V_{CHG} pin in a window of time t_{ST}. After a delay t_D, the device output will change state from low to high, and will return to the low state only when there is a high−to−low transition on PWR_ON.

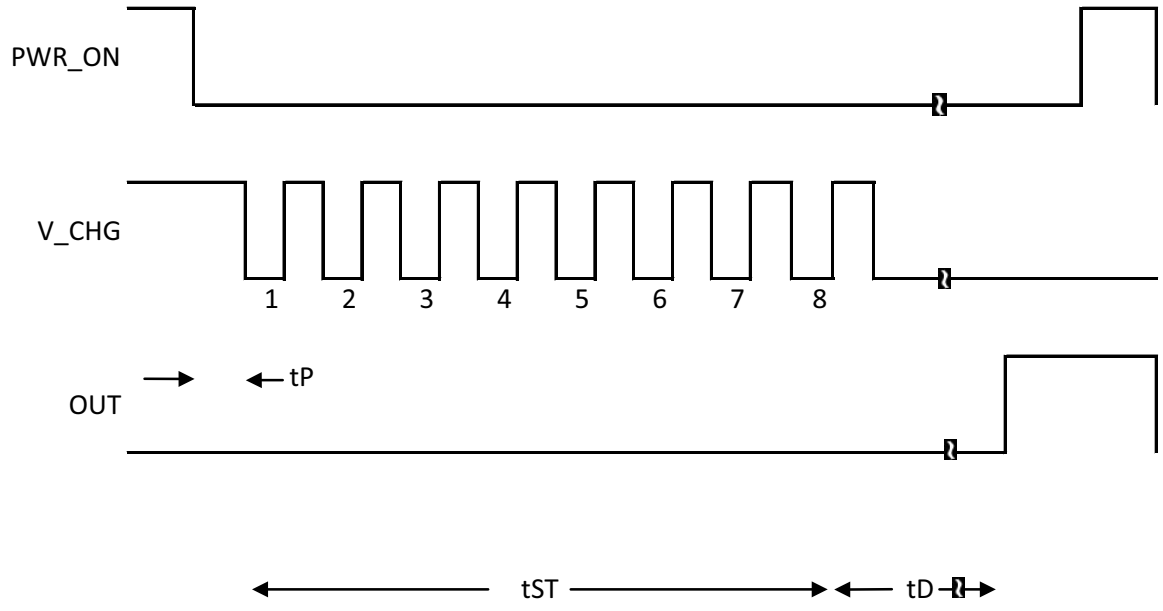


Figure 4. TOC Mode

APPLICATION INFORMATION

Output Operation

System with Two Different Power Supply Voltages

When both V_{CHG} and VBAT are present, the following application can be adapted. Schottky diodes D1 and D2 can be used to isolate the two sources. The higher source will supply the VDD power.

If V_{CHG} is not present then drop across D2 should be low enough to turn off Q1. If both V_{CHG} and VBAT are present, the timing waveforms should be used as shown in Figure 4.

An external resistor 1M should be used OUT, to discharge the output when both sources turn off.

Operation with Low VDD Voltage and Brownout Condition

The CAT874 requires a minimum supply voltage VDD of 1.8 V to guarantee the normal operation within the specification. To prevent small VDD supply glitch, a small ceramic capacitor can be added between the VDD pin and GND.

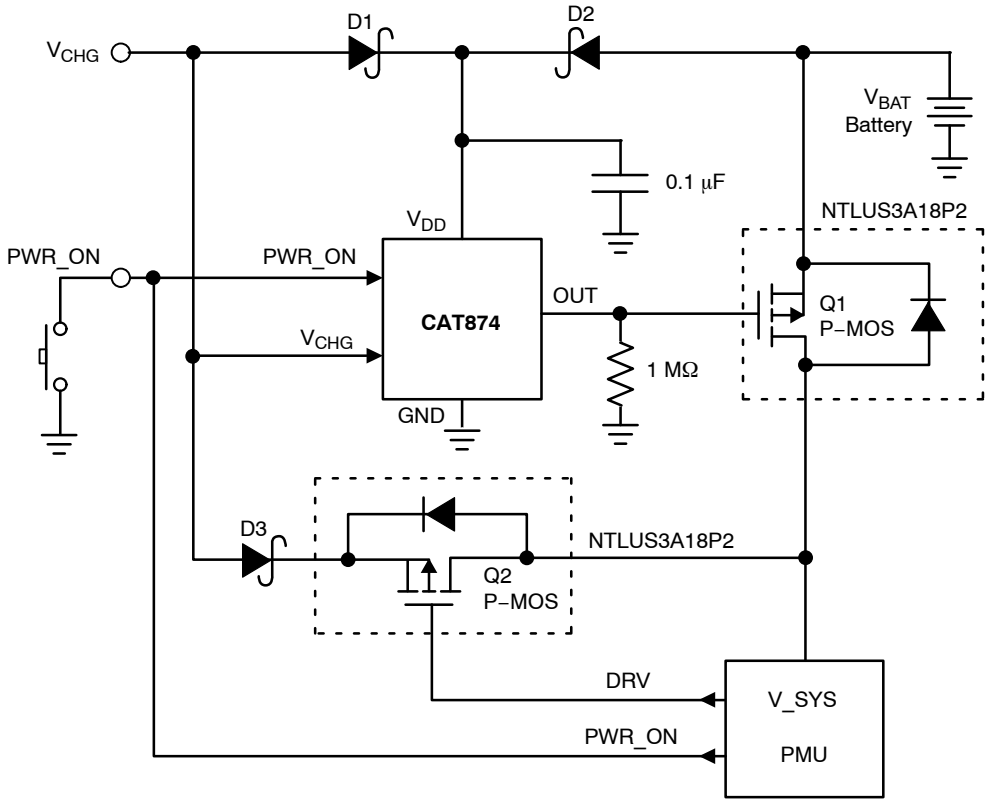
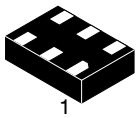


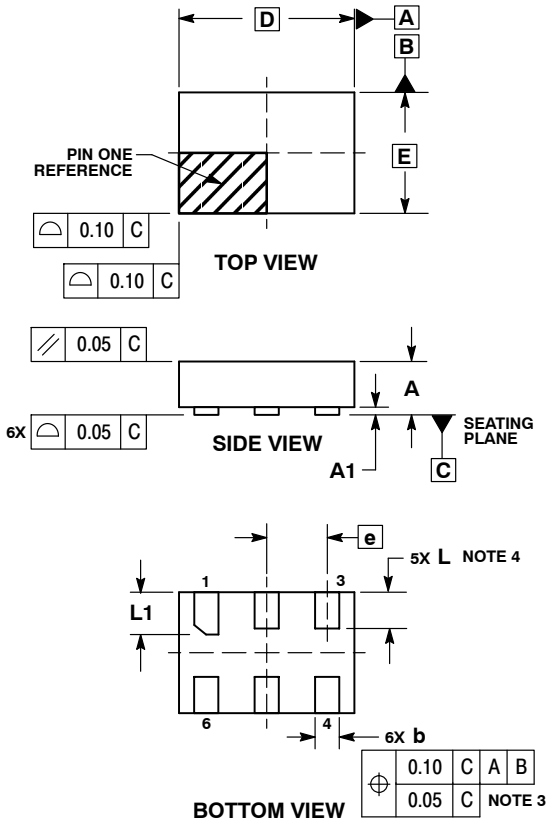
Figure 5. Application Schematic in Dual Supply System

ULLGA6, 1.45x1.0, 0.5P
CASE 613AF−01
ISSUE A

DATE 06 FEB 2008



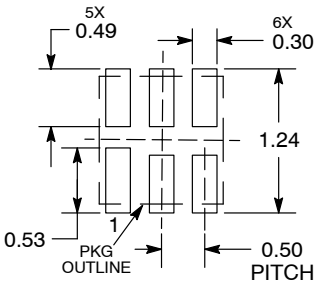
SCALE 8:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
4. A MAXIMUM OF 0.05 PULL BACK OF THE PLATED TERMINAL FROM THE EDGE OF THE PACKAGE IS ALLOWED.

	MILLIMETERS	
DIM	MIN	MAX
A	−−−	0.40
A1	0.00	0.05
b	0.15	0.25
D	1.45 BSC	
E	1.00 BSC	
e	0.50 BSC	
L	0.25	0.35
L1	0.30	0.40

MOUNTING FOOTPRINT
SOLDERMASK DEFINED*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**ULLGA6, 1.45X1.0, 0.5P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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