

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
  - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

# SN74LS90



ON Semiconductor®

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## DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to  $\overline{CP}$ ) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects

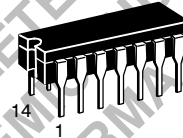
## DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER LOW POWER SCHOTTKY

### PIN NAMES

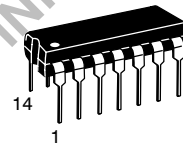
|  |   | LOADING (Note a) |              |
|--|---|------------------|--------------|
|  |   | HIGH             | LOW          |
| $\overline{CP}_0$                                | Clock (Active LOW going edge) Input to +2 Section                           | 0.5 U.L.         | 1.5 U.L.     |
| $\overline{CP}_1$                                | Clock (Active LOW going edge) Input to +5 Section (LS90), +6 Section (LS92) | 0.5 U.L.         | 2.0 U.L.     |
| $\overline{CP}_1$                                | Clock (Active LOW going edge) Input to +8 Section (LS93)                    | 0.5 U.L.         | 1.0 U.L.     |
| MR <sub>1</sub> , MR <sub>2</sub>                | Master Reset (Clear) Inputs   | 0.5 U.L.         | 0.25 U.L.    |
| MS <sub>1</sub> , MS <sub>2</sub>                | Master Set (Preset-9, LS90) Inputs  | 0.5 U.L.         | 0.25 U.L.    |
| Q <sub>0</sub>                                   | Output from +2 Section (Notes b & c)  | 10 U.L.          | 5 (2.5) U.L. |
| Q <sub>1</sub> , Q <sub>2</sub> , Q <sub>3</sub> | Outputs from +5 (LS90), +6 (LS92), +8 (LS93) Sections (Note b)              | 10 U.L.          | 5 (2.5) U.L. |

### NOTES:

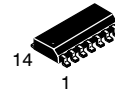
- 1 TTL Unit Load (U.L.) = 40  $\mu$ A HIGH/1.6 mA LOW.
- The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
- The Q<sub>0</sub> Outputs are guaranteed to drive the full fan-out plus the  $\overline{CP}_1$  input of the device.
- To insure proper operation the rise (t<sub>r</sub>) and fall time (t<sub>f</sub>) of the clock must be less than 100 ns.



J SUFFIX  
CERAMIC  
CASE 632-08



N SUFFIX  
PLASTIC  
CASE 646-06

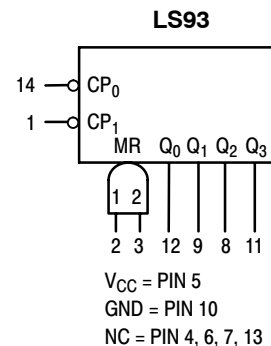
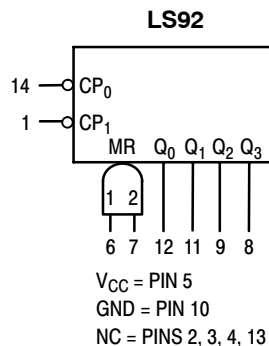
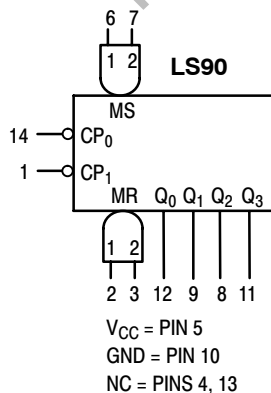


D SUFFIX  
SOIC  
CASE 751A-02

### ORDERING INFORMATION

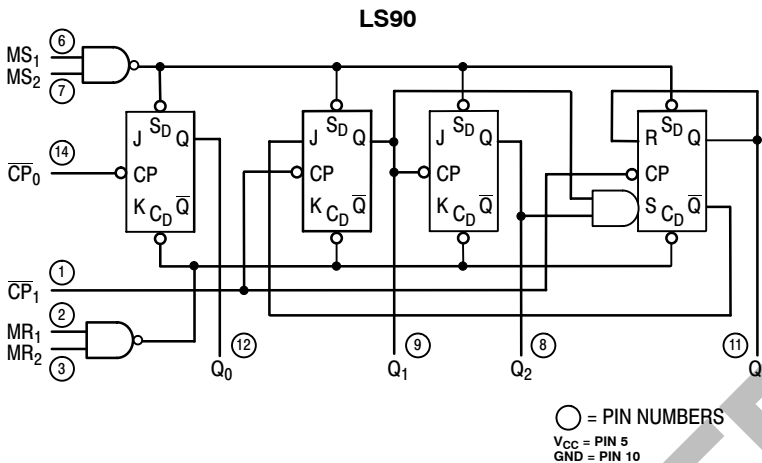
|           |         |
|-----------|---------|
| SN54LSXXJ | Ceramic |
| SN74LSXXN | Plastic |
| SN74LSXXD | SOIC    |

### LOGIC SYMBOL



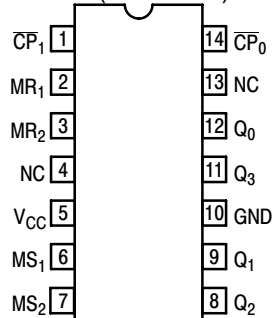
# SN74LS90

## LOGIC DIAGRAM



## CONNECTION DIAGRAM

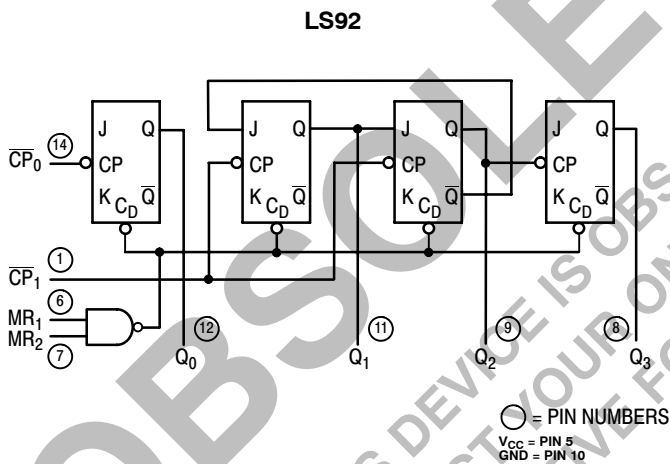
### DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

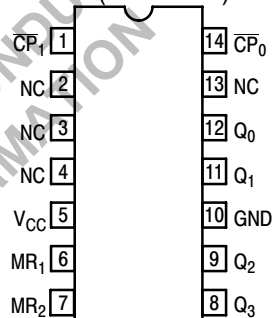
**NOTE:**  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

## LOGIC DIAGRAM



## CONNECTION DIAGRAM

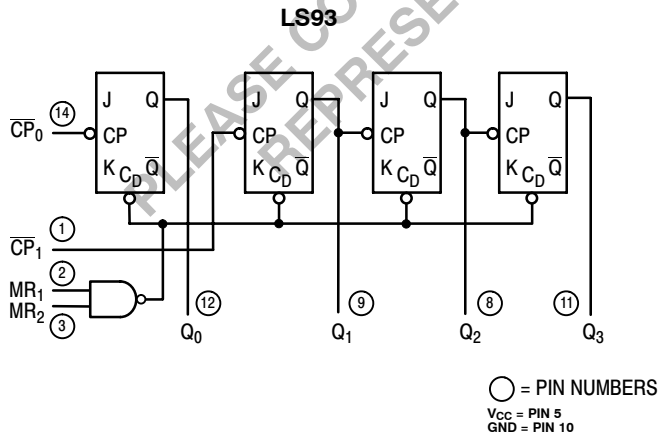
### DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

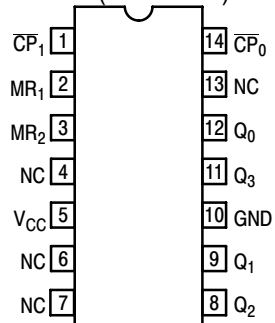
**NOTE:**  
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## LOGIC DIAGRAM



## CONNECTION DIAGRAM

### DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

**NOTE:**  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

**FUNCTIONAL DESCRIPTION**

The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The  $Q_0$  output of each device is designed and specified to drive the rated fan-out plus the  $\overline{CP}_1$  input of the device.

A gated AND asynchronous Master Reset ( $MR_1 \cdot MR_2$ ) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ( $MS_1 \cdot MS_2$ ) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

**LS90**

- A. BCD Decade (8421) Counter — The  $\overline{CP}_1$  input must be externally connected to the  $Q_0$  output. The  $\overline{CP}_0$  input receives the incoming count and a BCD count sequence is produced.
- B. Symmetrical Bi-quinary Divide-By-Ten Counter — The  $Q_3$  output must be externally connected to the  $\overline{CP}_0$  input. The input count is then applied to the  $\overline{CP}_1$  input and a divide-by-ten square wave is obtained at output  $Q_0$ .

- C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ( $\overline{CP}_0$  as the input and  $Q_0$  as the output). The  $\overline{CP}_1$  input is used to obtain binary divide-by-five operation at the  $Q_3$  output.

**LS92**

- A. Modulo 12, Divide-By-Twelve Counter — The  $\overline{CP}_1$  input must be externally connected to the  $Q_0$  output. The  $\overline{CP}_0$  input receives the incoming count and  $Q_3$  produces a symmetrical divide-by-twelve square wave output.
- B. Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The  $\overline{CP}_1$  input is used to obtain divide-by-three operation at the  $Q_1$  and  $Q_2$  outputs and divide-by-six operation at the  $Q_3$  output.

**LS93**

- A. 4-Bit Ripple Counter — The output  $Q_0$  must be externally connected to input  $\overline{CP}_1$ . The input count pulses are applied to input  $\overline{CP}_0$ . Simultaneous divisions of 2, 4, 8, and 16 are performed at the  $Q_0$ ,  $Q_1$ ,  $Q_2$ , and  $Q_3$  outputs as shown in the truth table.
- B. 3-Bit Ripple Counter — The input count pulses are applied to input  $\overline{CP}_1$ . Simultaneous frequency divisions of 2, 4, and 8 are available at the  $Q_1$ ,  $Q_2$ , and  $Q_3$  outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.



# SN74LS90

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol          | Parameter  |        | Limits |       |      | Unit | Test Conditions   |
|-----------------|--|--------|--------|-------|------|------|---|
|                 |  |        | Min    | Typ   | Max  |      |   |
| V <sub>IH</sub> | Input HIGH Voltage   |        | 2.0    |       |      | V    | Guaranteed Input HIGH Voltage for All Inputs  |
| V <sub>IL</sub> | Input LOW Voltage  | 54     |        |       | 0.7  | V    | Guaranteed Input LOW Voltage for All Inputs   |
|                 |  | 74     |        |       | 0.8  |      |   |
| V <sub>IK</sub> | Input Clamp Diode Voltage  |        |        | -0.65 | -1.5 | V    | V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA   |
| V <sub>OH</sub> | Output HIGH Voltage  | 54     | 2.5    | 3.5   |      | V    | V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table  |
|                 |  | 74     | 2.7    | 3.5   |      | V    |   |
| V <sub>OL</sub> | Output LOW Voltage   | 54, 74 |        | 0.25  | 0.4  | V    | I <sub>OL</sub> = 4.0 mA<br>I <sub>OL</sub> = 8.0 mA<br>V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table |
|                 |  | 74     |        | 0.35  | 0.5  | V    |   |
| I <sub>IH</sub> | Input HIGH Current   |        |        |       | 20   | μA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V  |
|                 |  |        |        |       | 0.1  | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V  |
| I <sub>IL</sub> | Input LOW Current<br>MS, MR<br>CP <sub>0</sub><br>CP <sub>1</sub> (LS90, LS92)<br>CP <sub>1</sub> (LS93) |        |        |       | -0.4 | mA   | V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V  |
|                 |  |        |        |       | -2.4 |      |   |
|                 |  |        |        |       | -3.2 |      |   |
|                 |  |        |        |       | -1.6 |      |   |
| I <sub>OS</sub> | Short Circuit Current (Note 1)   |        | -20    |       | -100 | mA   | V <sub>CC</sub> = MAX   |
| I <sub>CC</sub> | Power Supply Current   |        |        |       | 15   | mA   | V <sub>CC</sub> = MAX   |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

# SN74LS90

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V, C<sub>L</sub> = 15 pF)

| Symbol                               | Parameter  | Limits |          |          |      |          |          |      |          |          | Unit |
|--------------------------------------|--|--------|----------|----------|------|----------|----------|------|----------|----------|------|
|                                      |  | LS90   |          |          | LS92 |          |          | LS93 |          |          |      |
|                                      |  | Min    | Typ      | Max      | Min  | Typ      | Max      | Min  | Typ      | Max      |      |
| f <sub>MAX</sub>                     | CP <sub>0</sub> Input Clock Frequency                                | 32     |          |          | 32   |          |          | 32   |          |          | MHz  |
| f <sub>MAX</sub>                     | CP <sub>1</sub> Input Clock Frequency                                | 16     |          |          | 16   |          |          | 16   |          |          | MHz  |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | Propagation Delay,<br>CP <sub>0</sub> Input to Q <sub>0</sub> Output |        | 10<br>12 | 16<br>18 |      | 10<br>12 | 16<br>18 |      | 10<br>12 | 16<br>18 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | CP <sub>0</sub> Input to Q <sub>3</sub> Output                       |        | 32<br>34 | 48<br>50 |      | 32<br>34 | 48<br>50 |      | 46<br>46 | 70<br>70 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | CP <sub>1</sub> Input to Q <sub>1</sub> Output                       |        | 10<br>14 | 16<br>21 |      | 10<br>14 | 16<br>21 |      | 10<br>14 | 16<br>21 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | CP <sub>1</sub> Input to Q <sub>2</sub> Output                       |        | 21<br>23 | 32<br>35 |      | 10<br>14 | 16<br>21 |      | 21<br>23 | 32<br>35 | ns   |
| t <sub>PLH</sub><br>t <sub>PHL</sub> | CP <sub>1</sub> Input to Q <sub>3</sub> Output                       |        | 21<br>23 | 32<br>35 |      | 21<br>23 | 32<br>35 |      | 34<br>34 | 51<br>51 | ns   |
| t <sub>PLH</sub>                     | MS Input to Q <sub>0</sub> and Q <sub>3</sub> Outputs                |        | 20       | 30       |      |          |          |      |          |          | ns   |
| t <sub>PHL</sub>                     | MS Input to Q <sub>1</sub> and Q <sub>2</sub> Outputs                |        | 26       | 40       |      |          |          |      |          |          | ns   |
| t <sub>PHL</sub>                     | MR Input to Any Output   |        | 26       | 40       |      | 26       | 40       |      | 26       | 40       | ns   |

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

| Symbol           | Parameter                   | Limits |     |      |     |      |     | Unit |
|------------------|-----------------------------|--------|-----|------|-----|------|-----|------|
|                  |                             | LS90   |     | LS92 |     | LS93 |     |      |
|                  |                             | Min    | Max | Min  | Max | Min  | Max |      |
| t <sub>W</sub>   | CP <sub>0</sub> Pulse Width | 15     |     | 15   |     | 15   |     | ns   |
| t <sub>W</sub>   | CP <sub>1</sub> Pulse Width | 30     |     | 30   |     | 30   |     | ns   |
| t <sub>W</sub>   | MS Pulse Width              | 15     |     |      |     |      |     | ns   |
| t <sub>W</sub>   | MR Pulse Width              | 15     |     | 15   |     | 15   |     | ns   |
| t <sub>rec</sub> | Recovery Time MR to CP      | 25     |     | 25   |     | 25   |     | ns   |

RECOVERY TIME (t<sub>rec</sub>) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs

## AC WAVEFORMS

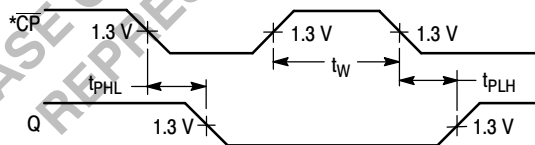


Figure 1

\*The number of Clock Pulses required between the t<sub>PHL</sub> and t<sub>PLH</sub> measurements can be determined from the appropriate Truth Tables.

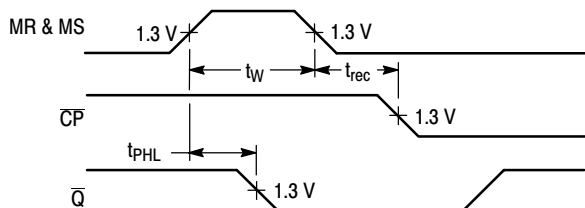


Figure 2

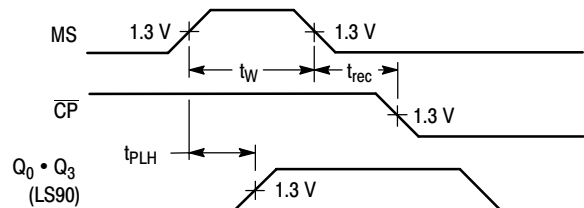


Figure 3

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