SC2608A
Simple, Synchronous Voltage Mode PWM Controller

Description

The SC2608A is a versatile voltage-mode PWM controller designed for use in step down DC/DC power supply applications. A simple, fixed frequency, highly efficient buck regulator can be implemented using the SC2608A with minimal external components. The input voltage range is from +5V to +12V. Internal level shift and drive circuitry eliminates the need for an expensive P-channel, high-side MOSFET. The small device footprint allows for compact circuit design.

SC2608A features include temperature compensated voltage reference, triangle wave oscillator, current limit comparator, and an externally compensated error amplifier. Current limit is implemented by sensing the voltage drop across the bottom MOSFET $R_{DS(ON)}$.

The SC2608A operates at a fixed frequency of 250kHz providing an optimum compromise between efficiency , external component size, and cost.

SC2608A has a thermal protection circuit, which is activated if the junction temperature exceeds 150 ^{o}C.

Features

- +5V or +12V input voltage
- 250kHz operation
- High efficiency (>90%)
- 1.5% Reference voltage accuracy
- Hiccup mode over current protection
- Robust output drive
- $R_{DS(ON)}$ Current sensing for protection
- Industrial temperature range
- SO-8 package
- Integrated boot strap diode
- Thermal Shut down
- Fully WEEE and RoHS Compliant

Applications

- Termination supplies
- Low cost microprocessor supplies
- Peripheral card supplies
- Industrial power supplies
- High density DC/DC conversion

Typical Application Circuit

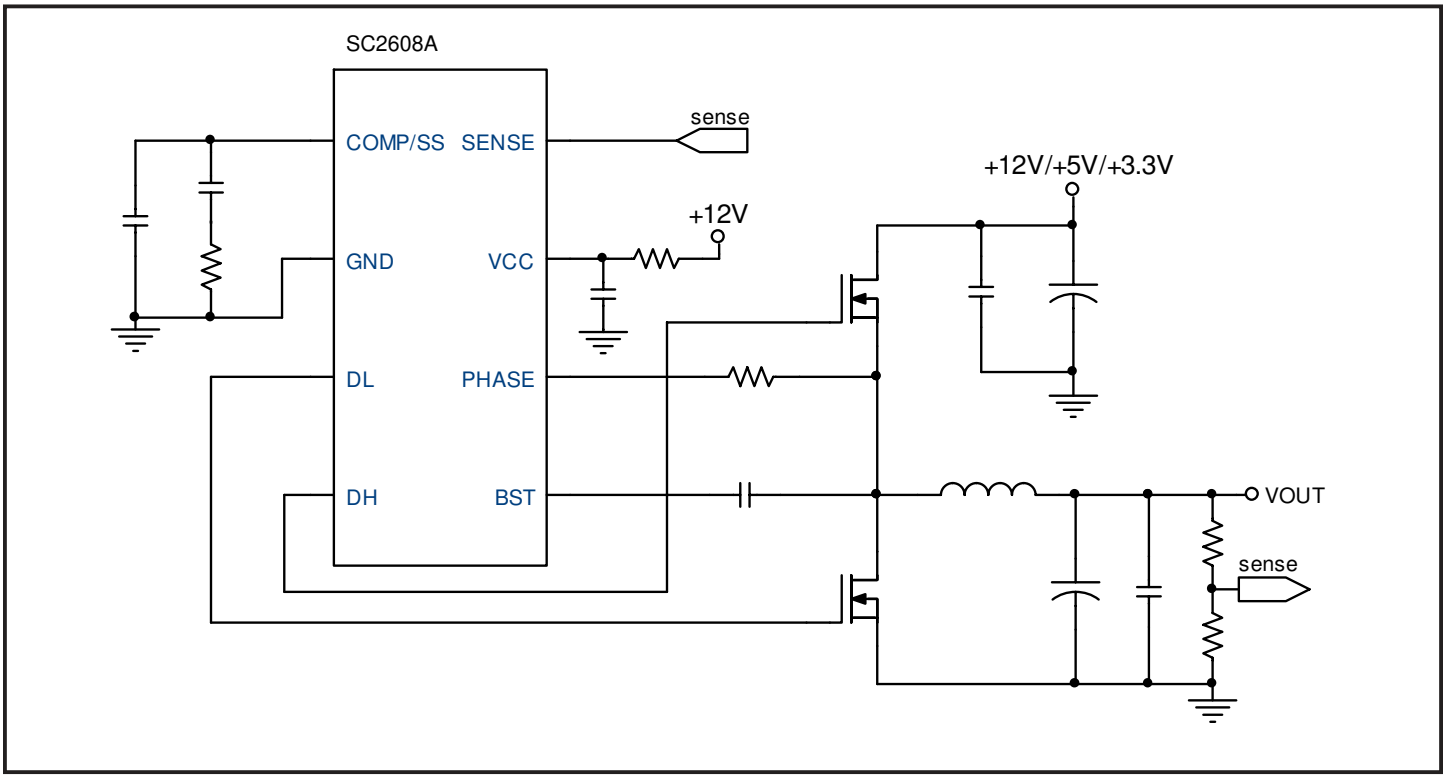


Figure 1

Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
V_{CC} to GND		+20	V
BST to PHASE		+15	V
BST to GND		+35	V
PHASE to GND (note1)		-1 to +24	V
DH to PHASE (note1)		+15	V
DL to GND (note2)		-1 to +15	V
COMP/SS to GND		+7	V
SENSE to GND		+7	V
Thermal Resistance Junction to Case	θ_{JC}	40	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	120	°C/W
Operating Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
ESD Rating (Human Body Model)	ESD	2	kV

Note 1: Under pulsing condition, the peak negative voltage can not be lower than -3.6V with less than 20nS from 50% to 50%.
Note 2: Under pulsing condition, the peak negative voltage can not be lower than -5V with less than 20nS from 50% to 50%.

Electrical Characteristics

Unless specified: V_{CC} = 12V, V_{BST} - V_{Phase} = 12 V, V_{OUT} = 3.3V, T_J = T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply						
Supply Voltage	V_{CC}		4.5		14	V
Supply Current	I_{CC}	V_{COMP} < 0.4V		6		mA
Error Amplifier						
Feedback Voltage	V_{FB}	4.75V<Vcc<12.6V 0°C < T_A < 85 °C	0.788	0.8	0.812	V
		-40 °C < T_A < 125 °C		0.8		V
E/A Transconductance	G_m			7		mS
Open Loop DC Gain	A_O			60		dB
Input Bias Current	I_{FB}			1	3	uA
Output Sink Current	I_{SINK}	V_{SENSE} > 0.9V; V_{COMP} = 2.1V		-700		uA
Output Source Current	I_{SOURCE}	V_{SENSE} < 0.7V; V_{COMP} = 2.1V		120		uA

Electrical Characteristics

Unless specified: V_{CC} = 12V, V_{BST} - V_{Phase} = 12 V, V_{OUT} = 3.3V, T_J = T_A = 25°C.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Oscillator						
Switching Frequency	F_{OSC}	Vcc =12V	225	250	275	kHz
Ramp Peak Voltage	V_{P-K}	4.75V < V_{CC} < 12.6V		1.8		V
Ramp Valley Voltage	V_V	4.75V < V_{CC} < 12.6V		0.8		V
Maximum Duty Cycle	D_{MAX}	250kHz		85		%
MOSFET Drivers						
DH Sink/Source Current	I_{DH}	t_{PW} > 400nS V_{GS} = 4.5V (src)	0.6	0.8		A
DL Sink/Source Current	I_{DL}	V_{GS} = 2.5V (snk)	0.6	0.7		A
DH Rise/Fall Time	tr, tf	C_L = 3000pF, See Fig. 2		50		ns
DL Rise/Fall Time	tr, tf	C_L = 4000pF, See Fig. 2		50		ns
Dead Time	t_{dt}	See Fig. 2		80		ns
DL Minimum On Time	t_{ON}	4.75V < Vcc < 12.6V		400		ns
Current Limit						
Trip Voltage	V_{TRIP}	4.75V < Vcc < 12.6V V_{trip} = V_{PHASE} - GND	-400	-350	-300	mV
Soft-Start						
SS Source Current	I_{SRC}	V_{COMP} < 2.5V		6		uA
SS Sink Current	I_{SNK}	V_{COMP} > 0.5V		-6		uA
Under voltage Lockout						
UVLO Threshold	V_{th}	-40< T_J < 85°C	3.9	4.1	4.3	V
Thermal Shutdown						
Over Temperature Trip Point	T_{OTP}			150		°C

Gate Drive Timing Diagram

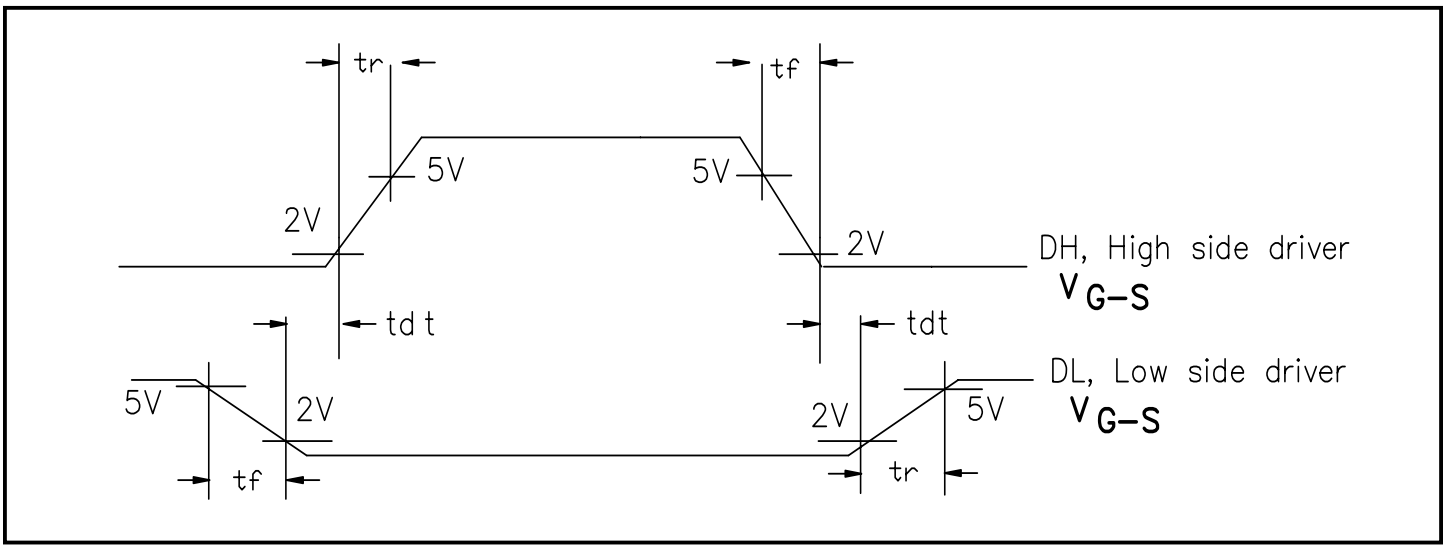


Figure 2

Block Diagram

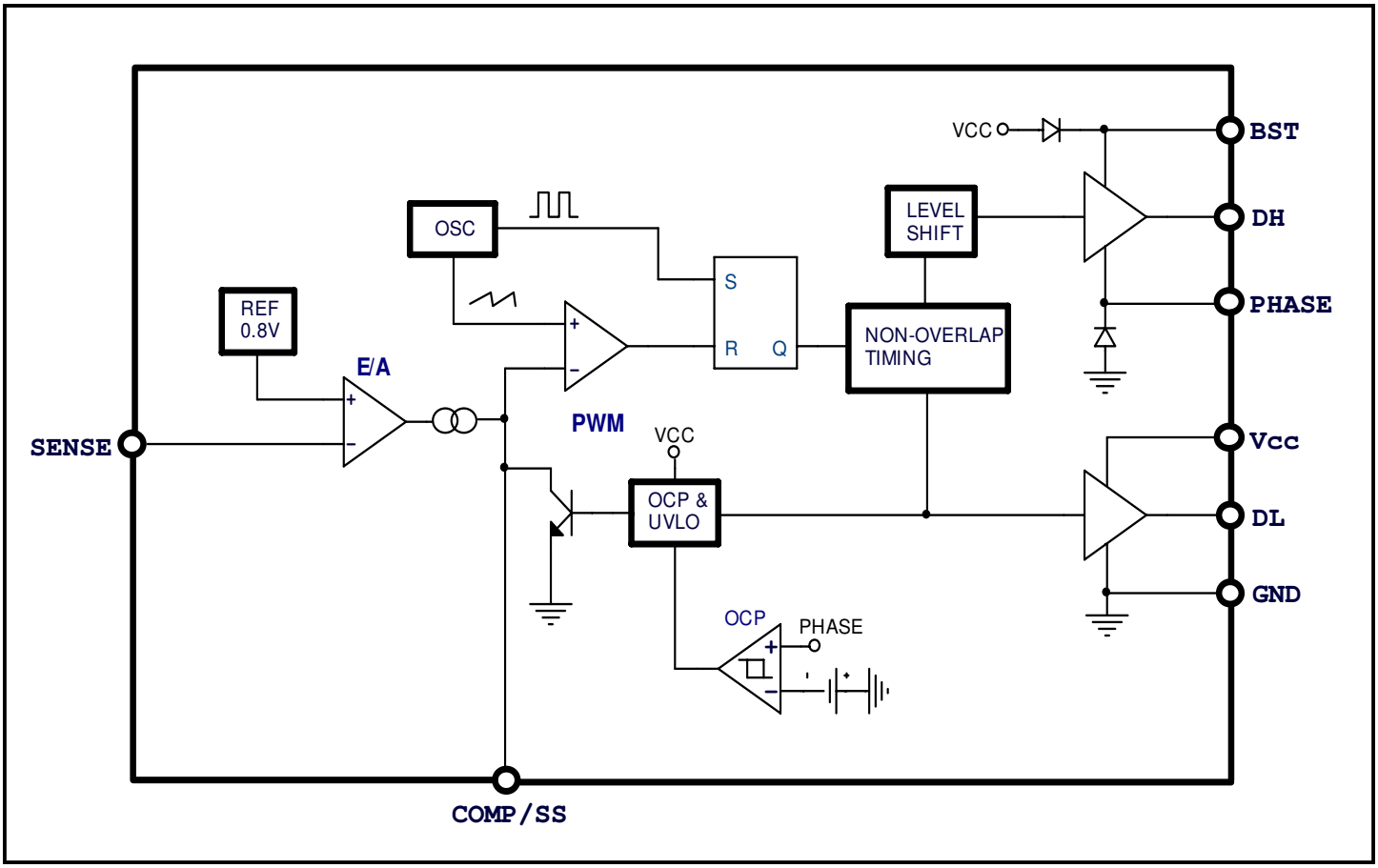
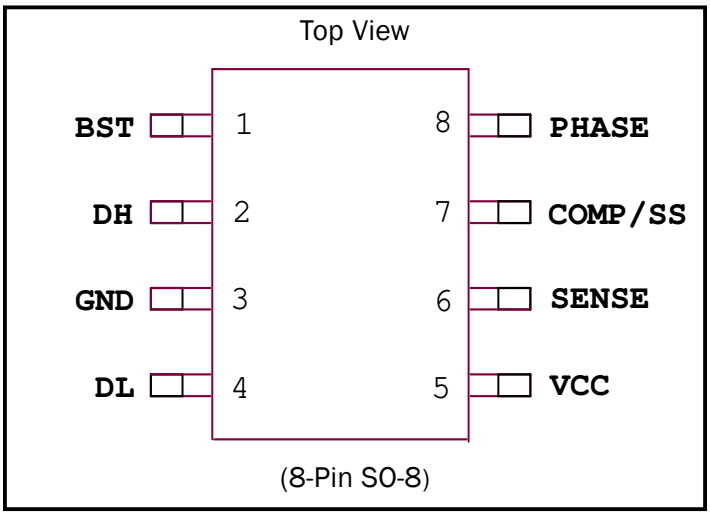


Figure 3

Pin Configuration



Ordering information

Device (1)	Package	Temp Range (T_J)
SC2608ASTRT(2)	SO-8	-40 to 125°C
SC2608AEVB	Evaluation Board	

Notes:
(1) Only available in tape and reel packaging. A reel contains 2500 devices.
(2) This device is fully WEEE and RoHS Compliant

Pin Descriptions

Pin #	Pin Name	Pin Function
1	BST	Bootstrap for high side driver.
2	DH	High side driver output.
3	GND	Ground.
4	DL	Low side driver output.
5	VCC	Chip bias supply pin.
6	Sense	Output voltage sense input.
7	COMP/SS	Error amplifier output. Connect compensation network to GND. The compensation capacitor serves as soft start capacitor. By pulling this pin low will disable the output.
8	PHASE	Connect this pin to the switching node between the MOSFETs.

Theory of Operation

Synchronous Buck Converter

The output voltage of the synchronous converter is set and controlled by the output of the error amplifier. The inverting input of the error amplifier receives its voltage from the SENSE pin. The non-inverting input of the error amplifier is connected to an internal 0.8V reference. The error amplifier output is connected to the compensation pin. The error amplifier generates a current proportional to (0.8V-Vsense), which is the COMP pin output current (Transconductance ~ 7mS). The voltage on the COMP pin is the integral of the error amplifier current. The COMP voltage is the non-inverting input of the PWM comparator and controls the duty cycle of the MOSFET drivers. The compensation network controls the stability and transient response of the regulator. The larger capacitor, the slower COMP voltage changes, and slower the duty cycle changes.

The non-inverting input voltage of the PWM comparator is the triangular ramp signal generated from the oscillator. The peak-to-peak voltage of the ramp is 1V, this is a parameter used in control loop calculation. When the oscillator ramp signal rises above the COMP voltage, the comparator output goes high and the PWM latch is reset. This pulls DH low, turning off the high-side MOSFET. After a short delay (dead time), DL is pulled high, turning on the low-side MOSFET. The oscillator also produces a set pulse for the PWM latch to turn off the low-side MOSFET, After a delay time, DH is pulled high to turn on the high-side MOSFET. The delay time is determined by a monostable on the chip.

The triangle wave minimum is about 0.8V, and the maximum is about 1.8V. Thus, if Vcomp = 0.7V, high side duty cycle is the minimum (~0%) , but if Vcomp is 1.8V, duty cycle is at maximum (~90%).The internal oscillator uses an on-chip capacitor and trimmed precision current sources to set the oscillation frequency to 250kHz. Figure 1 shows a 2.5V output converter. If the Vout <2.5V, then the SENSE voltage < 0.8V. In this case the error amplifier will be sourcing current into the COMP pin so that COMP voltage and duty cycle will gradually increase.If Vout > 2.5V, the error amplifier will sink current and reduce the COMP voltage, so that duty cycle will decrease.The circuit will be in steady state when Vout =2.5V , Vsense = 0.8V, Icomp = 0. The COMP voltage and duty cycle depend on Vin.

Under Voltage Lockout

The under voltage lockout circuit of the SC2608A assures that both high-side and low-side MOSFET driver outputs remain in the off state whenever the supply voltage drops below the set threshold. Lockout occurs if V_{CC} falls below 4.1V typ.

Soft Start

The SC2608A provides a soft start function to prevent large inrush currents upon power-up or hiccup retry. If both COMP and SENSE pins are low (<300mV), the device enters soft start mode, and the compensation capacitor is slowly charged by an internal 6uA current source. When the COMP pin reaches 300mV, the low side FET is switched on in order to refresh the bootstrap capacitor, and begin PWM from a known state. As the COMP pin rises above 800mV, PWM begins at minimum duty cycle.

COMP continues to charge, slowly sweeping the device through the duty cycle range until FB reaches the regulation point of 800mV. Once FB reaches the regulation point, the soft start current is switched off, and the strong error amp is enabled, providing a glitch-free entrance into closed loop operation. The overcurrent comparator is still active during soft start mode, and will override soft start in the event that an overcurrent is detected, such as startup into a dead short.

$R_{DS(ON)}$ Current Limiting

In case of a short circuit or overload, the low-side (LS) FET will conduct large currents. To protect the regulator in this situation, the controller will shut down the regulator and begin a soft start cycle later. While the LS driver is on,the Phase voltage is compared to the OCP trip voltage. If the phase voltage is lower than OCP trip voltage, an over current condition is detected. The low-side R_{dson} sense is implemented at end of each LS-FET turn-on duration. The minimum turn-on time of the LS-FET is set to be 400nS. This will ensure the sampled signal is noise free by giving enough time for the switching noise to die down.

OCP Hiccup

In the event that an overcurrent is detected, the SC2608A latches the fault and begins a hiccup cycle. Switching is immediately stopped, and the drivers are set to a tristate condition (Both DH and DL are low). COMP is slowly discharged to 300mV with an internal 6uA current source, providing a long cooldown time to keep power dissipation low in the event of a continuous dead short. Once COMP and SENSE both fall below the 300mV threshold, the part re-enables the 6uA soft start current , and the device begins a normal startup cycle again.

Applications Information (Cont.)

A note to the user is needed: The device cannot restart until both COMP and SENSE are low, to prevent start up into a charged output. In the event of an overcurrent condition, the output is quickly discharged by the load, therefore bringing SENSE below the 300mV threshold. If the COMP pin is pulled low by an external device (such as an open-drain logic gate used for system shutdown), and SENSE is high(above 300mV) while COMP is low, then the SC2608A turns on the low side FET to discharge the output before changing to shutdown or soft-start mode. The low side FET turns off when SENSE drops below 300mV and the converter remains in the tri-state condition until COMP is released. Although this shutdown technique can be used successfully on the SC2608A, the system designer using COMP for external shutdown will need to consider the load on the low side FET when discharging the output capacitor bank. For large capacitor bank, this peak current can be quite large as it is limited only by the $R_{DS(ON)}$ of the low side FET. Fortunately the duration of this event is quite short, and has been shown in the lab to have no detrimental effect on the performance of the external FETs.

Disabling the output by pulling down COMP/SS pin is only recommended when the output capacitor bank is not too large.

Compensation Network Design

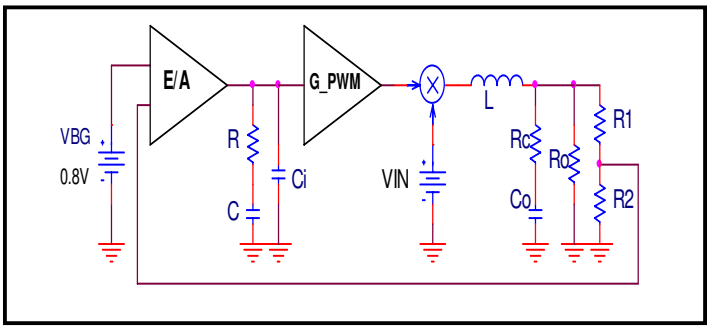


Fig. 4. SC2608A small signal model.

The control model of SC2608A is depicted in Fig. 4. This model can also be used to generate loop gain Bode plots. The bandgap reference is 0.8V and trimmed to +/-1% accuracy. The desired output voltage can be achieved by setting the resistive divider network, R1 and R2. The error amplifier is transconductance type with fixed gain of:

$$G_m = \frac{0.007\ A}{V}$$

The compensation network includes a resistor and a capacitor in series, which terminates the output of the error amplifier to the ground.

The PWM gain is inversion of the ramp amplitude, and this gain is given by:

$$G_{pwm} = \frac{1}{V_{ramp}}$$

where the ramp amplitude is fixed at 1 volts.

The total control loop-gain can then be derived as follows:

$$T(s) = G_m \bullet G_{pwm} \bullet V_{in} \bullet \left(\frac{V_{bg}}{V_o}\right) \bullet H_c(s) \bullet \frac{1 + sR_cC_o}{1 + s\left(R_cC_o + \frac{L}{R_o}\right) + s^2LC_o\left(1 + \frac{R_c}{R_o}\right)}$$

$$H_c(s) = \frac{1}{\frac{1}{R + \frac{1}{sC}} + sC_i}$$

The task here is to properly choose the compensation network for a nicely shaped loop-gain Bode plot. The following design procedures are recommended to accomplish the goal:

(1) Calculate the corner frequency of the output filter:

$$F_o = \frac{1}{2\pi\sqrt{LC_o}}$$

(2) Calculate the ESR zero frequency of the output filter capacitor:

$$F_{esr} = \frac{1}{2\pi R_cC_o}$$

(3) Check that the ESR zero frequency is not too high.

$$F_{esr} < \frac{F_{SW}}{5}$$

If this condition is not met, the compensation structure may not provide loop stability. The solution is to add some electrolytic capacitors to the output capacitor bank to correct the output filter corner frequency and the ESR zero frequency. In some cases, the filter inductance may also need to be adjusted to shift the filter corner frequency. It is not recommended to use only high frequency multi-layer ceramic capacitors for output filter.

(4) Choose the loop gain cross over frequency (0 dB frequency). It is recommended that the crossover frequency is always less than one fifth of the switching frequency :

$$F_{X\_OVER} = \frac{1}{5} \bullet F_{SW}$$

If the transient specification is not stringent, it is better to choose a crossover frequency that is less than one tenth of the switching frequency for good noise immunity. The resistor in the compensation network can then be calculated as:

$$R = \frac{1}{G_{pwm} \bullet V_{in} \bullet G_m} \bullet \left(\frac{F_{esr}}{F_o}\right)^2 \bullet \left(\frac{F_{X\_OVER}}{F_{esr}}\right) \bullet \left(\frac{V_o}{V_{bg}}\right)$$

when

$$F_o < F_{esr} < \frac{F_{sw}}{5}$$

Applications Information (Cont.)

(5) The compensation capacitor is determined by choosing the compensator zero to be about one fifth of the output filter corner frequency:

$$F_{zero} = \frac{F_o}{5}$$

$$C = \frac{1}{2\pi R \bullet F_{zero}}$$

SC2608A soft start time is determined by the compensation capacitor. Capacitance can be adjusted to satisfy the soft start requirement.

(6) The final step is to generate the Bode plot by using the simulation model in Fig. 4 or using the equations provided here with Mathcad. The phase margin can then be checked using the Bode plot.

An example is given below to demonstrate the procedure introduced above.

V_{in}=12V
V_o=2.5V
I_o=15A
F_{sw}=250KHz
L=2.2uH
C_o=4400uF
R_c=0.009Ω
V_{bg}=0.8V
V_{ramp}=1V
G_m=0.007A/V

set C_i=1nF
R_c=1.33KΩ set to R_c=1.5KΩ
C=327.95nF set to C=100nF

for suitable soft start time

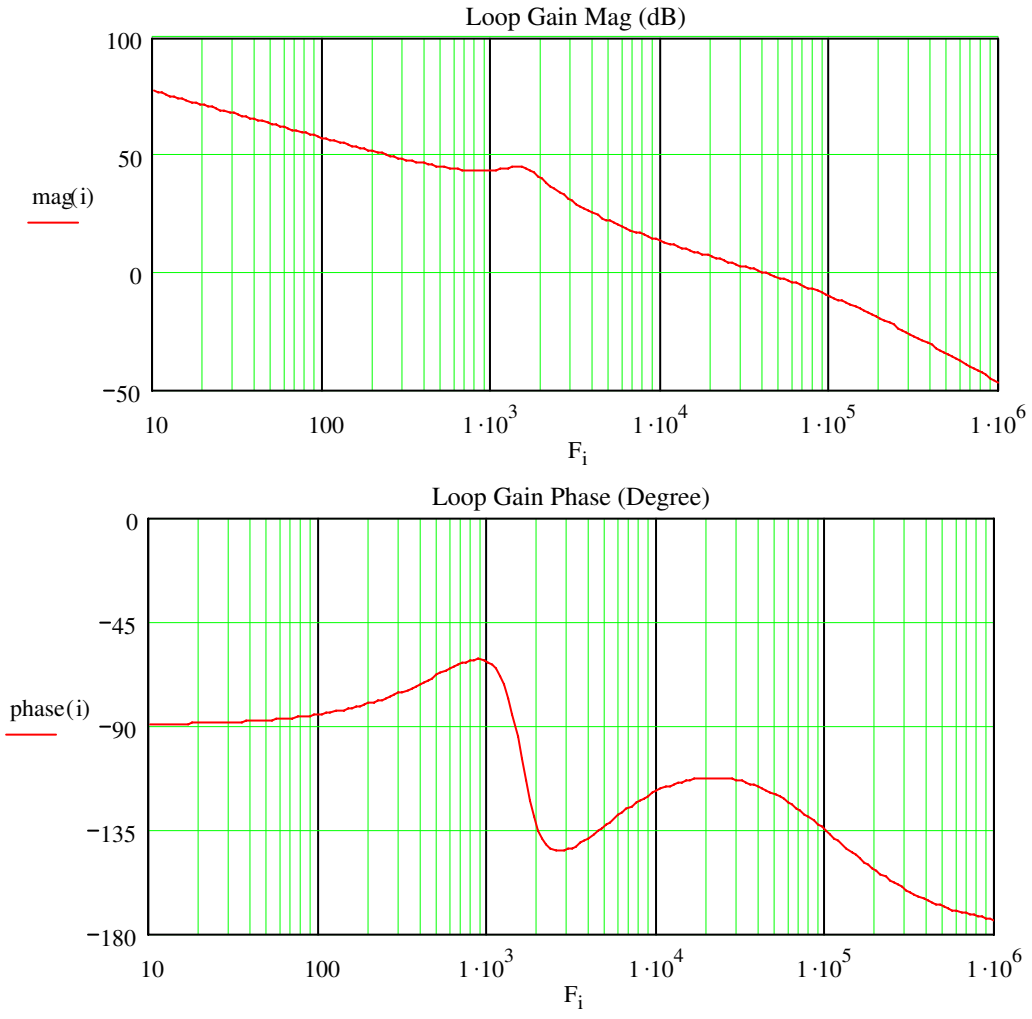
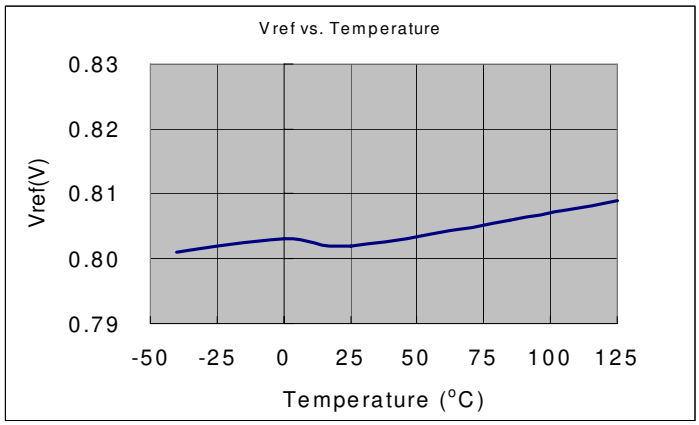
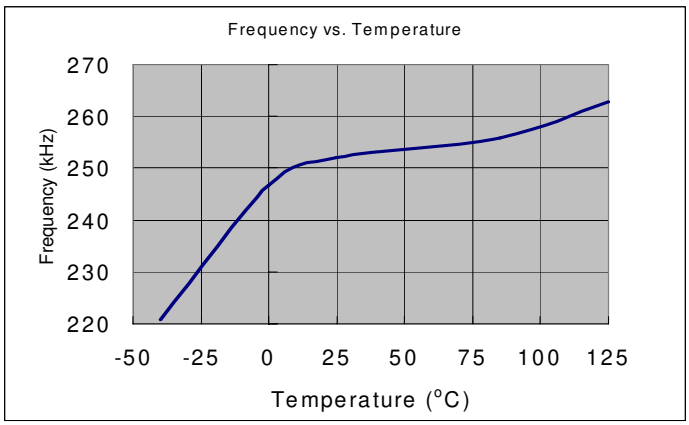
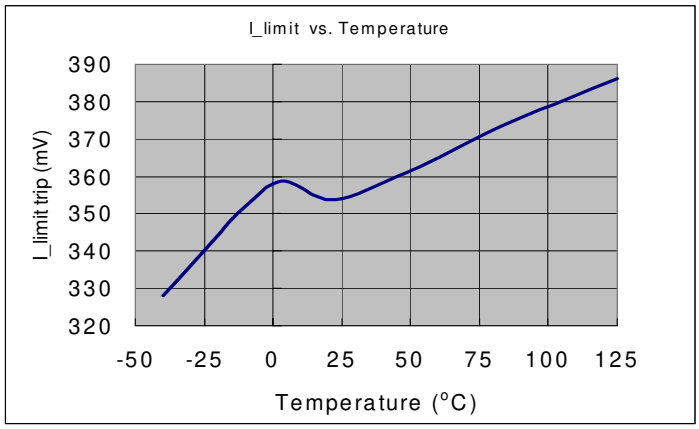


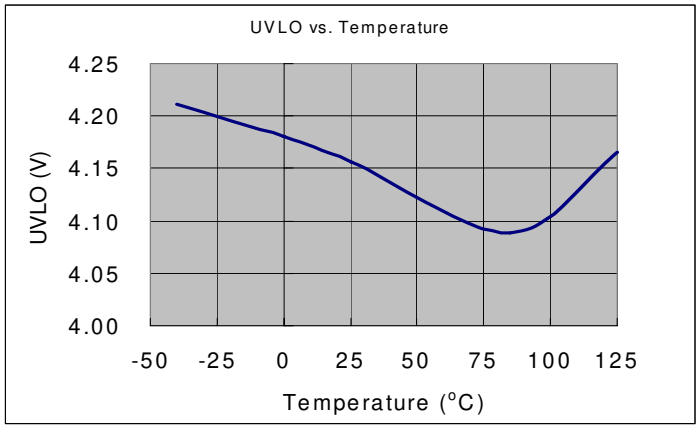
Fig. 5. Bode plot of the loop

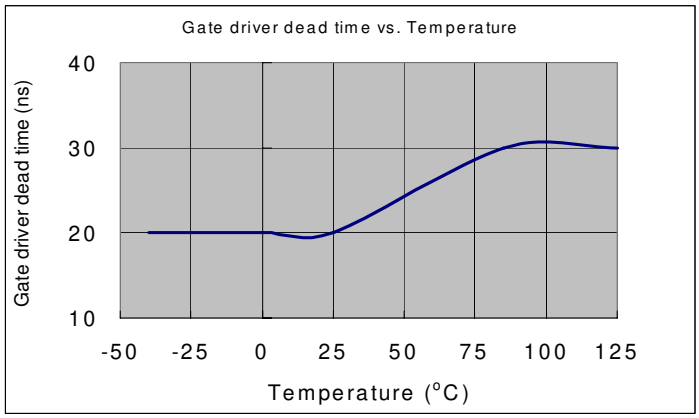
Typical Performance Characteristics

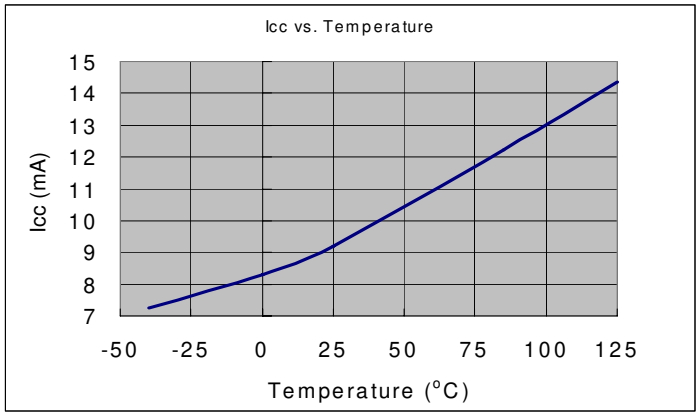




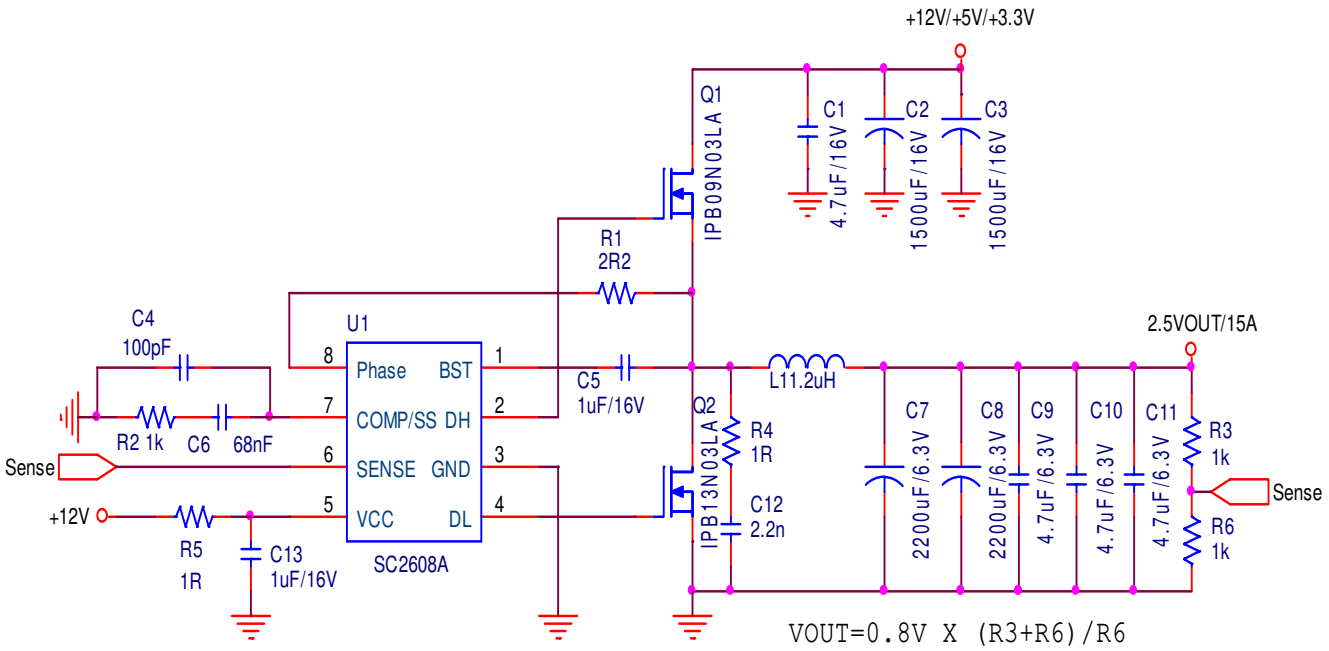








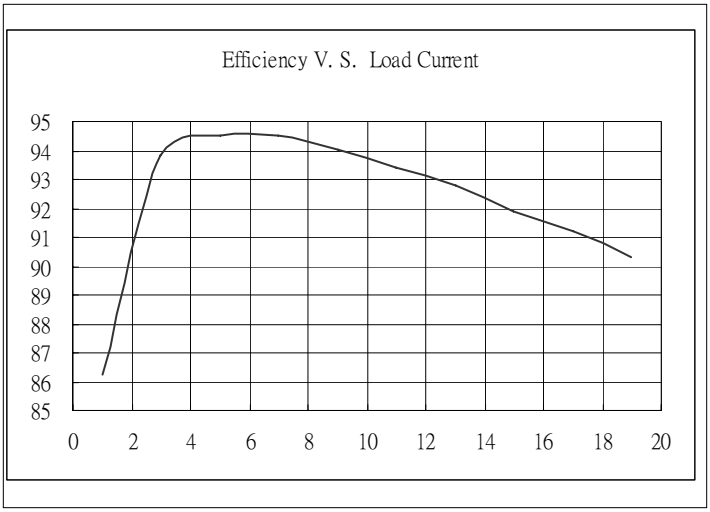
Typical Application Schematic



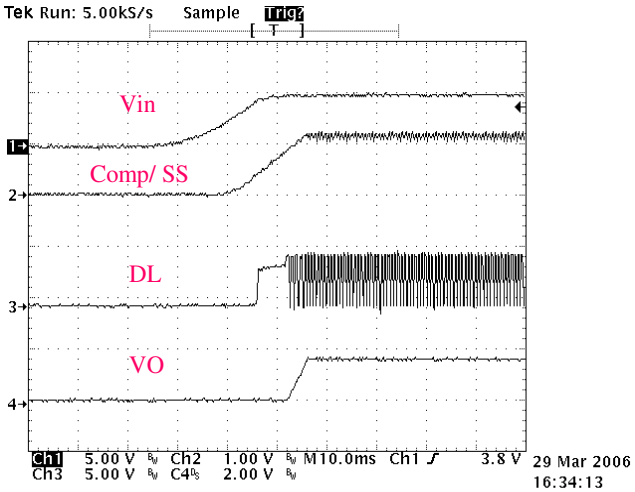
Bill of Materials

Item	Quantity	Reference	Part	Vender
1	1	C1	4.7uF/16V	Any
2	2	C2,C3	1500uF/16V	Panasonic FJ
3	1	C4	100pF/50V	Any
4	2	C5,C13	1uF/16V	Any
5	1	C6	68nF/25V	Any
6	2	C7,C8	2200uF/6.3V	Panasonic FJ
7	3	C9,C10,C11	4.7uF/6.3V	Any
8	1	C12	2.2nF	Any
9	1	L1	1.2uH	Any
10	1	Q1	IPD09N03LA	Infineon
11	1	Q2	IPD13N03LA	Infineon
12	1	R1	2R2	Any
13	1	R2	1K	Any
14	2	R3,R6	1K, 1%	Any
15	2	R4,R5	1RO	Any
16	1	U1	SC2608A	SEMTECH

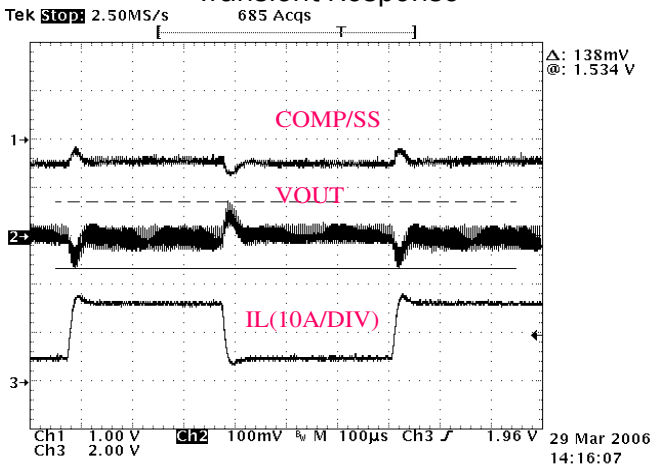
Typical Performance Characteristics



Start up

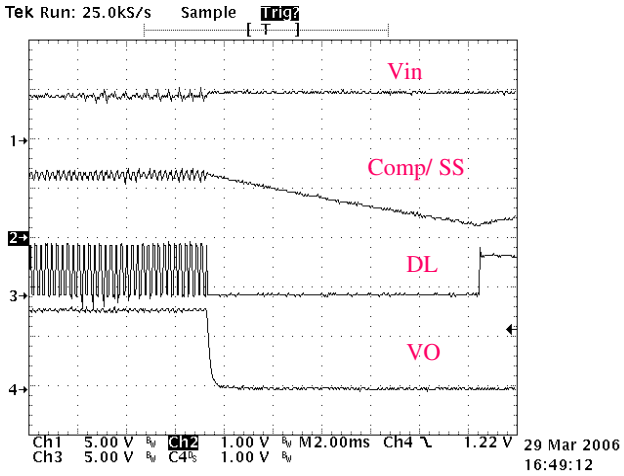


Transient Response

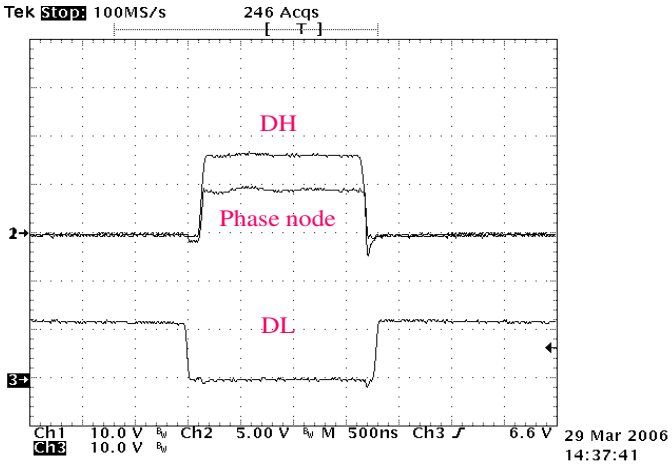


5 -18 A step load

Over Current Protection (21A DC tripped)

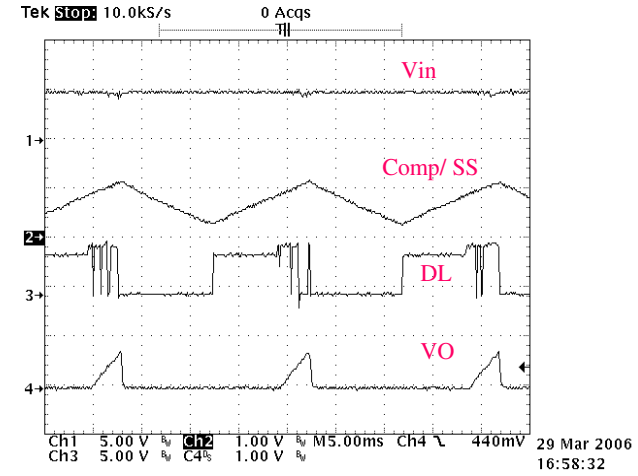


Gate waveforms

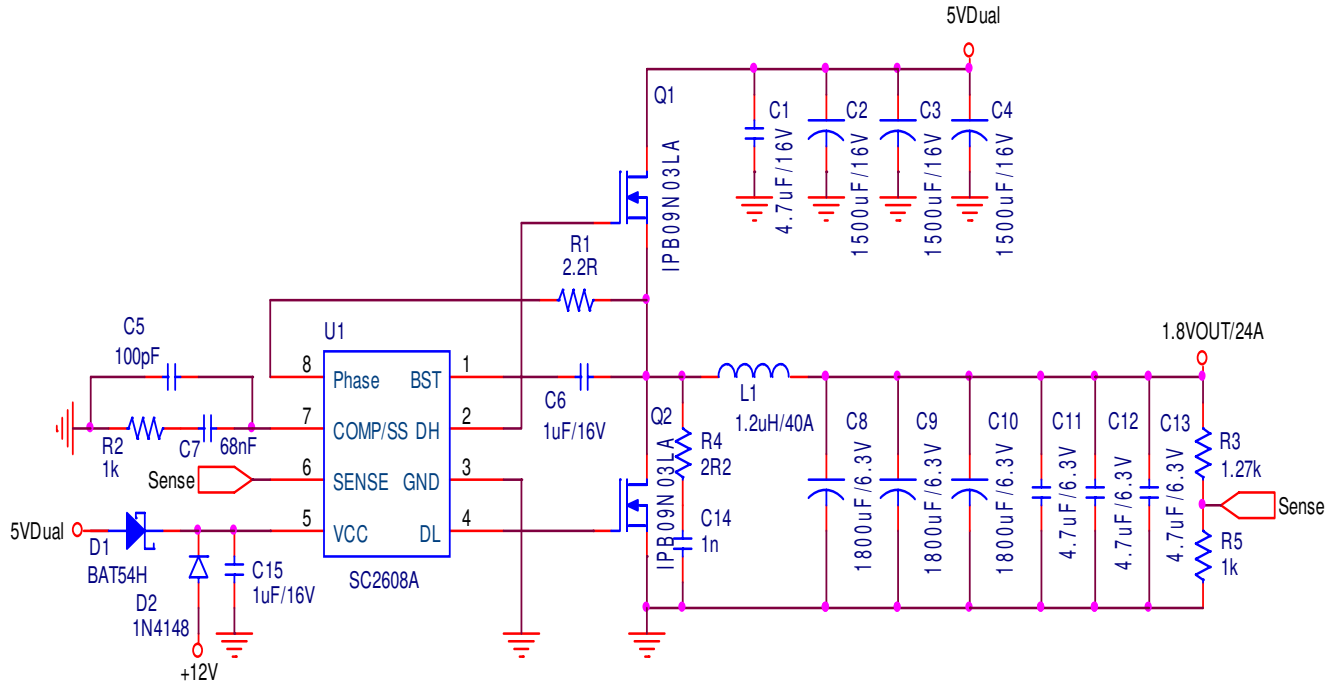


15 A sustain loading

OCP HICCUP



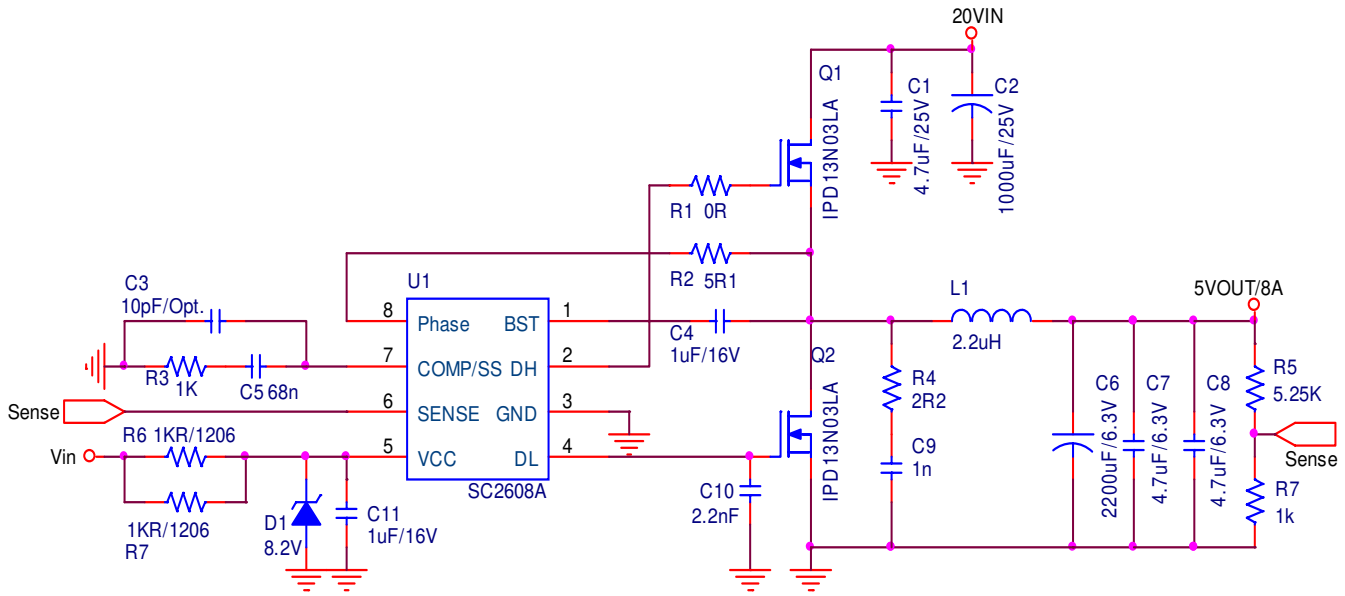
Typical DDR VDDQ Application Schematic



Bill of Materials

Item	Quantity	Reference	Part	Vender
1	4	C1,C11,C12,C13	4.7uF/6.3V	Any
2	3	C2,C3,C4	1500uF/6.3V	Panasonic FJ
3	1	C5	100pF/50V	Any
4	2	C6,C15	1uF/16V	Any
5	1	C7	68nF/25V	Any
6	3	C8,C9,C10	1800uF/6.3V	Panasonic FJ
7	1	C14	1nF/50V	Any
8	1	D1	BAT54H	Any
9	1	D2	1N4148	Any
10	1	L1	1.2uH/40A	Any
11	1	Q1	IPD09N03LA	Infineon
12	1	Q2	IPD09N03LA	Infineon
13	2	R1,R4	2R2	Any
14	1	R2	1K	Any
15	1	R3	1.27K, 1%	Any
16	1	R5	1K, 1%	Any
17	1	U1	SC2608A	SEMTECH

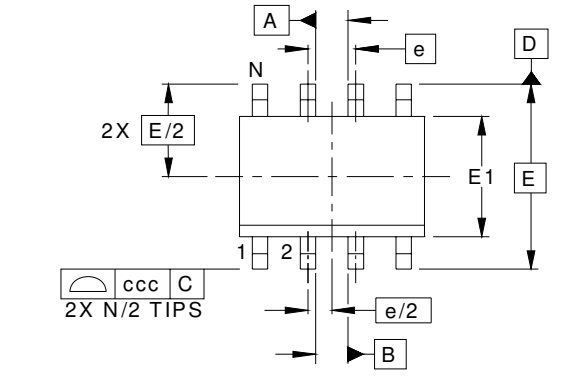
Typical High Input Voltage Application Schematic

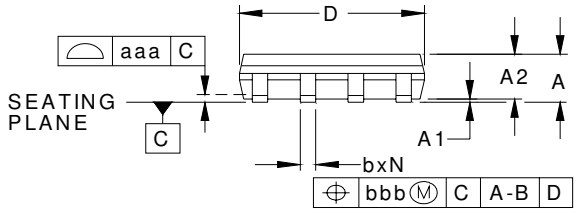


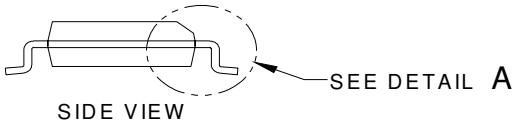
Bill of Materials

Item	Quantity	Reference	Part	Vender
1	1	C1	4.7uF/25V	Any
2	1	C2	1000uF/25V	Panasonic FJ
3	1	C3	10pF/50V , Opt.	Any
4	2	C4,C11	1uF/16V	Any
5	1	C5	68nF/16V	Any
6	1	C6	2200uF/6.3V	Panasonic FJ
7	2	C7,C8	4.7uF/6.3V	Any
8	1	C9	1nF/50V	Any
9	1	C10	2.2nF/50V	Any
10	1	D1	Zener 8.2V	Any
11	1	L1	2.2uH/15A	Any
12	1	Q1	IPD13N03LA	Infineon
13	1	Q2	IPD13N03LA	Infineon
14	1	R1	OR	Any
15	1	R2	5.1R	Any
16	2	R3,R7	1.K, 1%	Any
17	1	R4	2R2	Any
18	1	R5	5.25K, 1%	Any
19	2	R6,R7	1KR, 1206	Any
20	1	U1	SC2608A	SEMTECH

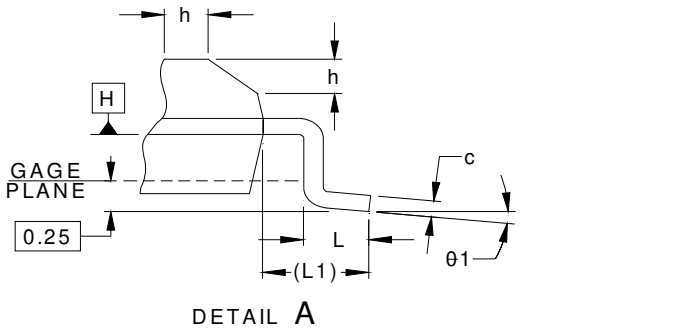
Outline Drawing - SO-8







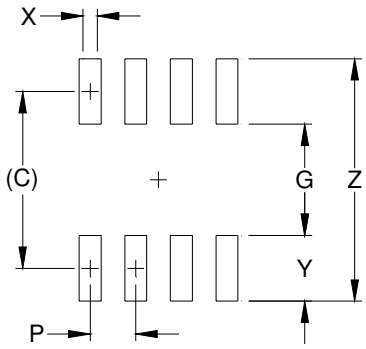
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.053	-	.069	1.35	-	1.75
A1	.004	-	.010	0.10	-	0.25
A2	.049	-	.065	1.25	-	1.65
b	.012	-	.020	0.31	-	0.51
c	.007	-	.010	0.17	-	0.25
D	.189	.193	.197	4.80	4.90	5.00
E1	.150	.154	.157	3.80	3.90	4.00
E	.236 BSC			6.00 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.020	0.25	-	0.50
L	.016	.028	.041	0.40	0.72	1.04
L1	(.041)			(1.04)		
N	8			8		
θ1	0	-	8	0	-	8
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.008			0.20		



NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

Land Pattern - SO-8



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.205)	(5.20)
G	.118	3.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.291	7.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 300A.

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