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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

June 2013

FDZ2040L
Integrated Load Switch

Features

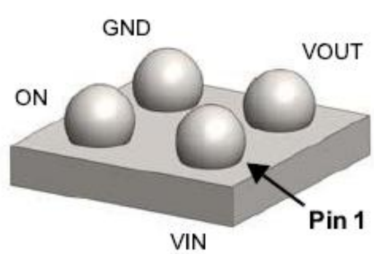
- Optimized for Low-Voltage Core ICs in Portable Systems
- Very Small Package Dimension: WL-CSP 0.8 X 0.8 X 0.5 mm^3
- Current = 1.2 A, V_{IN} max. = 4 V
- Current = 2 A, V_{IN} max. = 4 V (Pulsed)
- $R_{DS(ON)}$ = 80 mΩ at V_{ON} = 0 V, V_{IN} = 4 V
- $R_{DS(ON)}$ = 85 mΩ at V_{ON} = 0 V, V_{IN} = 3.6 V
- $R_{DS(ON)}$ = 90 mΩ at V_{ON} = 0 V, V_{IN} = 3 V
- RoHS Compliant

General Description

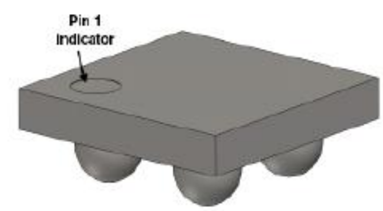
This device is particularly suited for compact power management in portable applications where 1.6 V to 4 V input and 1.2 A output current capability are needed. This load switch integrates a level-shifting function that drives a P-channel power MOSFET in the very small 0.8 X 0.8 X 0.5 mm^3 WL-CSP package.

Applications

- Load Switch
- Power Management in Portable Applications



BOTTOM



TOP

Ordering Information

Part Number	Device Marking	Ball Pitch	Operating Temperature Range	Switch	Package	Packing Method
FDZ2040L	ZL	0.4 mm	-25 to 75°C	80 mΩ, P-Channel MOSFET	0.8x0.8x0.5 mm^3 WL-CSP	Tape and Reel

Application Diagram and Block Diagram

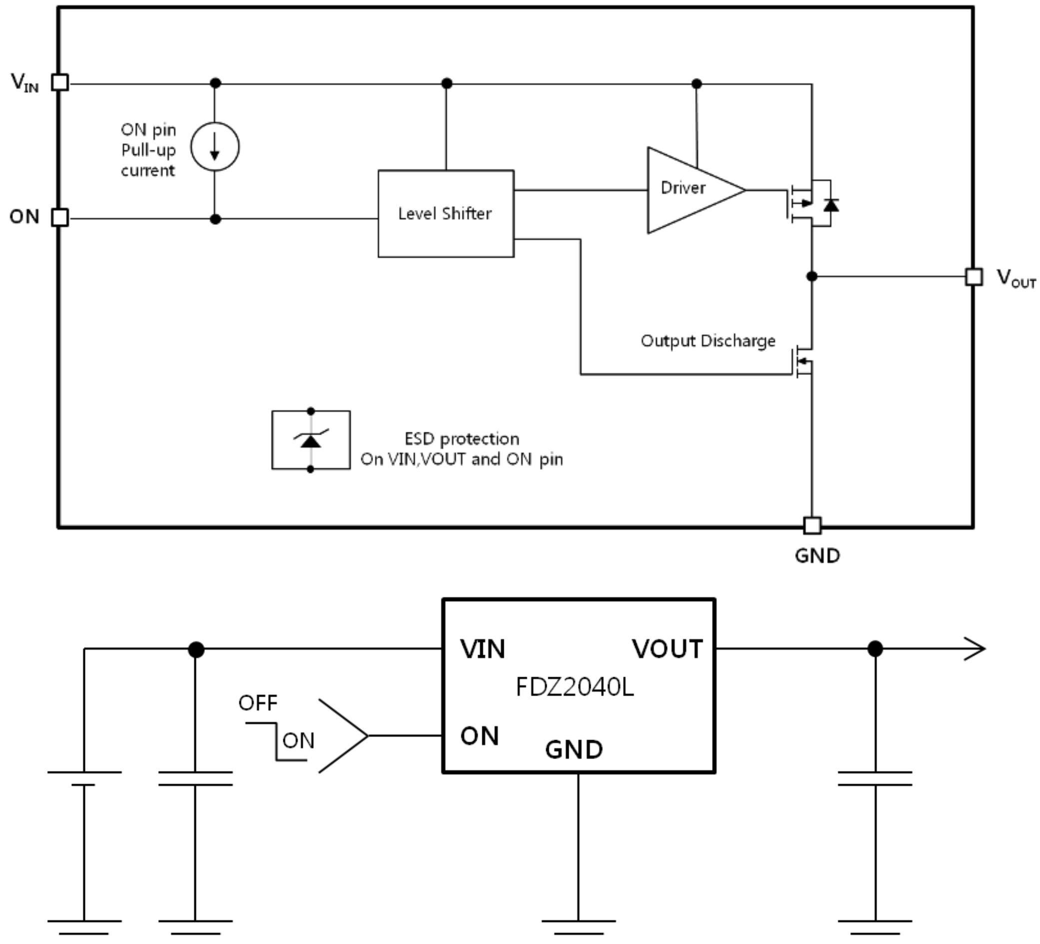


Figure 1. Block Diagram and Typical Application Pin Configuration

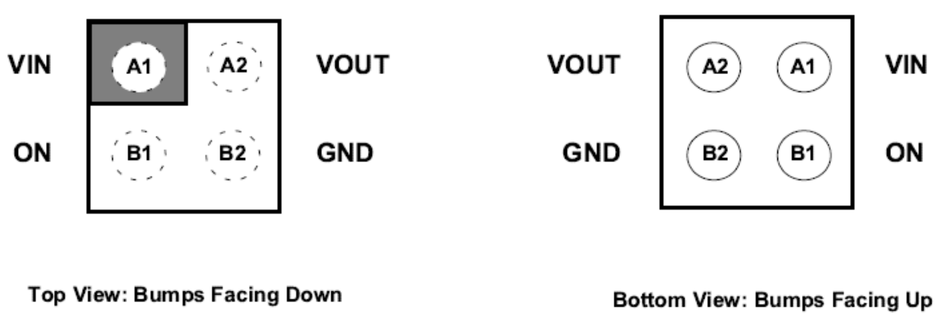


Figure 2. Pin Assignment

Pin Definitions

Pin #	Name	Description
A1	V_{IN}	Supply Input: Input to the load switch
A2	V_{OUT}	Switch Output: Output of the load switch
B1	ON	ON/OFF Control Input, Active LOW
B2	GND	Ground

Absolute Maximum Ratings

Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, ON to GND		-0.3	4.2	V
I_{OUT} – Load Current (Continuous)[(1a)]			1.2	A
I_{OUT} – Load Current (Pulsed)[(2)]			2	A
Power Dissipation @ T_A = 25°C[(1a)]			0.9	W
Operating Temperature Range		-40	105	°C
Storage Temperature		-65	150	°C
Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8		kV
	Charged Device Model, JESD22-C101	2		

Thermal Characteristics

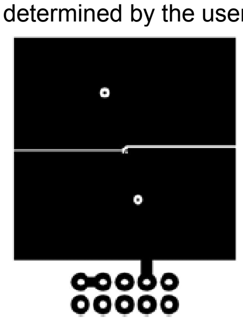
Parameter	Min.	Max.	Unit
Thermal Resistance, Junction to Ambient[(1a)]		117	°C/W

Recommended Operating Conditions

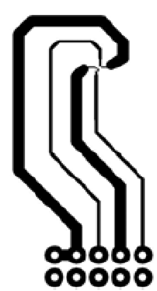
Parameter	Min.	Max.	Unit
V_{IN}	1.6	4.0	V
Ambient Operating Temperature, T_A	-25	75	°C

Notes:

1. $R_{\Theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\Theta JC}$ is guaranteed by design while $R_{\Theta JA}$ is determined by the user's board design.



a. 117 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 277 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 µs, Duty Cycle < 2.0%.

Electrical Characteristics

T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Operation Voltage		1.6		4.0	V
V_{IL}	ON Input Logic LOW Voltage	V_{IN} = 1.6 V, Ramp-Down V_{ON} from 1 V to 0 V, V_{OUT} LOW to HIGH, T_J = -25 to 75°C			0.35	V
		V_{IN} = 4 V, Ramp-Down V_{ON} from 1 V to 0 V, V_{OUT} LOW to HIGH, T_J = -25 to 75°C			0.35	V
V_{IH}	ON Input Logic HIGH Voltage	V_{IN} = 1.6 V, Ramp-Up V_{ON} from 0 V to 1 V, V_{OUT} HIGH to LOW, T_J = -25 to 75°C	1.35			V
		V_{IN} = 4 V, Ramp-Up V_{ON} from 0 V to 1 V, V_{OUT} HIGH to LOW, T_J = -25 to 75°C	1.35			V
I_Q	Quiescent Current	V_{IN} = 3 V, V_{ON} = 0.35 V, I_{OUT} = 0 A, T_J = -25 to 75°C		1.55	2.50	µA
I_{Q_off}	Off Supply Current	V_{IN} = 3 V, V_{ON} = 1.3 V, I_{OUT} = 0 A, T_J = -25 to 75°C		2.4	6.5	µA
I_{SD_off}	Off Switch Current	V_{IN} = 3 V, V_{ON} = 1.3 V, V_{OUT} = 0 V, T_J = -25 to 75°C		0.1	3.5	µA
I_{Q_off} (VON float)	Off Supply Current with ON Pin Floating	V_{IN} = 3 V, V_{ON} = Floating, I_{OUT} = 0 A		1.6	2.3	µA
		V_{IN} = 3 V, V_{ON} = Floating, I_{OUT} = 0 A, T_J = -25 to 75°C		1.6	4.0	µA
$R_{PULL-DOWN}$	Output Pull-Down Resistance	V_{IN}=3 V, I_{OUT}=10 mA		22		Ω
$R_{DS(ON)}$	On Resistance	V_{IN} = 1.6 V, V_{ON} = 0 V, I_{OUT} = 300m A		68	120	mΩ
		V_{IN} = 3 V, V_{ON} = 0 V, I_{OUT} = 300m A		50	90	
		V_{IN} = 3.6 V, V_{ON} = 0 V, I_{OUT} = 300 mA		48	85	
		V_{IN} = 4 V, V_{ON} = 0 V, I_{OUT} = 300 mA, T_J = -25 to 75°C		47	80	
$C_{V-ON(INP)}$	ON Input Capacitance	T_J = -25 to 75°C			5	pF
$I_{ON(PULL-UP)}$	ON Pull-Up Current	V_{IN} = 3 V, V_{ON} = 0 V, T_J = -25 to 75°C	0.30	0.76	1.20	µA

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{on}	Turn-On Time (V_{ON} 50% to V_{OUT} 90%)	V_{IN}=3 V, V_{ON} = 0 V as Logic LOW and 1.3 V as Logic HIGH, C_{OUT} = 1 nF, R_L = 30 Ω, T_J = -25 to 75°C		45	150	ns
t_{don}	Turn-On Delay (V_{ON} 50% to V_{OUT} 10%)			35	100	ns
t_{rise}	Turn-On Rise Time (V_{OUT} 10% to 90%)			10	50	ns
t_{off}	Turn-Off Time (V_{ON} 50% to V_{OUT} 10%)			60	150	ns
t_{doff}	Turn-Off Delay (V_{ON} 50% to V_{OUT} 90%)			25	100	ns
t_{fall}	Turn-Off Fall Time (V_{OUT} 90% to 10%)			35	65	ns
$t_{don} - t_{doff}$	Turn-On Turn-Off Delay Delta				50	ns

Typical Performance Characteristics

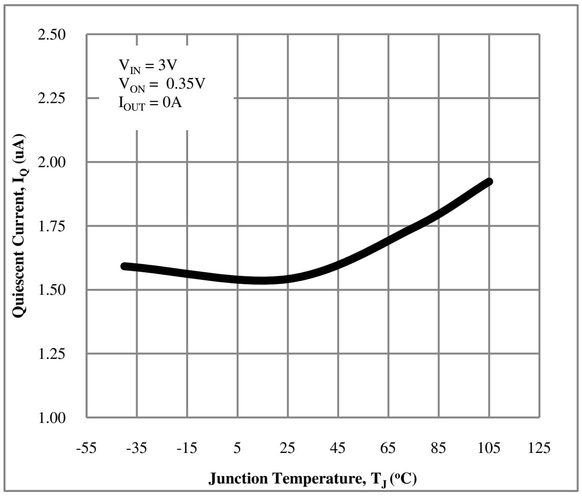


Figure 3. Quiescent Current vs. Temperature

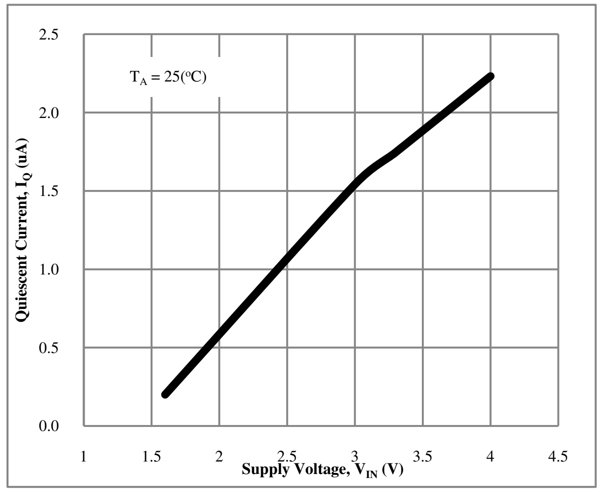


Figure 4. Quiescent Current vs. Supply Voltage

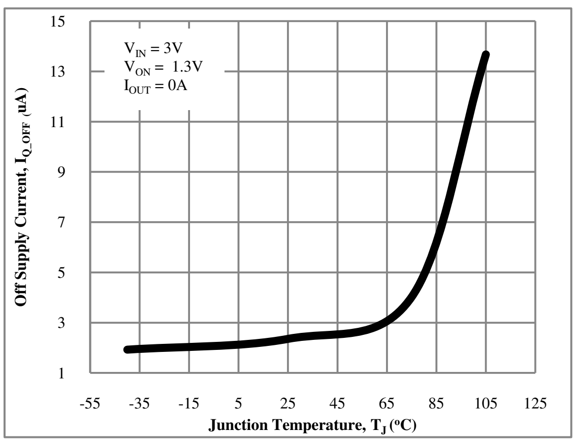


Figure 5. Off Supply Current vs. Temperature

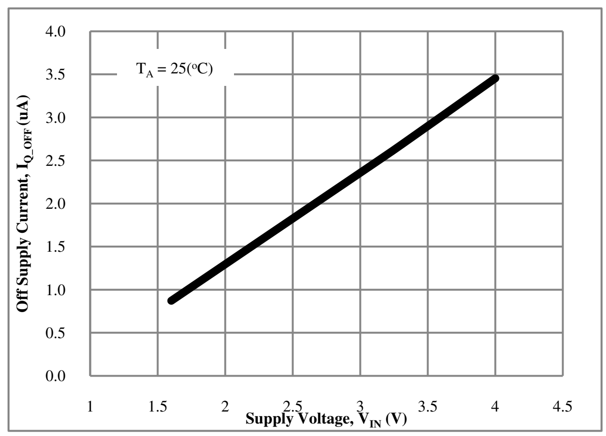


Figure 6. Off Supply Current vs. Supply Voltage

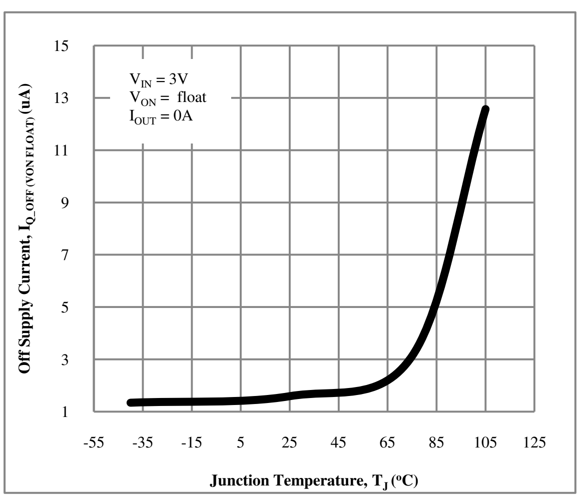


Figure 7. Off Supply Current (V_{ON} Float) vs. Temperature

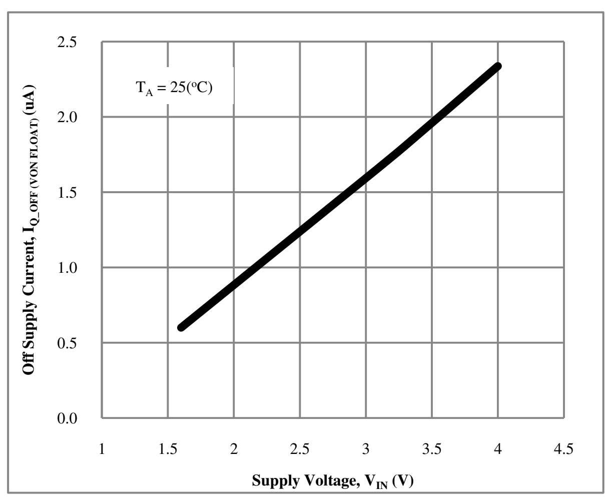


Figure 8. Off Supply Current (V_{ON} Float) vs. Supply Voltage

Typical Performance Characteristics (Continued)

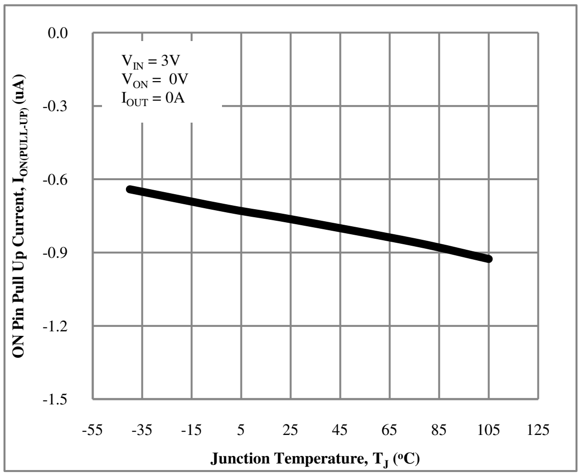


Figure 9. ON Pin Pull-Up Current vs. Temperature

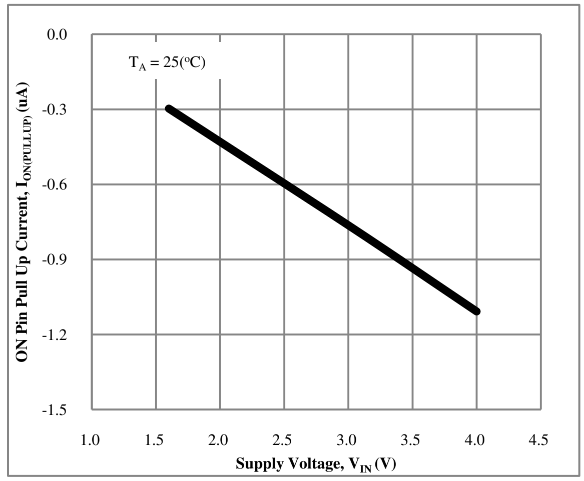


Figure 10. ON Pin Pull-Up Current vs. Supply Voltage

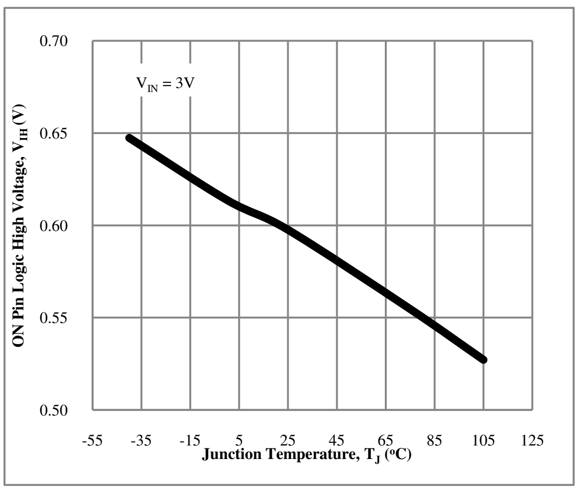


Figure 11. ON Pin Logic HIGH Voltage vs. Temperature

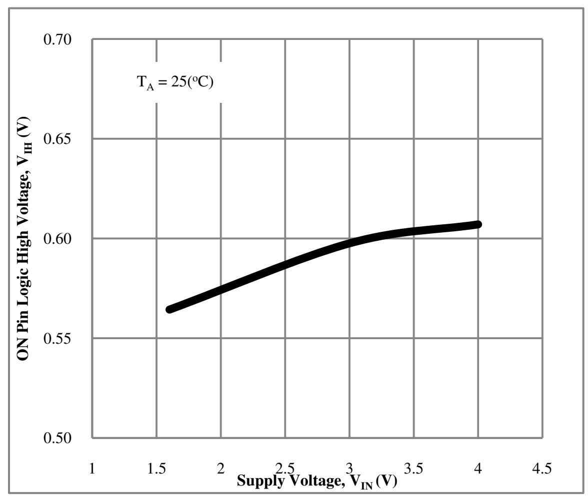


Figure 12. ON Pin Logic HIGH Voltage vs. Supply Voltage

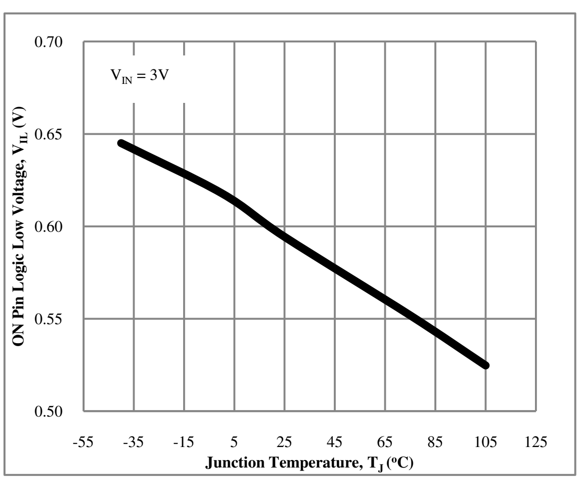


Figure 13. ON Pin Logic LOW Voltage vs. Temperature

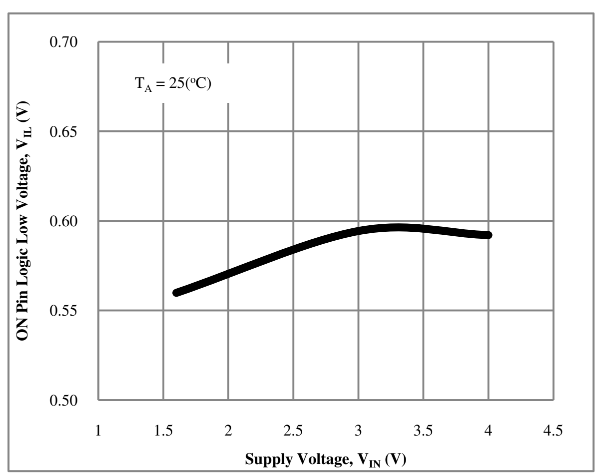


Figure 14. ON Pin Logic LOW Voltage vs. Supply Voltage

Typical Performance Characteristics (Continued)

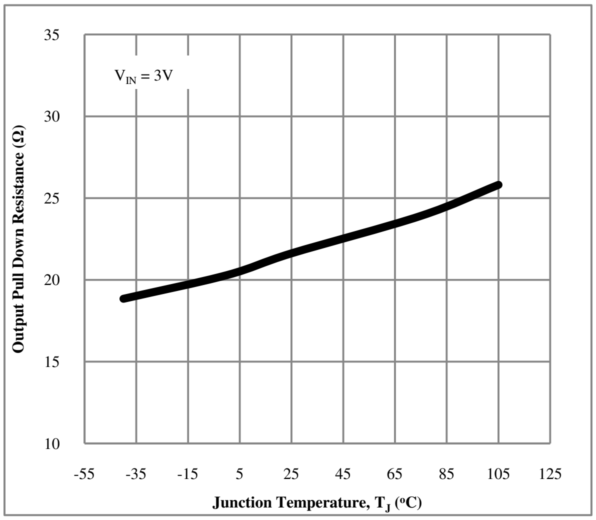


Figure 15. Output Pull-Down Resistance vs. Temperature

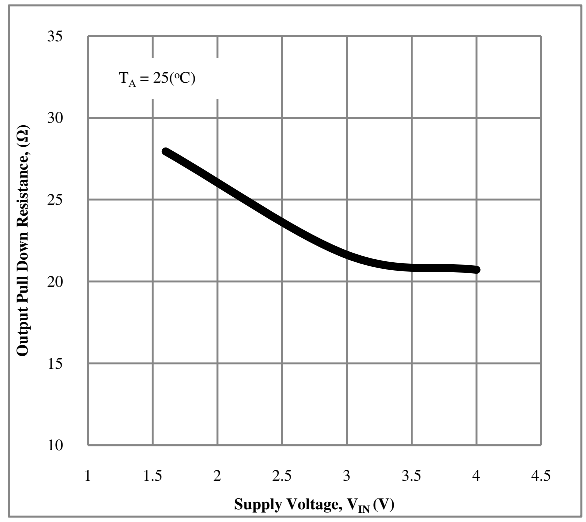


Figure 16. Output Pull-Down Resistance vs. Supply Voltage

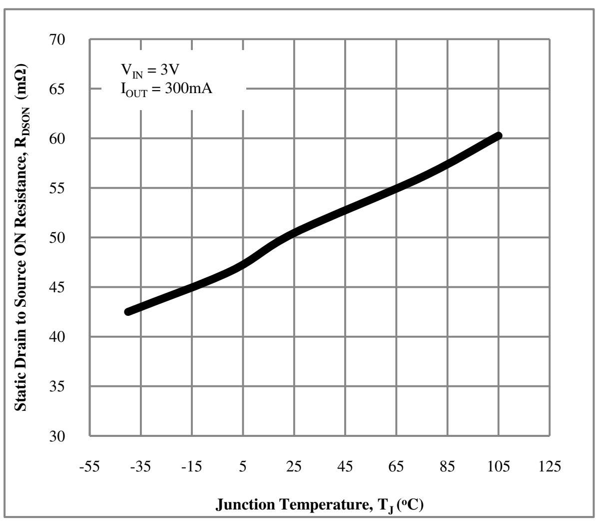


Figure 17. Static Drain-to-Source ON Resistance vs. Temperature

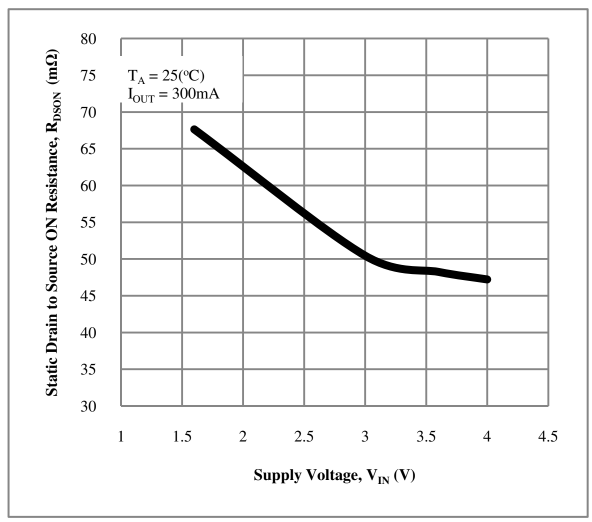
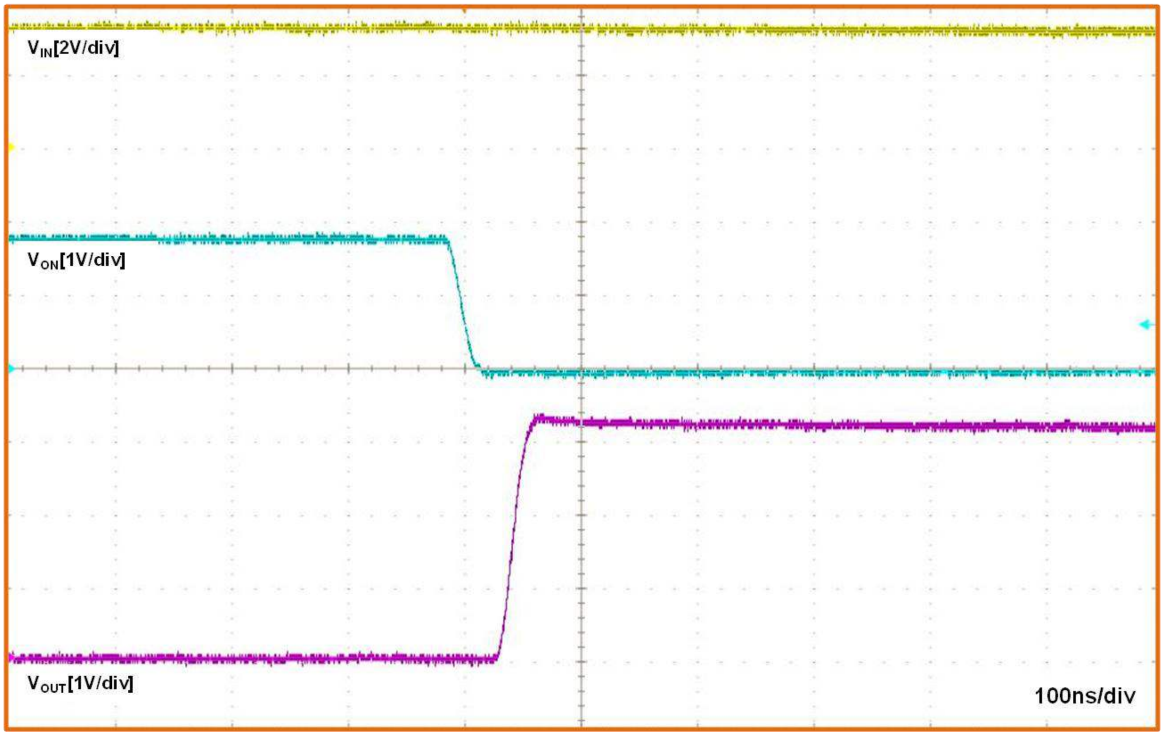


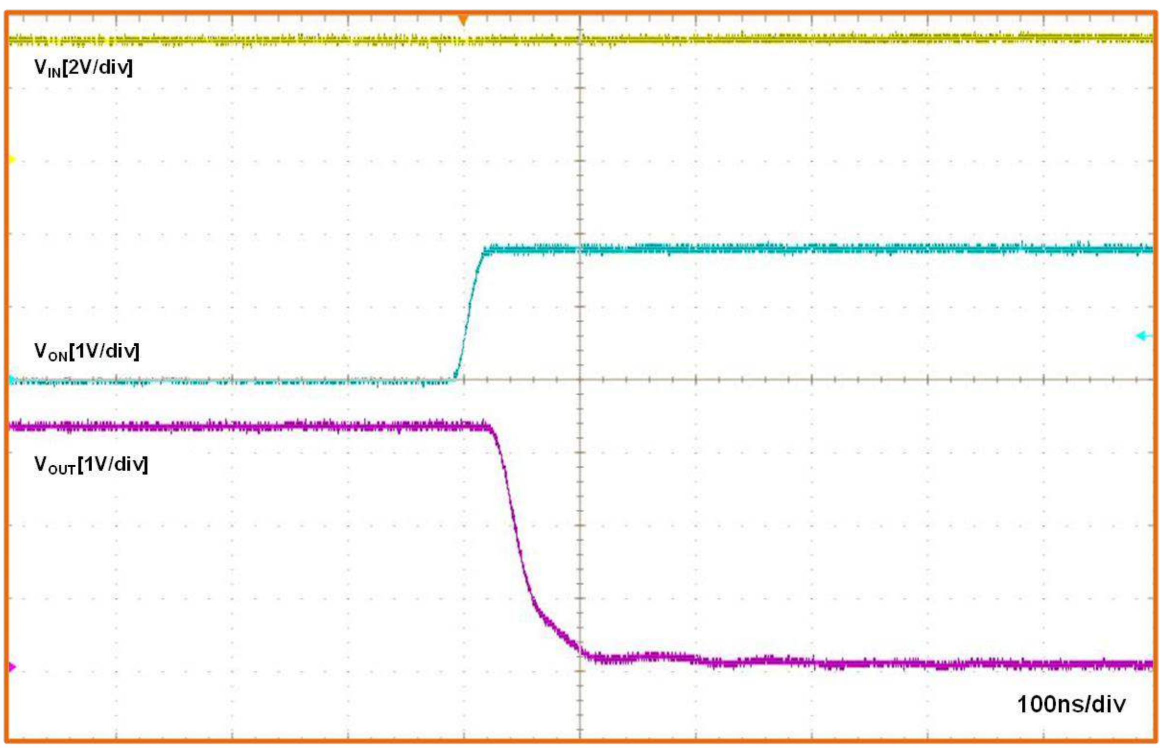
Figure 18. Static Drain-to-Source ON Resistance vs. Supply Voltage

Typical Performance Characteristics (Continued)



V_{IN} = 3.3 V, V_{ON} = 0 V, C_{IN} = 1 µF, C_{OUT} = 1 nF, R_L = 30 Ω

Figure 19. t_{ON} Response



V_{IN} = 3.3 V, V_{ON} = 0 V, C_{IN} = 1 µF, C_{OUT} = 1 nF, R_L = 30 Ω

Figure 20. t_{OFF} Response

Operation Description

The FDZ2040L is a low-$R_{DS(ON)}$ P-channel load switch packaged in space-saving 0.8 x 0.8 WL-CSP.

The core of the device is an 80mΩ P-channel MOSFET and capable of functioning over a wide input operating range of 1.6 V-4 V.

Applications Information

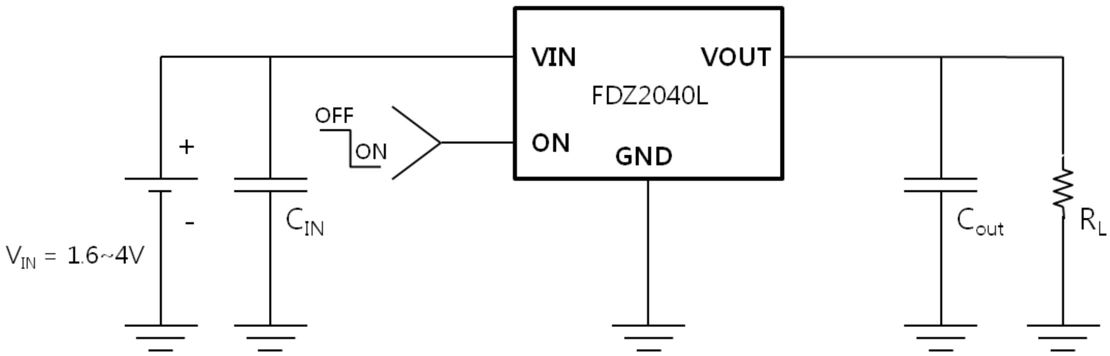


Figure 21. Typical Application

Input Capacitor

To reduce device inrush current effect, a 0.1 µF ceramic capacitor, C_{IN} is recommended close to the V_{IN} pin. A higher value of C_{IN} can be used to further reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

Output Capacitor

FDZ2040L switch works without an output capacitor. If parasitic board inductance forces V_{OUT} below GND when switching off, a 1 nF capacitor, C_{OUT}, should be placed between VOUT and GND.

Note:

3. The intrinsic diode for P-channel load switch would conduct if V_{OUT} is greater than V_{IN}, by a diode drop.

Evaluation Board Layout

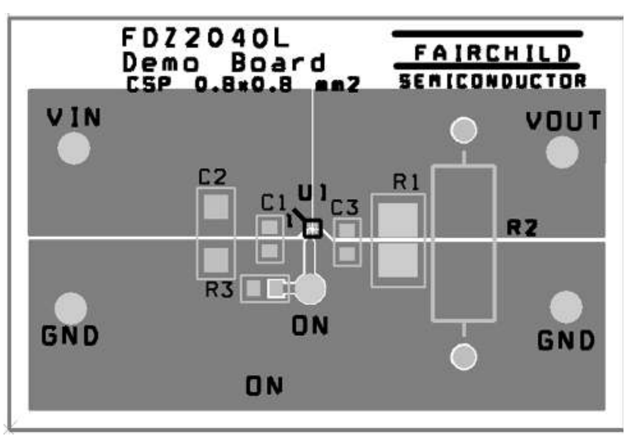


Figure 22. Top View

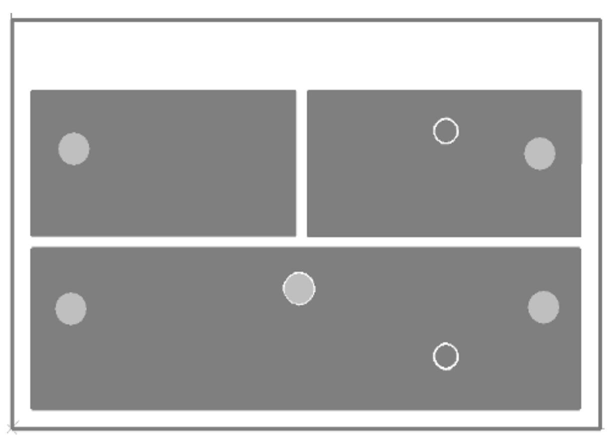
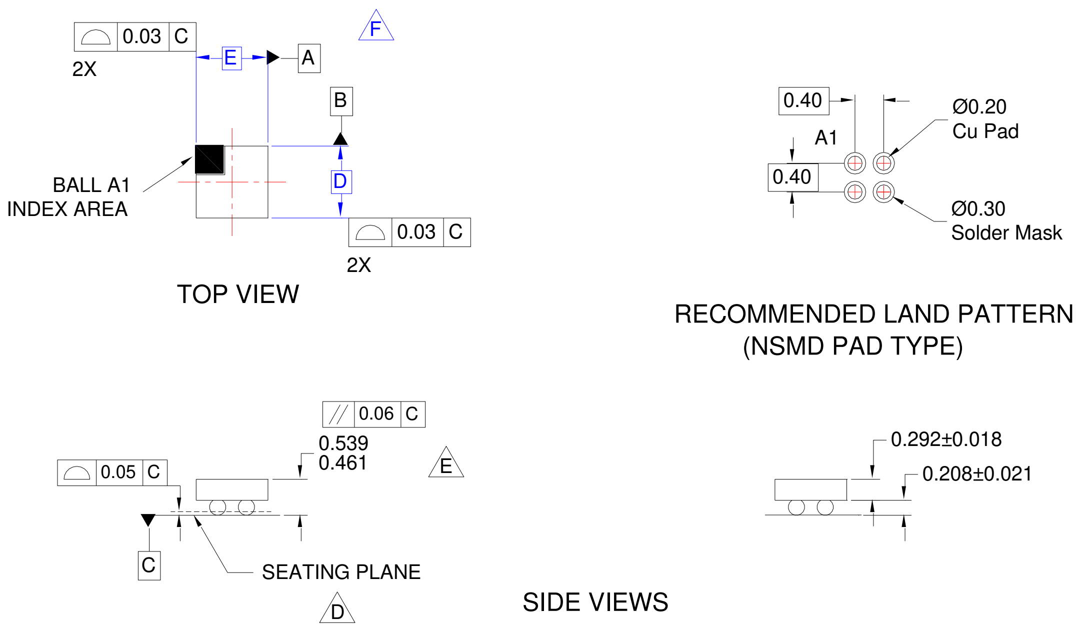
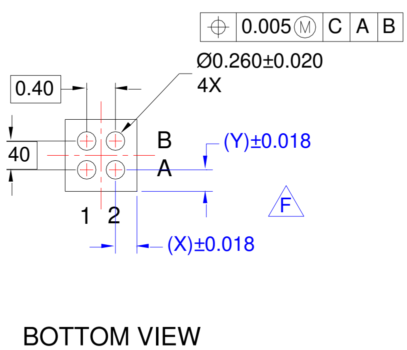


Figure 23. Bottom View

Physical Dimensions





NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 500 MICRONS ±39 MICRONS (461-539 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC004AFrev1.

Figure 24. 4 Ball, WLCSP, 2 X 2 Array, 0.4 mm Pitch, 250 µm Ball

Product-Specific Dimensions

Product	D	E	X	Y
FDZ2040L	0.8 ± 0.03 mm	0.8 ± 0.03 mm	0.21 mm	0.21 mm

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I64

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