10-BIT 240-MSPS VIDEO DAC WITH TRI-LEVEL SYNC AND VIDEO (ITU-R.BT601)-COMPLIANT FULL-SCALE RANGE

Check for Samples: THS8135

FEATURES

- **Triple 10-Bit D/A Converters**
- **240-MSPS Operation**
- **YPbPr/RGB Configurable Blanking Levels, Correctly Positioned for Either Full (0-1023) or Video (ITU-R.BT601) Compliant Input Code Ranges**
- **Generic Triple DAC Mode for Non-Video Applications**
- **Direct Drive of Double-Terminated 75-Ω Load Into Standard Video Levels**
- **3x10 Bit 4:4:4, 2x10 Bit 4:2:2 or 1x10 Bit 4:2:2 (ITU-R.BT656) Multiplexed YCbCr/GBR Input Data Formats**
- **Bi-Level (EIA) or Tri-Level (SMPTE) Sync Generation**
- **Integrated Sync-On-Green/Luminance or Sync-On-All Composite Sync Insertion**
- **Internal Voltage Reference**
- **Low-Power Operation From 3.3-V Analog and 1.8-V Digital Suply Levels**

APPLICATIONS

- **High-Definition Television (HDTV) Set-Top Boxes/Receivers/Displays**
- **High-Resolution Image Processing**

DESCRIPTION

The THS8135 is a general-purpose triple high-speed D/A converter optimized for use in video/graphics applications. The device operates from 3.3-V analog and 1.8-V digital supplies. The THS8135 performance is assured at a sampling rate up to 240 MSPS. The THS8135 consists of three 10-bit D/A converters and additional circuitry for bi-level/tri-level sync and blanking level generation. By providing a dc offset for the lowest video amplitude output in video DAC mode, the device can insert a (negative) bi-level or (negative/positive) tri-level sync on either only the green/luminance (sync-on-green/sync-on-Y) channel or on all channels for video applications. A generic DAC mode avoids this dc offset, making this device suitable for non-video applications as well.

The THS8135 is a footprint-compatible functional upgrade to the THS8133. In addition, the THS8135 allows a higher update rate for oversampled video digitizing for all PC graphics formats up to UXGA (1600x1200) resolution at 85 Hz and all practical digital TV formats including HDTV. The support for oversampling significantly reduces the complexity of the analog reconstruction filter required behind the DAC.

Standard video levels can be generated for the full 10-bit input code range. Alternatively, the same levels can be reached from a reduced input code range compliant to the video sampling standard ITU-R.BT-601. In that case, the full-scale range of the DAC is dependent on the RGB or YCbCr color space configuration of the device. When configured for RGB operation, full video output swing is reached for input codes 64-940 on all channels. When configured for YCbCr operation, code range 64-940 on Y and code range 64-960 on Cb and Cr channels generate full output swing using internal amplitude scaling on these color components. The device provides headroom to accommodate under-/over-shoot outside the ITU-R.BT601 range to allow the generation of ITU-R.BT601 illegal colors or super-black / super-white levels.

A digital control input for insertion of a reference (blanking) level on the analog outputs is included. The amplitude of the blanking level is configurable for either RGB or YPbPr component outputs and for full or reduced input code ranges. The inserted sync output amplitude(s) always has the required 7:3 ratio to the full-scale video amplitude.

The current-steering DACs can be directly terminated in resistive loads to produce voltage outputs. The device provides a flexible configuration of maximum output current drive. The devices output drivers have been specifically designed to produce standard video output levels when directly connected to a single-ended double-terminated 75-Ω coaxial cable.

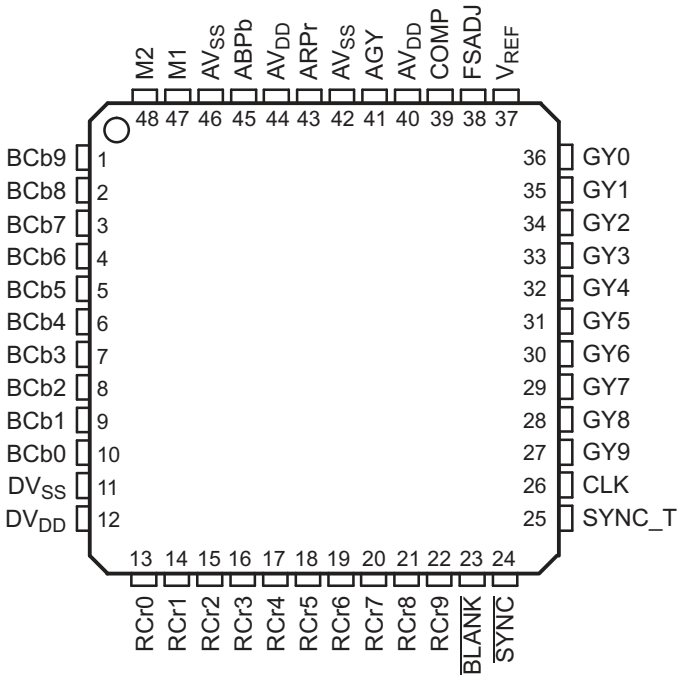
The input data format can be either 3x10 bit 4:4:4, 2x10 bit 4:2:2, or 1x10 bit 4:2:2. This enables a direct interface to a wide range of video DSP/ASICs including parts generating ITU-R.BT656 formatted output data. However, the THS8135 needs specific input synchronization signals to properly insert a composite sync onto its outputs as it does not extract embedded SAV/EAV synchronization codes from the ITU-R.BT656 input. Along with other extra functionality, this feature is available on a derivative device (THS8200).

Table 1. Ordering Information(1)

T_A	PACKAGED DEVICES(2) TQFP-48 PowerPAD™
0°C to 70°C	THS8135PHP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

PHP PACKAGE
(TOP VIEW)



Functional Block Diagram

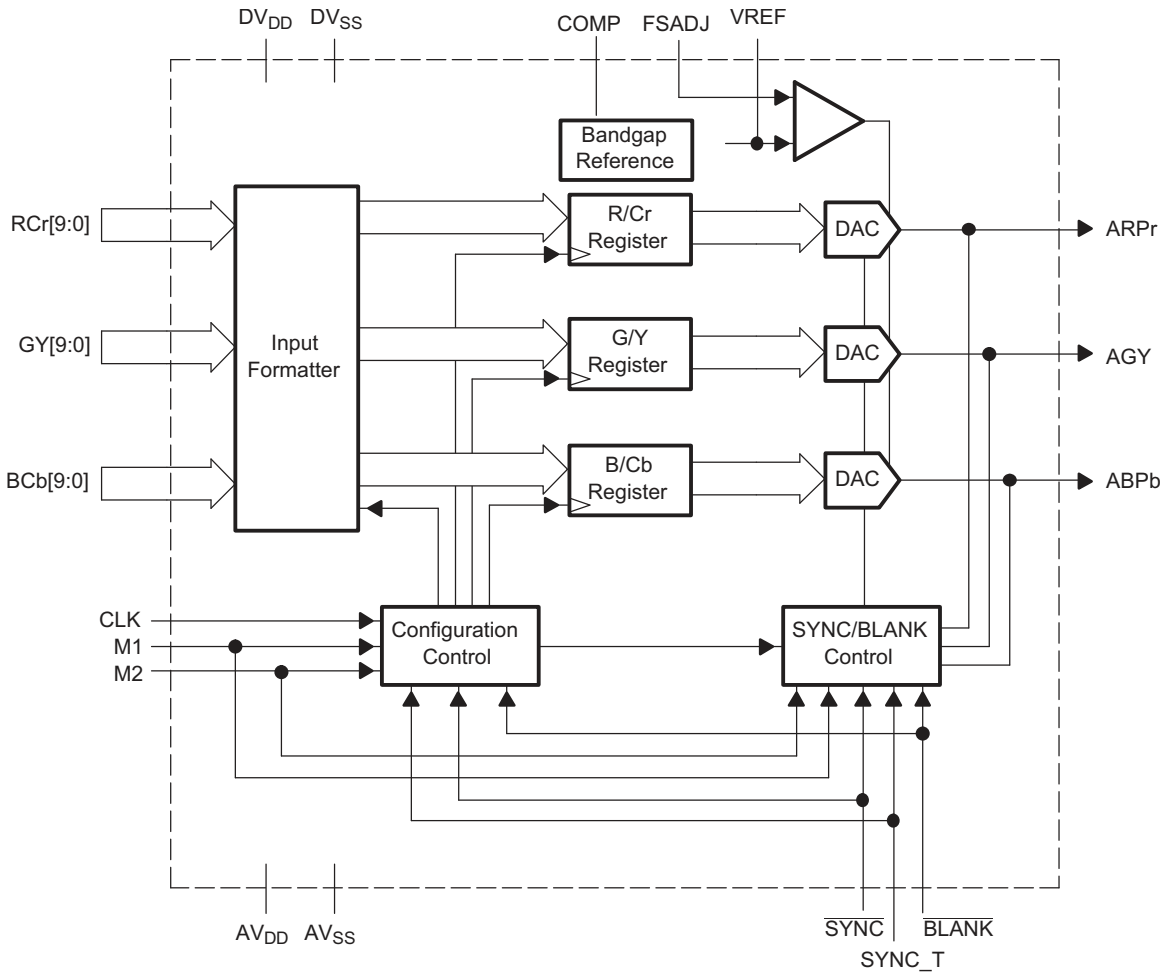


Table 2. Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
ABPb	45	O	Analog blue or Pb current output, capable of directly driving a double terminated 75-Ω coaxial cable
AGY	41	O	Analog green or Y current output, capable of directly driving a double terminated 75-Ω coaxial cable
ARPr	43	O	Analog red or Pr current output, capable of directly driving a double terminated 75-Ω coaxial cable
AV_{DD}	40, 44	I	Analog power supply (3.3 V). All AV_{DD} pins must be connected.
AV_{SS}	42, 46	I	Analog ground
BCb0-BCb9	10-1	I	Blue or Cb pixel data input. Signals with index 0 denote the least significant bits.
$\overline{BLANK}$	23	I	Blanking control input, active low. A rising edge on CLK latches $\overline{BLANK}$. When asserted, the ARPr, AGY, and ABPb outputs are driven to the blanking level, irrespective of the value on the data inputs. $\overline{SYNC}$ takes precedence over $\overline{BLANK}$, so asserting $\overline{SYNC}$ (low) while $\overline{BLANK}$ is active (low) results in sync generation. The amplitude of the DAC outputs during $\overline{BLANK}$ active are determined by the color space and input code range configurations of the device. $\overline{BLANK}$ control is available in both video and generic DAC modes.
CLK	26	I	Clock input. A rising edge on CLK latches RCr0-9, GY0-9, BCb0-9, $\overline{BLANK}$, $\overline{SYNC}$, and SYNC_T. In video DAC mode, the M1 and M2 inputs are latched by a rising edge on CLK as well but only when additional conditions are satisfied as explained in their terminal description. In generic DAC mode, M1 and M2 are continuously interpreted that is independent of additional conditions, to determine color space and input data formats. This allows easier configuration.
COMP	39	O	Compensation terminal. A 0.1-µF capacitor must be connected between COMP and AV_{DD}.
DV_{DD}	12	I	Digital power supply (1.8 V)

Table 2. Terminal Functions (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
DV_{SS}	11	I	Digital ground
FSADJ	38	I	Full-scale adjust control. The full-scale current drive on each of the output channels is determined by the value of a resistor R_{FS} connected between this terminal and AV_{SS}. Figure 5 shows the relationship between full-scale output voltage compliance and R_{FS} for the nominal DAC termination of 37.5 Ω.
GY0-GY9	36-27	I	Green or Y pixel data input. Signals with index 0 denote the least significant bits.
M1	47	I	Operation mode control 1. In video DAC mode, the second rising edge on CLK after a transition on $\overline{SYNC}$ latches M1. The interpretation is dependent on the polarity of the last $\overline{SYNC}$ transition: $\overline{SYNC}$ L → H: latched as M1_INT $\overline{SYNC}$ H → L: latched as BLNK_INT Together with M2_INT, M1_INT configures the device as shown in Table 4 for video DAC mode. BLNK_INT determines if the device operates with the full- or reduced-scale input code range. Together with the color space configuration, this sets the amplitude of the blanking level on the analog output(s) as shown in Table 7. In generic DAC mode, M1 is continuously interpreted as M1_INT, BLNK_INT control is not available and the device always assumes full-scale input code range for blank level positioning.
M2	48	I	Operation mode control 2. In video DAC mode, the second rising edge on CLK after a transition on $\overline{SYNC}$ latches M2. The interpretation is dependent on the polarity of the last $\overline{SYNC}$ transition: $\overline{SYNC}$ L → H: latched as M2_INT $\overline{SYNC}$ H → L: latched as INS3_INT Together with M1_INT, M2_INT configures the device as shown in Table 5 for video DAC mode. When INS3_INT is high, the device inserts sync on all DAC outputs; when low, sync is inserted only on the AGY output. In generic DAC mode, M2 is continuously interpreted as M2_INT, INS3_INT control is not applicable, because sync insertion is not available in generic DAC mode.
RCr0-RCr9	13-22	I	Red or Cr pixel data input. Signals with index 0 denote the least significant bits.
$\overline{SYNC}$	24	I	Sync control input, active low. A rising edge on CLK latches $\overline{SYNC}$. When asserted, only the AGY output (when INS3_INT = L, see terminal M2) for sync-on-G/Y, or ARPr, AGY, and ABPb outputs (when INS3_INT = H, see terminal M2) for sync-on-all, are driven to the sync level, irrespective of the values on the data or $\overline{BLANK}$ inputs. Therefore, $\overline{SYNC}$ should remain low for the whole duration of sync, which is in the case of a tri-level sync both the negative and positive portion. See Figure 10 for timing control. $\overline{SYNC}$ control is only available in video DAC mode.
SYNC_T	25	I	Sync tri-level control, active high. A rising edge on CLK latches SYNC_T. When asserted (high), a positive sync (higher than blanking level) is generated when $\overline{SYNC}$ is low. When disabled (low), a negative sync (lower than blanking level) is generated when $\overline{SYNC}$ is low. When generating a tri-level (negative-to-positive) sync, an L->H transition on this signal positions the start of the positive transition. Figure 10 for timing control. SYNC_T is also used to put the device in generic DAC mode: $\overline{SYNC}$ = H AND SYNC_T = H → generic DAC mode. Therefore, the user should always drive SYNC_T low outside the sync period when video DAC mode operation is intended.
V_{REF}	37	O	Voltage reference for DACs. An internal voltage reference of nominally 1.2 V is provided, which requires an external 0.1-µF ceramic capacitor between VREF and AV_{SS}.

DETAILED DESCRIPTION

The THS8135 is a fast well-matched triple DAC with current outputs optimized for video applications without sacrificing its usefulness as a general-purpose triple DAC, thanks to a generic DAC mode. For video applications, the device can embed an analog output (composite) bi-level or tri-level sync on only the green/luma channel or on all three DAC output channels. The THS8135 offers compatibility with several popular video data formats and provides standard analog output compliance levels for component video digitized according to the ITU-R.BT601 sampling standard. The DAC full-scale range is also adjustable.

Sync Generation

The $\overline{\text{SYNC}}$ and SYNC_T control inputs enable the superposition of an additional current onto the AGY channel or onto all three channels, depending on the setting of INS3_INT. Using a combination of the $\overline{\text{SYNC}}$ and SYNC_T control inputs, either bi-level negative going pulses or tri-level pulses can be generated. By driving these terminals with the correct timing inputs, the user can insert onto the analog output(s) any composite sync format consisting of horizontal sync, vertical sync, pre- and post-serration, and equalization pulses. Assertion of $\overline{\text{SYNC}}$ (active low) identifies the sync period, while assertion of SYNC_T (active high) within this period identifies the positive excursion of a tri-level sync.

Blanking Generation

The $\overline{\text{BLANK}}$ control input fixes the output amplitude on all channels to the blanking level, irrespective of the value on the data input ports. The position of the blanking level on each channel and its relation to active video is different depending on the RGB versus YCbCr color space configuration: bottom-range blanking level for R, G, B, and Y outputs versus mid-range blanking level for Pb and Pr outputs. This also depends on the full-scale versus reduced-scale (ITU-R.BT601) input code range configuration: bottom-range blanking levels correspond to input code 0 when in full-scale, or to code 64 when in reduced-scale input code range configuration; mid-range blanking levels remain at 512 in all cases.

Generic DAC Mode vs Video DAC Mode

In video DAC mode, the device provides additional dc bias on R, G, B, and Y channels to provide headroom for negative sync insertion, as shown on Figure 1 and Figure 3.

Such bias might be undesirable in applications where no sync embedding is needed, because it causes additional power consumption and might prevent dc coupling of the DAC outputs. In such cases, only a triple DAC operation without dc bias (that is, DAC input code 0 corresponding to 0-V output) might be preferred as there is no need for sync insertion. Therefore, the THS8135 includes a generic DAC mode that does not add any dc bias. Sync insertion is not supported in generic DAC mode. Also, in this mode, only full-scale operation is available. Other features are still available in generic DAC mode: different input data formats, RGB versus YCbCr color space selection, and blanking level override option.

Because of the eliminated dc bias, the DAC output compliance for full-range video input can be higher in generic DAC mode: up to 1.286 Vpp at nominal double 75-Ω termination load. This is high enough for the D/A conversion of composite video (NTSC/PAL/SECAM), where the signal fed to the device contains the complete digital composite waveform, including sync and color-burst.

Selection between generic DAC versus video DAC mode is controlled through a combination of $\overline{\text{SYNC}}$ and SYNC_T settings. Because SYNC_T only determines the sync polarity in video DAC mode, this signal has *don't care* status when no sync insertion takes place that is, when $\overline{\text{SYNC}}$ is high. The THS8135 uses the logic level on the SYNC_T input when $\overline{\text{SYNC}}$ is high to enter generic DAC mode: SYNC_T and $\overline{\text{SYNC}}$ are high → generic DAC mode. Therefore, the user must make sure to keep SYNC_T low outside the sync insertion period (when $\overline{\text{SYNC}}$ is high) to prevent entering generic DAC mode, when he intends to use the device in video DAC mode.

Table 3 shows how to select between video DAC and generic DAC mode.

Table 3. Video vs Generic Mode Selection

$\overline{\text{SYNC}}$	$\overline{\text{BLANK}}$	SYNC_T	OPERATION MODE AND DAC OUTPUT
1	1	1	Generic DAC mode. Blanking override inactive.
1	0	1	Generic DAC mode. Blanking override active. Blanking level position is according to the codes of Table 7, however no dc bias is present on the Y, R, G, and B outputs
1	1	0	Video DAC mode. Blanking override inactive
1	0	0	Video DAC mode. Blanking override active. Blanking level position is according to the codes of Table 7, with dc bias present on the Y, R, G, and B outputs as shown in Figure 1 and Figure 3.
0	X	0	Video DAC mode. Negative sync inserted.
0	X	1	Video DAC mode. Positive sync inserted.

Device Configuration Using M1 and M2 in Video DAC Mode

In the video DAC mode, the configuration signals M1 and M2 are both sampled on the second rising edge of the CLK input signal after a L → H or H → L transition on $\overline{\text{SYNC}}$. Depending on the polarity of this last transition on $\overline{\text{SYNC}}$, M1 and M2 are interpreted differently by the THS8135, as shown in Table 4.

NOTE

In the THS8133, only M2 is a sampled signal while M1 is continuously interpreted. By doing so here, the additional input control signal BLNK_INT is generated. See the *backward compatibility with the THS8133* section.

Table 4. Interpretation of M1 in Video DAC Mode

IF LAST EVENT ON $\overline{\text{SYNC}}$ IS:	THEN M1 IS INTERPRETED ON THE SECOND CLK RISING EDGE FOLLOWING THIS EVENT AS:	DESCRIPTION
H → L	BLNK_INT	Sets operation with full or video (ITU-R.BT601) - input code range that is, the full-scale range is reached from either the 0-1023 10-bit input code range or the input code range of Table 8, see also Table 7 for blanking level positions.
L → H	M1_INT	Sets device operation mode. See Table 6 and Table 7.

Table 5. Interpretation of M2 in VIdeo DAC Mode

IF LAST EVENT ON $\overline{\text{SYNC}}$ IS:	THEN M2 IS INTERPRETED ON THE SECOND CLK RISING EDGE FOLLOWING THIS EVENT AS:	DESCRIPTION
H → L	INS3_INT	Sets sync Insertion mode: $\overline{\text{SYNC}}$ low enables sync generation on one (INS3_INT = L) or all three (INS3_INT = H) DAC outputs. SYNC_T determines the sync polarity.
L → H	M2_INT	Sets device operation mode. See Table 6 and Table 7.

Device Configuration Using M1 and M2 in Generic DAC Mode

To simplify device configuration in the generic DAC mode, the M1 and M2 configuration pins are continuously interpreted as M1_INT and M2_INT respectively, that is, their interpretation is not dependent on the last event on $\overline{\text{SYNC}}$ and is not only sampled on the second rising CLK edge after a transition on $\overline{\text{SYNC}}$. BLNK_INT and INS3_INT controls are not available in generic mode. As a result, in generic DAC mode, the device always operates with full-scale input range and no sync insertion is available.

M1_INT and M2_INT can be tied high or low externally to determine the input formatter setting and color space for blank level positions. Blanking override is still available in generic DAC mode using the $\overline{\text{BLANK}}$ input. Generic DAC mode only disables the dc bias for R, G, B, and Y component outputs.

Table 3 shows all combinations of these control signals. Note that when $\overline{\text{SYNC}}$ is low, it takes precedence over $\overline{\text{BLANK}}$.

Selection of Color Space and Input Formatter Configuration (Available in Video DAC and Generic DAC Modes)

Input data to the device can be supplied from a 3x10b GBR or YCbCr input port. If the device is configured to take data from all three channels, the data is clocked in at each rising edge of CLK. All three DACs operate at the full clock speed of CLK.

In the case of 4:2:2 sampled data (for YCbCr data), the device can be fed over either a 2x10 bit or 1x10 bit multiplexed input port. An internal demultiplexer routes the input samples to the appropriate DAC: Y at the rate of CLK, Cb and Cr each at rate of 1/2 CLK.

According to ITU-R.BT-656, the sample sequence is Cb-Y-Cr-Y over a 1x10-bit interface (Y-port). The sample sequence starts at the first rising edge of CLK after BLANK has been taken high (inactive). Note that in this case the frequency of CLK is 2x the Y conversion speed and 4x the conversion speed of both Cr and Cb.

In the case of a 2x10 bit input interface, both the Y-port and the Cr-port are sampled on every CLK rising edge. The Cr-port carries the sample sequence Cb-Cr. The sample sequence starts at the first rising edge of CLK after BLANK has been taken high (inactive). Note that in this case the frequency of CLK is equal to the conversion speed of Y and 2x the conversion speed of both Cr and Cb.

Table 6 shows the possible configurations of the input formatter, as determined by the internal M1_INT and M2_INT signals. The color space selection also determines the position of the blanking level and is explained in the next section.

Table 6. THS8135 RGB/YCbCr Color Space and Input Formatter Configuration

M1_INT	M2_INT	CONFIGURATION	DESRIPTION
L	L	GBR 3x10b-4:4:4	GBR mode 4:4:4. Data clocked in on each rising edge of CLK from G, B, and R input channels.
L	H	YCbCr 3x10b-4:4:4	YCbCr mode 4:4:4. Data clocked in on each rising edge of CLK from Y, Cb, and Cr input channels.
H	L	YCbCr 2x10b-4:2:2	YCbCr mode 4:2:2 2x10 bit. Data clocked in on each rising edge of CLK from Y channel. A sample sequence of Cb-Cr should be applied to the Cr port. At the first rising edge of CLK after BLANK is taken high, Cb should be present on this port.
H	H	YCbCr 1x10b-4:2:2	YCbCr mode 4:2:2 1x10 bit (ITU-R.BT-656 compliant). Data clocked in on each rising edge of CLK from Y channel. A sample sequence of Cb-Y-Cr-Y should be applied to the Y port. At the first rising edge of CLK after BLANK is taken high, Cb should be present on this port.

Selection of Full-Scale or Reduced-Scale ITU.BT601 Modes (Available in Video DAC Mode Only)

In video DAC mode, BLNK_INT sets the blanking level generated on the DAC outputs as shown in Table 7. This allows imposing a blanking level on the analog outputs corresponding to either full-scale code range or a reduced-scale code range compliant to ITU-R.BT601. The blanking level is correctly positioned for either RGB or YCbCr configurations, determined from the M1/M2 setting.

For generic DAC mode, BLNK_INT control is not available and the device always generates an output level during BLANK low assuming full-scale input code range.

Table 7. Full-Scale or ITU.BT601 Reduced-Scale Mode Selection and Impact on Blanking Level Positioning

M1_INT	M2_INT	BLNK_INT	AVAILABLE IN VIDEO DAC (V) AND GENERIC DAC (G) MODES?	OPERATION MODE	CHANNEL OUTPUT LEVEL DURING BLANK ACTIVE CORRESPONDING TO DAC INPUT CODE:		
					AGY	ABPb	ARPr
L	L	L	V, G	GBR 3x10b 4:4:4, full scale range	0	0	0
L	L	H	V	GBR 3x10b 4:4:4, ITU-R.BT601-compliant range	64	64	64
L	H	L	V, G	YCbCr 3x10b 4:4:4, full scale range	0	512	512
L	H	H	V	YCbCr 3x10b 4:4:4, ITU-R.BT601-compliant range	64	512	512
H	L	L	V	YCbCr 2x10b 4:2:2, ITU-R.BT601-compliant range	64	512	512
H	L	H	V, G	YCbCr 2x10b 4:2:2, full scale range	0	512	512
H	H	L	V	YCbCr 1x10b 4:2:2, ITU-R.BT601-compliant range	64	512	512
H	H	H	V, G	YCbCr 1x10b 4:2:2, full scale range	0	512	512

In full-scale range, the DAC is driven with input codes 0-1023 to the desired video level, set by the resistor connected to the FSADJ terminal (for example, a full-scale video amplitude of 700 mV when terminated into 37.5 Ω and when using the nominal R_{FS} value).

In reduced-scale ITU-R.BT601 range, it is the intention that full-scale video amplitude is reached when the device is driven with digital inputs within the input code range shown in Table 8. Note that the code range is unequal between RGBY on one hand and CbCr on the other hand. Figure 1 through Figure 4 illustrates the difference between ITU-R.BT601 reduced-scale and full-scale code range operation. In reduced-range configuration, the B/Cb and R/Cr components are digitally amplitude scaled internally. Note that there is no scaling on the G/Y component. Therefore, to accommodate the 700-mV video compliance on all components, the DAC full-scale output current needs to be increased between full-scale and reduced scale modes by a factor of 1023/(940-64) by decreasing R_{FS} in that proportion.

This implementation has the advantage of avoiding amplitude scaling on the most critical G/Y component, while still providing the possibility for instantaneous overshoot/undershoot on the analog component video output when illegal signals according to ITU-R.BT601, such as super-black or super-white, are applied to the device.

When using reduced-scale range, the output sync:video amplitude ratio is still 7:3, but now takes into account the reduced code range, not the full-scale range, to determine this ratio. Therefore, proper sync amplitudes are preserved in either mode, when the full-scale current is modified as explained higher. When changing DAC full-scale current using R_{FS}, the sync amplitude level always scales proportionally with the video output compliance.

Note that even when using reduced-scale range, the midscale blanking level on ABPb and ARPr channels still corresponds to code 512 = [64+(960-64)/2] when using YCbCr color space configuration. Table 8 shows the valid reduced input code ranges for RGB and YCbCr operation on each of the input data buses. While the THS8135 allows reduced-scale code range with RGB data, video systems normally use it only with YCbCr type data.

Table 8. Input Code Ranges for ITU.BT601 Modes

OPERATING MODE	GY[ ]	RPr[ ]	BPb[ ]
RGB	64-940	64-940	64-940
YCbCr	64-940	64-960	64-960

DAC Operation

The analog output drivers generate a current of which the drive level can be user-modified by choosing an appropriate resistor value R_{FS}, connected to the FSADJ pin.

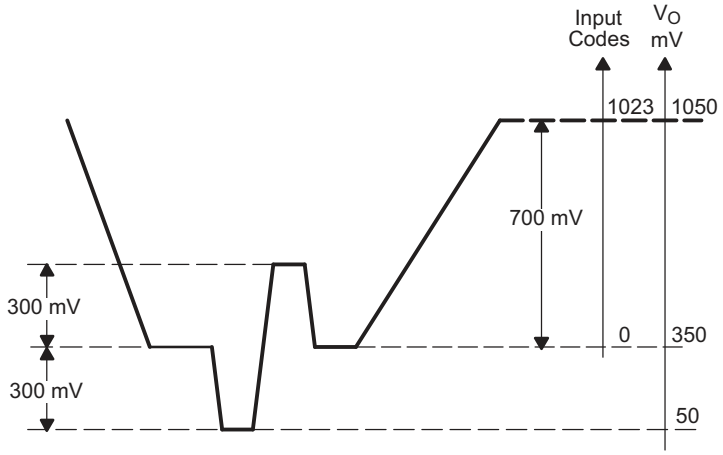
All current source amplitudes (video, blanking, and sync) are derived from an internal voltage reference such that the relative amplitudes of sync, blank, and video are always equal to their nominal relationships.

Figure 1 through Figure 4 show the nominal output voltage levels for full- or reduced-range input code range configurations on R, G, B, and Y versus Cb and Cr channels.

Note that in full-scale input code range configuration, the blanking level is at 350 mV on all outputs; while in reduced-scale operation it is at 400 mV on all outputs.

In reduced scale modes, after proper adjustment of R_{FS}, the nominal 700-mV output compliance is reached from an input code range of only 876 (= 940-64) codes on G/Y, and of only 896 (= 960-64) codes on R/Pr and B/Pr output channels. The maximum excursions are ~817 mV (= 1023/876 × 700 mV) on G/Y and ~800 mV (= 876/896 × 817 mV) on B/Pb and R/Pr channels. Figure 4 shows that when using reduced-scale input code range, the blanking level needs to be at 400 mV to accommodate the maximum negative excursion on B/Pr and R/Pr channels.

The figures also show the excursions for the sync level positions in either full-scale or reduced-scale configurations. These levels are internally adjusted and assure 300-mV sync excursions when using nominal termination loads and properly adjusting R_{FS}, as previously explained.



NOTE: Choose R_{FS} for 700 mV from input codes 0−1023 on Y.

Figure 1. YRGB Outputs, Full-Scale Input Code Range

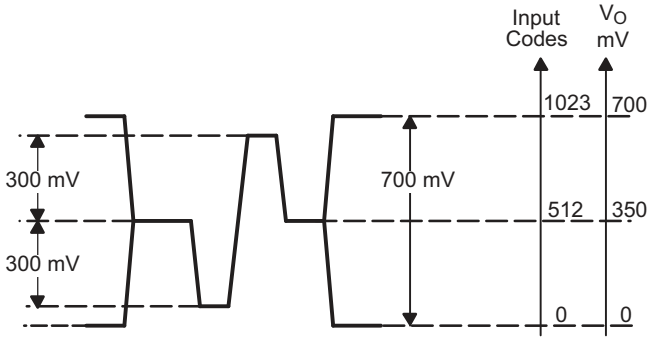
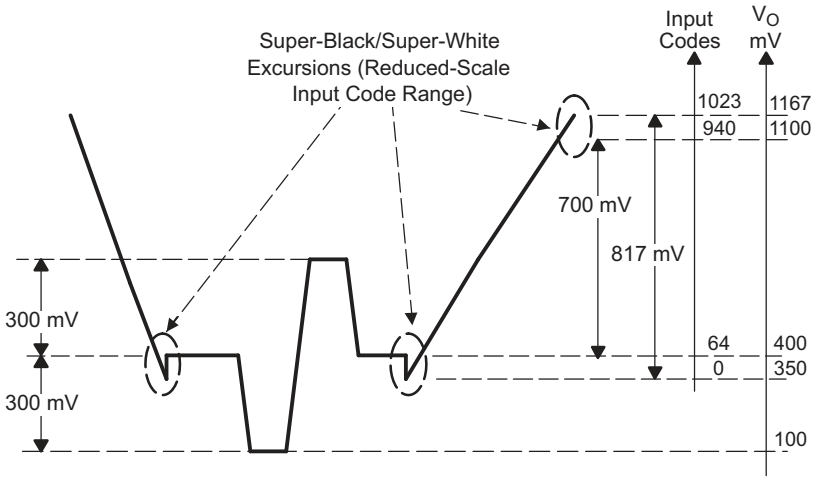


Figure 2. CbCr Outputs, Full-Scale Input Code Range



NOTE: Choose RFS for 700 mV from input codes 64−940 on Y.

Figure 3. YRGB Outputs, Reduced-Scale Input Code Range

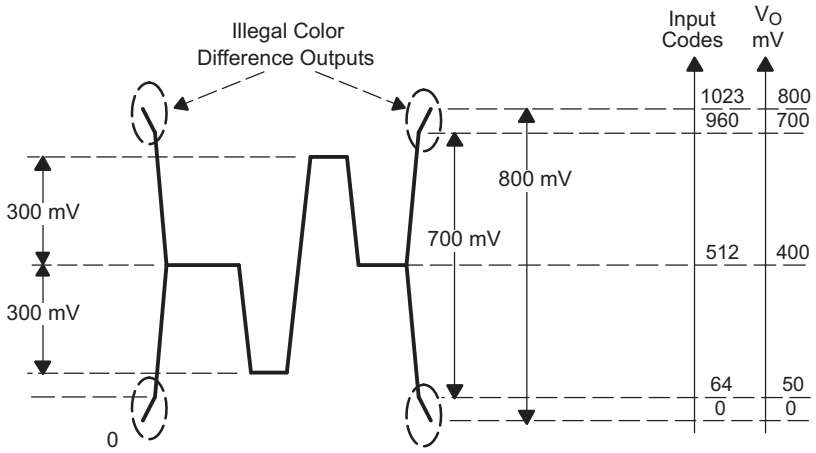


Figure 4. CbCr Outputs, Reduced-Scale Input Code Range

Output Amplitude Control

The current drive on all three output channels (including sync) is controlled by a resistor R_{FS} that must be connected between FSADJ and AVSS. In all operation modes the relative amplitudes of these current drivers are maintained irrespective of the R_{FS} value, as long as a maximum current drive capability is not exceeded. Therefore, a 7:3 video to sync ratio is preserved when adjusting $R_{FS.}$

The sync generator is composed of different current sources that are internally routed to a corresponding DAC output. Because they are additional to the video DACs, full 10-bit DAC resolution is preserved for video. Depending on the setting of INS3_INT during $\overline{\text{SYNC}}$ low, the sync current drive is added to either only the green channel output (sync-on-G/Y) if INS3_INT = L or all three channel outputs (sync-on-all) if INS3_INT = H. Sync insertion is only available in video DAC mode.

Figure 5 shows the relationship between R_{FS} and the current drive level on each channel for full-range DAC input. When using reduced-scale range, the codes on the G/Y channel are not internally scaled (only BCb and RCr channels are scaled). Therefore, the user should increase the DAC full-scale current by decreasing R_{FS} by a factor of 1023/(940-64) to map the reduced-scale Y input code range to the same output current drive level. Because these are the current drive levels for the video DACs, they do not take into account the additional dc bias for sync insertion when using video DAC mode. The voltage compliance outputs in Figure 5 assume termination with a 37.5-Ω resistor.

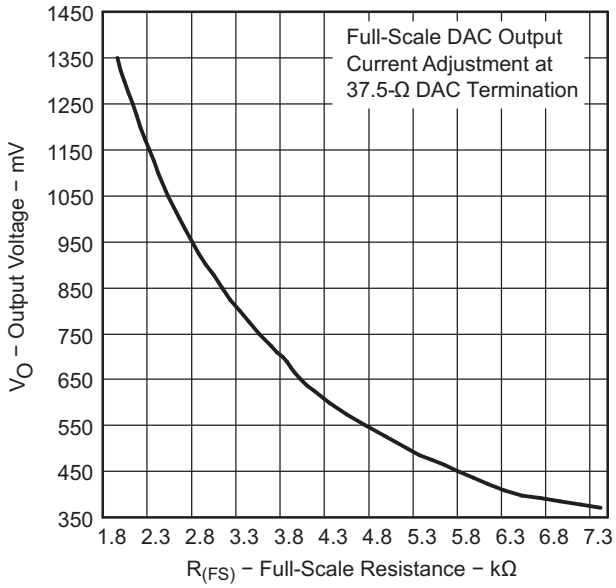


Figure 5. Output Voltage vs Full-Scale Resistance

The user is free to connect another resistor value, but care should be taken not to exceed the maximum current level on each of the DAC outputs as shown in the specifications section.

Backward Compatibility With the THS8133

Power Supply

The THS8135 is a functional superset to the THS8133 and is footprint compatible that is a board designed for the THS8133 can also be used with the THS8135. Both devices come in the same package and have identical pinouts. Only the power supply levels need to be adjusted as shown in Table 9.

Table 9. Power Supply Changes THS8133 vs THS8135

	THS8133	THS8135
AV_{DD}	5 V	3.3 V
DV_{DD}	3.3 V to 5 V	1.8 V

Device Configuration

The THS8135 samples both M1 and M2 on the second rising edge of CLK after a transition on $\overline{SYNC}$ in video modes. Depending on the polarity of the transition, M1 is interpreted as either M1_INT or BLK_INT. In the THS8133 the M1 signal is not sampled but continuously interpreted, and is only interpreted as M1_INT. The THS8133 does not offer a reduced-scale input code range configuration and therefore does not require BLNK_INT.

Only when this additional functionality, which is typical for video systems, is desired, a small change in the configuration of the device is required by supplying a dynamically changing signal on M1, generated in a similar way as M2, as shown in Table 10.

Note that this backward compatibility is due to the selection of full-scale versus reduced-scale configurations in Table 7. All configurations that have equal logic levels for BLNK_INT and M1_INT produce full-scale input code range, which are compatible with the THS8133. This allows the use of a signal tied high or low on M1, as on the THS8133, for these backward compatible full-scale configurations.

DAC Outputs

The position of the blanking levels in the THS8135 differs from the position of the blanking levels in the THS8133. This is to accommodate both full- and reduced-scale configurations on this device, while the THS8133 only supported full-scale. When the DAC output is ac-coupled, as is typically the case, there is no change to the output video waveform. Typically a clamp circuit at the receiving side will restore the signal to the proper dc level.

Video DAC Mode vs Generic DAC Mode

The THS8133 does not offer a generic DAC mode. The THS8135 uses only the same number of control signals than the THS8133 but additionally introduces a generic video mode by specific use of a *don't care* signal combination of these control signals on the THS8133.

Programming Example for M2 (1)

Configuration of the device is normally static in a given application, although it is theoretically possible to reconfigure the device during operation.

If M2_INT and INS3_INT need to be either low or high, the M2 pin is simply tied low or high. If M2_INT and INS3_INT need to have different levels, these can be easily derived from the signal on the $\overline{\text{SYNC}}$ pin, as shown in Table 10 and Figure 6.

(1) Programming M1 is analogous.

Table 10. Generating M2 From $\overline{\text{SYNC}}$

TO HAVE:		APPLY TO M2:
M2_INT	INS3_INT	
L	H	... $\overline{\text{SYNC}}$ delayed by two CLK periods
H	L	... inverted $\overline{\text{SYNC}}$ delayed by two CLK periods

M1 can be generated similarly. Therefore, at most one inverter and two flip flops are needed to configure any of the THS8135 modes using M1 and M2.

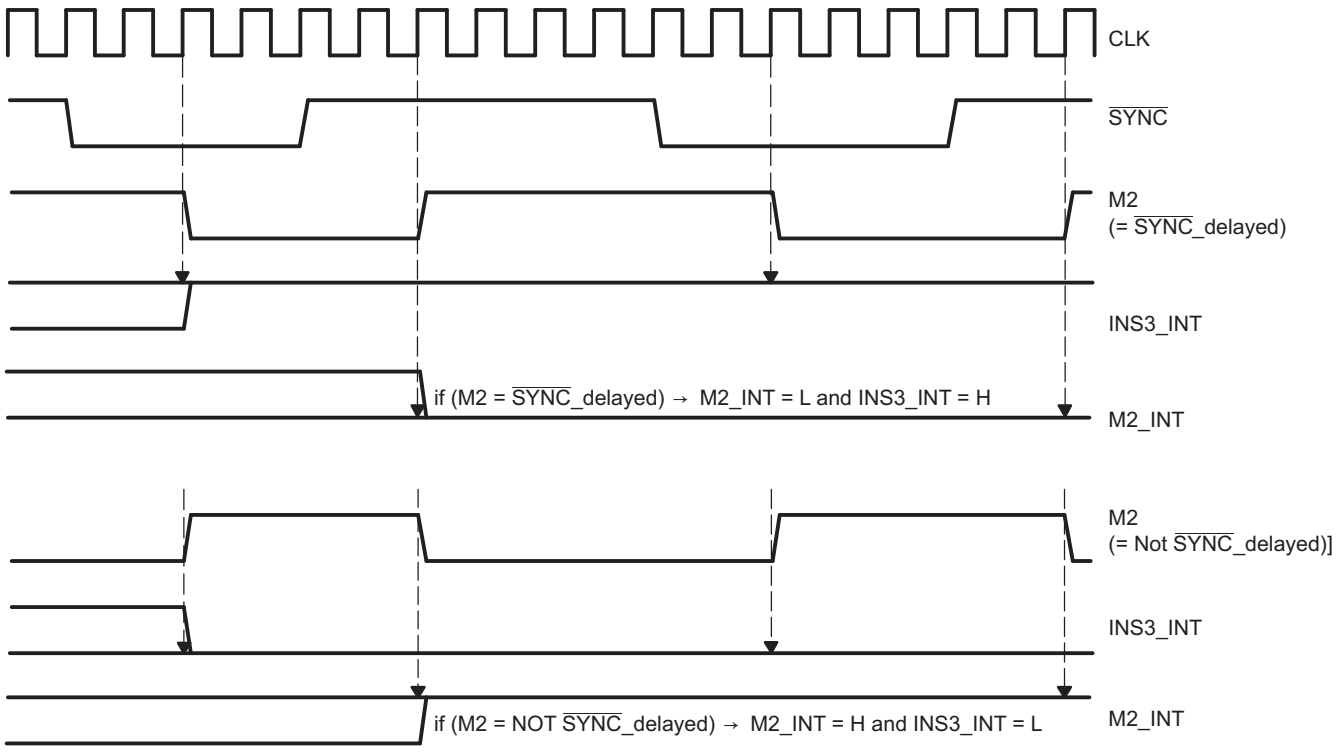


Figure 6. Generating INS3_INT and M2_INT From M2

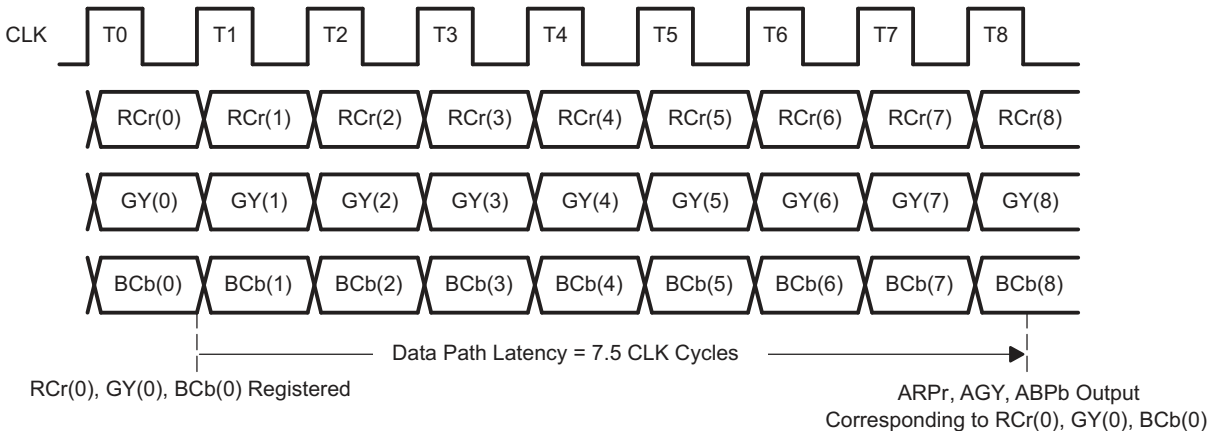


Figure 7. Input Format and Latency YCbCr 4:4:4 and GBR 4:4:4 Modes

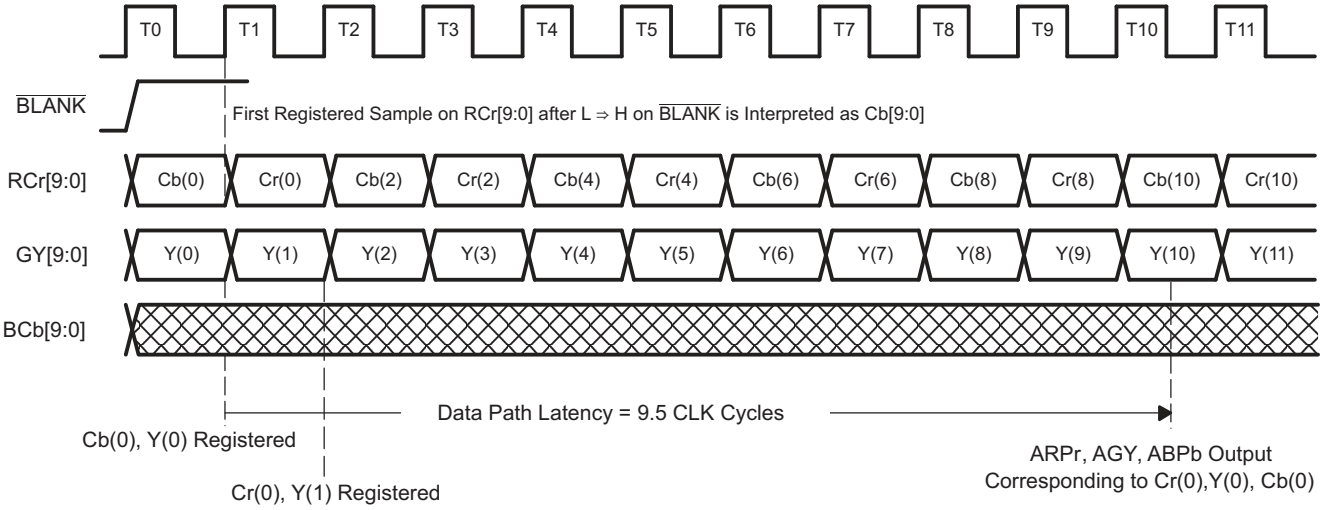


Figure 8. Input Format and Latency YCbCr 4:2:2 2x10-Bit Mode

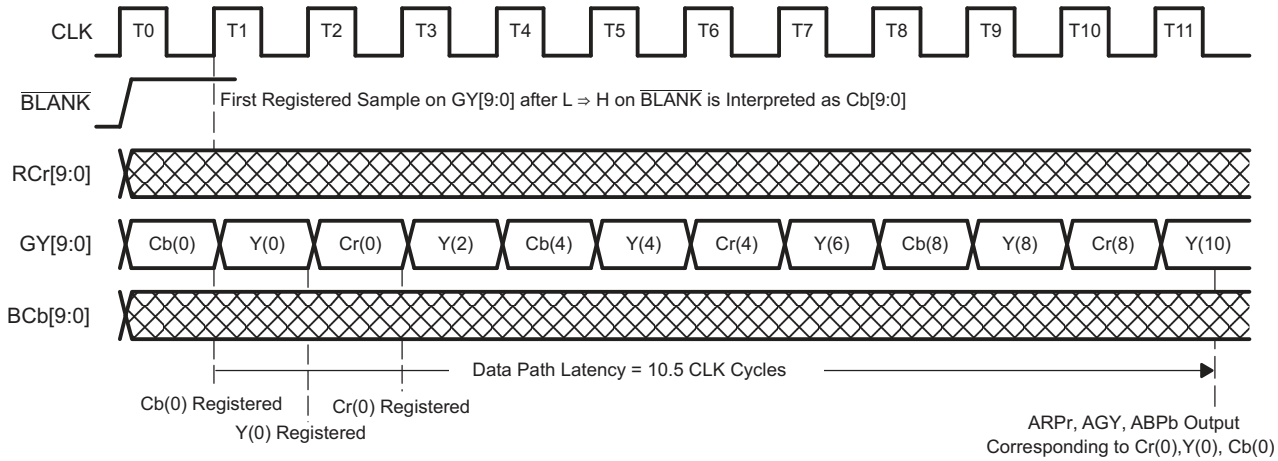


Figure 9. Input Format and Latency YCbCr 4:2:2 1x10-Bit Mode

Figure 10 shows how to control the $\overline{\text{SYNC}}$, SYNC_T, and $\overline{\text{BLANK}}$ signals to generate tri-level sync levels and blanking at the DAC output in video mode. A bi-level (negative) sync can be generated similarly by avoiding the positive transition on SYNC_T during $\overline{\text{SYNC}}$ low.

Note that on the THS8135 it is required to keep SYNC_T low outside the sync interval to avoid entering the generic DAC mode.

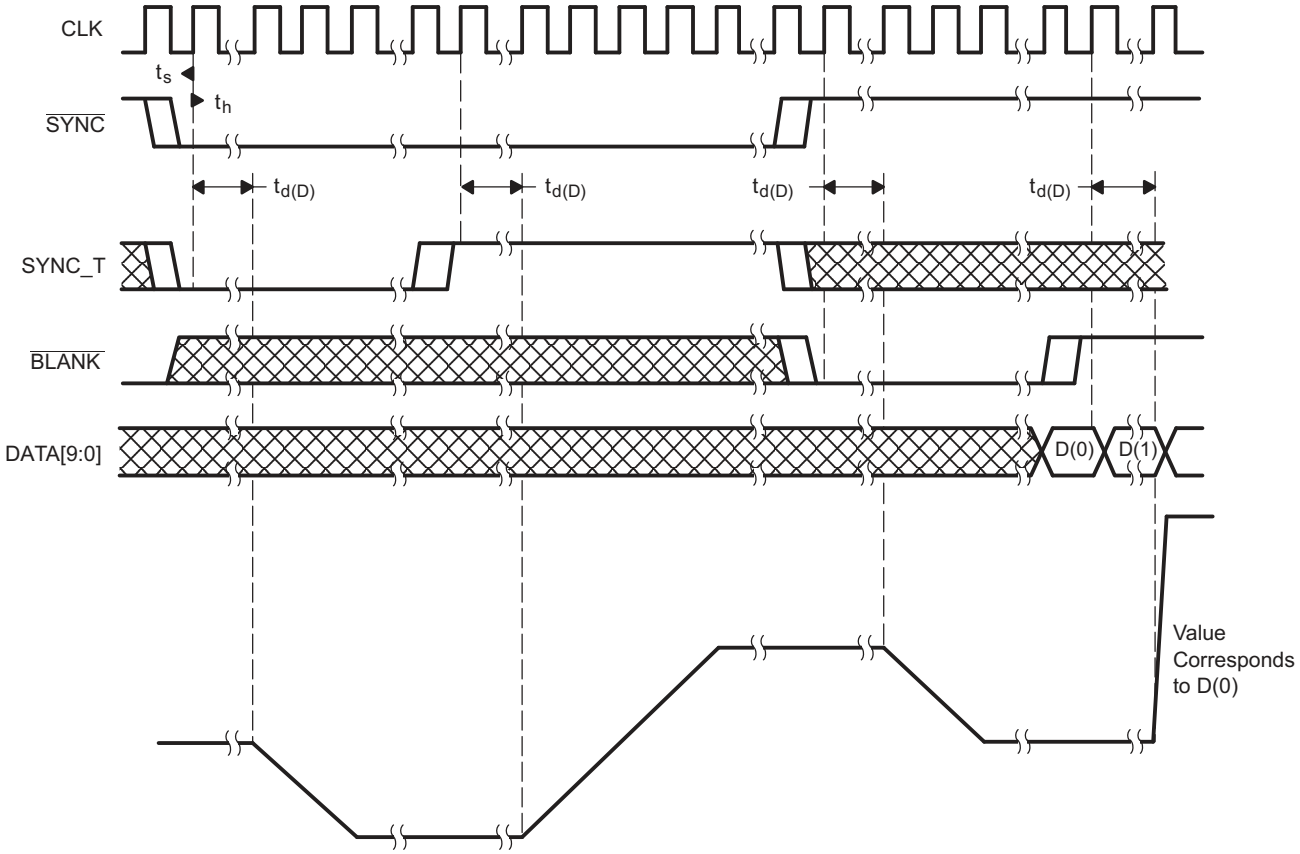


Figure 10. Sync and Blanking Generation

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

V_{DD}	Supply voltage	AV_{DD} to AV_{SS}	-0.5 V to 3.6 V
		DV_{DD} to DV_{SS}	-0.5 V to 2 V
	Supply voltage, difference between analog and digital supplies	AV_{DD} to DV_{DD}, AV_{SS} to DV_{SS}	-0.5 to 0.5 V
	Digital input voltage range to DV_{SS}		-0.5 V to DV_{DD} + 0.5 V
T_A	Operating free-air temperature range		0°C to 70°C
T_{stg}	Storage temperature range		-55°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Thermal Specifications

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air	Thermal PAD soldered to 4-layer High-K PCB		29.11		°C/W
		Low-K PCB, Thermal PAD not soldered		64.42		
θ_{JC}	Junction-to-case thermal resistance, still air			0.12		°C/W
$T_{J(MAX)}$	Maximum junction temperature for reliable operation				105	°C

(1) When split ground planes are used, attach the thermal pad to the analog ground plane.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Power Supply						
V_{DD}	Supply voltage	AVDD	3	3.3	3.6	V
		DVDD	1.65	1.8	2	
Digital and Reference Inputs						
V_{IH}	High-level input voltage		1.2		DV_{DD}	V
V_{IL}	Low-level input voltage		DV_{SS}		0.7	V
f_{clk}	Clock frequency		0		240	MHz
$t_{w(CLKH)}$	Clock high pulse duration		40%		60%	CLK period
$t_{w(CLKL)}$	Clock low pulse duration		40%		60%	CLK period
R_{FS}	FSADJ resistor(1)			3.8		kΩ

(1) R_{FS} should be chosen such that the maximum full-scale DAC output current (I_{FS}) does not exceed their maximum stated levels. This yields the nominal output voltage compliance at the nominal load termination of 37.5 Ω.

Electrical Characteristics

over recommended operating conditions with f_{CLK} = 240 MSPS and use of internal reference voltage V_{REF}, with $R_{FS} = R_{FS(nom)}$ and 37.5-Ω load termination (unless otherwise noted)

Power Supply

1 MHz, -1 dBFS digital sine simultaneously applied to all three channels

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IAV_{DD}	Operating supply current, analog	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 80 MSPS	RGB	89	95	100	mA
			YCbCr	71	76	80	
			Generic (700 mV)	63	66	69	
IDV_{DD}	Operating supply current, digital	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 80 MSPS	RGB	14.5	15.1	15.7	mA
			YCbCr	11.7	12.15	12.7	
			Generic (700 mV)	14.64	15.1	15.7	
P_D	Power dissipation	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 80 MSPS	RGB	328	338	350	mW
			YCbCr	262	270	280	
			Generic (700 mV)	237	245	252	
IAV_{DD}	Operating supply current, analog	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 240 MSPS	RGB	89	95	100	mA
			Generic (700 mV)	63	66	69	
IDV_{DD}	Operating supply current, digital	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 240 MSPS	RGB	38	40	41	mA
			Generic (700 mV)	38	40	41.1	
P_D	Power dissipation	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 240 MSPS	RGB	373	384	394	mW
			Generic (700 mV)	281	290	298	
IAV_{DD}	Operating supply current, analog	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 80 MSPS	Generic (1.3 V)		114		mA
IDV_{DD}	Operating supply current, digital	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 80 MSPS	Generic (1.3 V)		16		mA
P_D	Power dissipation	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 80 MSPS	Generic (1.3 V)		405		mW
IAV_{DD}	Operating supply current, analog	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 240 MSPS	Generic (1.3 V)		114		mA
IDV_{DD}	Operating supply current, digital	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 240 MSPS	Generic (1.3 V)		41		mA
P_D	Power dissipation	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, CLK = 240 MSPS	Generic (1.3 V)		450		mW

Digital Inputs – DC Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level input current	AV_{DD} = 3.3 V, DV_{DD} = 1.8 V, Digital inputs and CLK at 0 V for I_{IL}, Digital inputs and CLK at 2 V for I_{IH}			1	µA
I_{IL}	Low-level input current				-1	µA
$I_{IL(CLK)}$	Low-level input current, CLK		-1		1	µA
$I_{IH(CLK)}$	High-level input current, CLK		-1		1	µA
C_I	Input capacitance	T_A = 25°C		5		pF
t_s	Data and control inputs setup time		2			ns
t_h	Data and control inputs hold time		500			ps
$t_{d(D)}$	Digital process delay from first registered color component of pixel(1)	RGB and YCbCr 4:4:4		7.5		CLK periods
		YCbCr 4:2:2, 2 x 10 bit		9.5		
		YCbCr 4:2:2, 1 x 10 bit		10.5		

(1) This parameter is assured by design. The digital process delay is defined as the number of CLK cycles required for the first registered color component of a pixel, starting from the time of registering it on the input bus, to propagate through all processing and appear at the DAC output drivers. The remaining delay through the IC is the analog delay $t_{d(A)}$ of the analog output drivers.

Analog (DAC) Outputs

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	DAC resolution				10		bits
INL	Integral nonlinearity	Static, best-fit, sync-on-all, video mode, RGB full-scale			-1.1/0.9	-2/1.5	LSB
		Static, best-fit, sync-on-all, video mode, RGB ITU.R-BT601			-1.2/0.8	-2/1.5	
		Static, best fit, generic mode, 1.3 V			-1.61/0.94	-2/1.5	
DNL	Differential nonlinearity	Static, sync-on-all, video mode, RGB full-scale			±0.4	±1	LSB
		Static, sync-on-all, video mode, RGB ITU.R-BT601			±0.5	±1	
		Static, generic mode, 1.3 V			-0.32/0.24		
PSRR	Power supply ripple rejection ratio of DAC output (full scale)	f = DC(1)			38.5		dB
XTALK	Crosstalk between channels(2)	f = 1 MHz			-63		dB
		f = 30 MHz			-39		
V_{refo}	Voltage reference output			1.13	1.15	1.16	V
R_R	VREF output resistance			276.5	284	294	Ω
K_{IMBAL}	Imbalance between DACs	CLK = 80 MSPS(3)	Video mode, RGB full-scale	-2%	1.8%	2%	
			Video mode, RGB ITU-R.BT601	-3%	2.8%	3%	
V_{OC}	DAC output compliance voltage (video only)(4)	Video mode, RGB full-scale			0.7		V
		Video mode, RGB ITU-R.BT601			0.817		
		Generic mode			1.3		
I_{FS}	Video mode, full-scale RGB, sync-on-all	CLK = 80 MSPS(5)	AGY	27	28	29.3	mA
			ABPb and ARPr	27	28	29.3	
	Video mode, full-scale YCbCr, sync-on-all		AGY	27	28	29.3	
			ABPb and ARPr	18	18.67	19.5	
	Video mode, ITU-R.BT601RGB, sync-on-all		AGY	30	31.18	32.0	
			ABPb and ARPr	30	31.18	32.3	
	Video mode, ITU-R.BT601 YCbCr, sync-on-all		AGY	30	31.18	32.1	
			ABPb and ARPr	20	21.39	22.5	
t_{RDAC}	DAC output current rise time	CLK = 80 MSPS, 10 to 90% of full-scale		3.2	3.5	4.2	ns
t_{FDAC}	DAC output current fall time	CLK = 80 MSPS, 10 to 90% of full-scale		3.2	3.5	4.2	ns
$t_{d(A)}$	Analog output delay	Measured from CLK = $V_{IH(min)}$ to 50% of full-scale transition(6)			4		ns
t_S	Analog output settling time	Measured from 50% of full scale transition on output to output settling, within 2%(7)			15		ns
SFDR	Spurious-free dynamic range	1 MHz, -1 dBFS digital sine input			55		dB
BW	Bandwidth	1 dB			50		MHz
		3 dB			100		
E_{glitch}	Glitch energy	Full-scale code transition at 240 MSPS			25		pVs

(1) PSRR is measured with a 0.1-µF capacitor between the COMP and AVDD pin; with a 0.1-µF capacitor connected between the VREF pin and AVSS. The ripple amplitude is within the range 100 mVp-p to 500 mVp-p with the DAC output set to full scale and a double-terminated 75 Ω (= 37.5 Ω) load. PSRR is defined as 20 x log(ripple voltage at DAC output/ripple voltage at AVDD input). Limits from characterization only.
(2) Crosstalk spec applies to each possible pair of the three DAC outputs. Limits are from characterization only.
(3) The imbalance between DACs applies to all possible pairs of the three DACs.
(4) Values at $R_{FS} = R_{FS(nom)}$. Limits from characterization only.
(5) Values at $R_{FS} = R_{FS(nom)}$.
(6) This value excludes the digital process delay, $t_{D(D)}$. Limits from characterization only.
(7) Limit from characterization only. Measured on Y channel with other channels not driven.

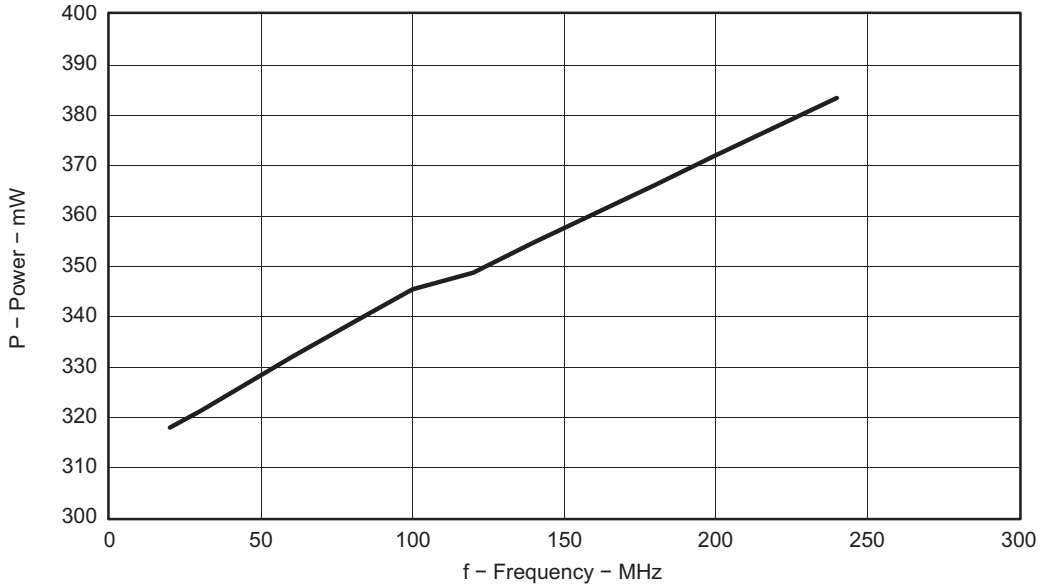


Figure 11. Power vs Clock Frequency, RGB Mode, 1-MHz Input Tone on All Channels

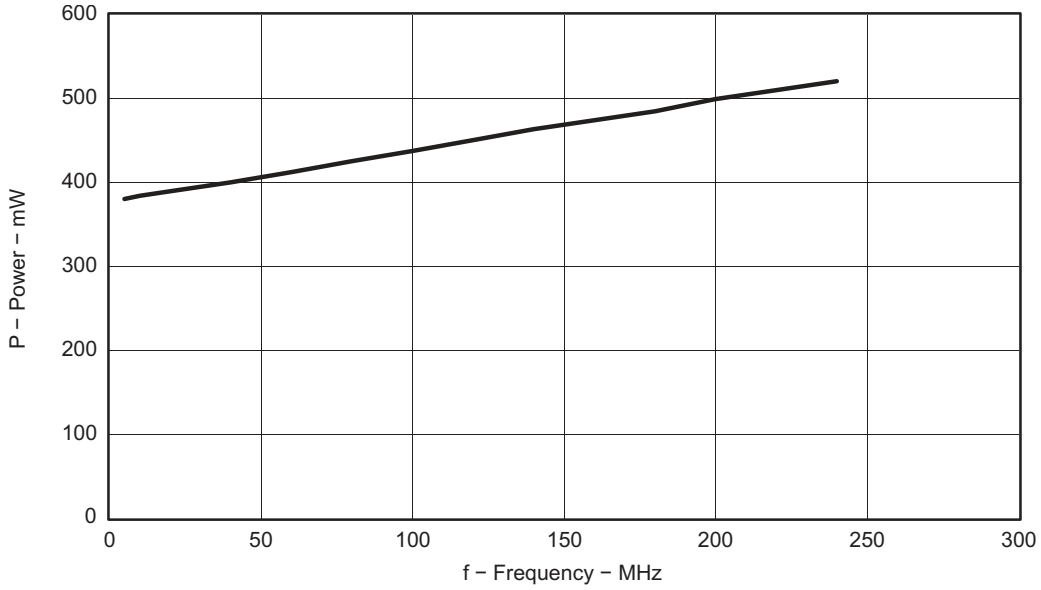


Figure 12. Power vs Clock Frequency, Generic DAC Mode 1.3-V Output, Full-Scale Input Toggle on All Channels

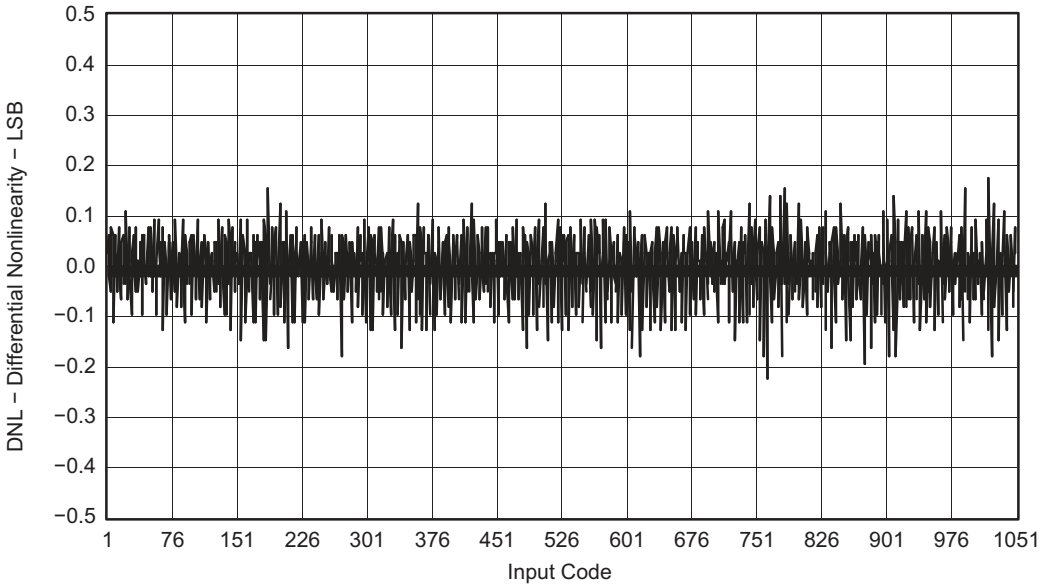


Figure 13. DNL, Generic DAC Mode (1.3-V Output Compliance)

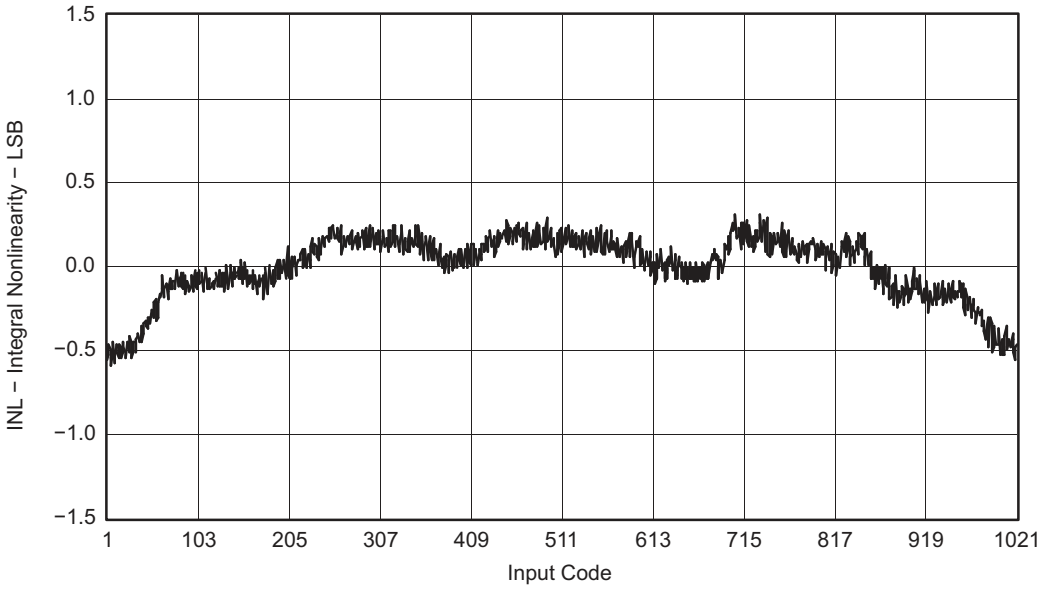


Figure 14. Best-Fit INL, Generic DAC Mode (1.3-V Output Compliance)

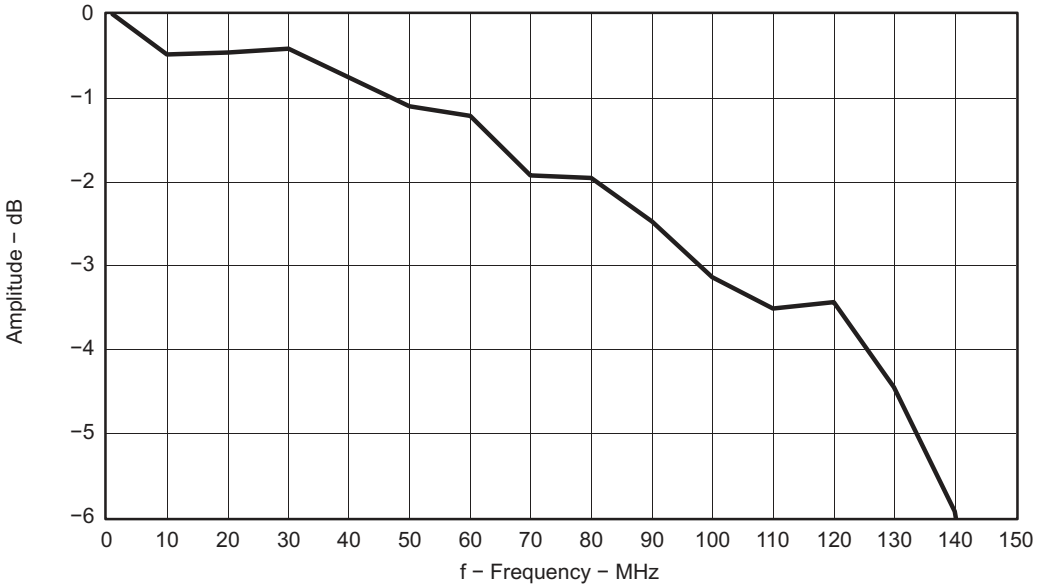


Figure 15. Amplitude Response vs Input Frequency at 240 MSPS

REVISION HISTORY

Revision	Comments
SLAS343B	Added Thermal Specifications.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS8135PHP	ACTIVE	HTQFP	PHP	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	THS8135	Samples
THS8135PHPG4	ACTIVE	HTQFP	PHP	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	THS8135	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

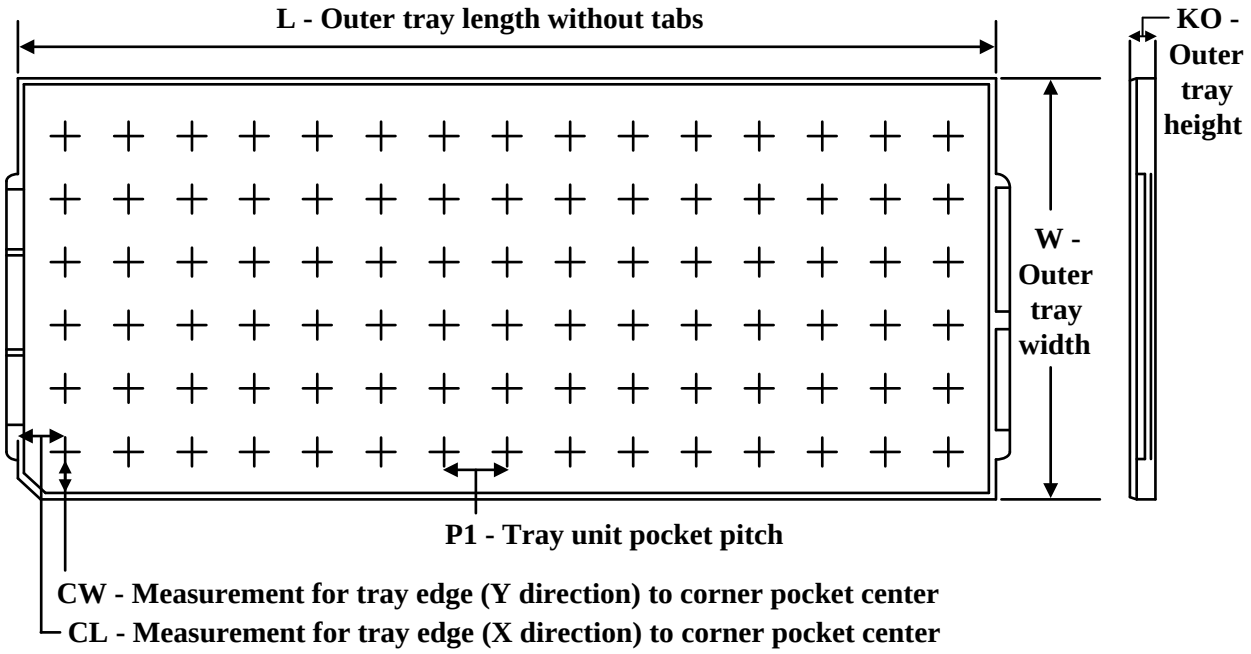
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
THS8135PHP	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
THS8135PHPG4	PHP	HTQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

GENERIC PACKAGE VIEW

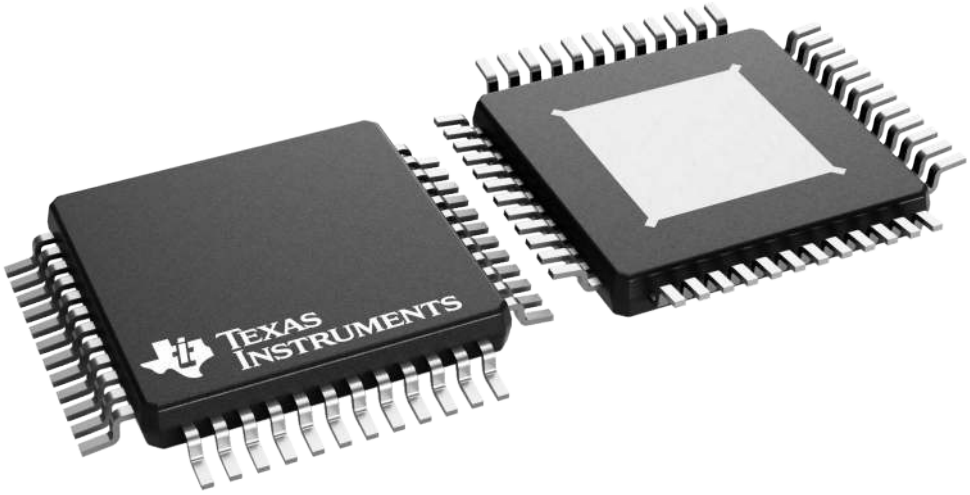
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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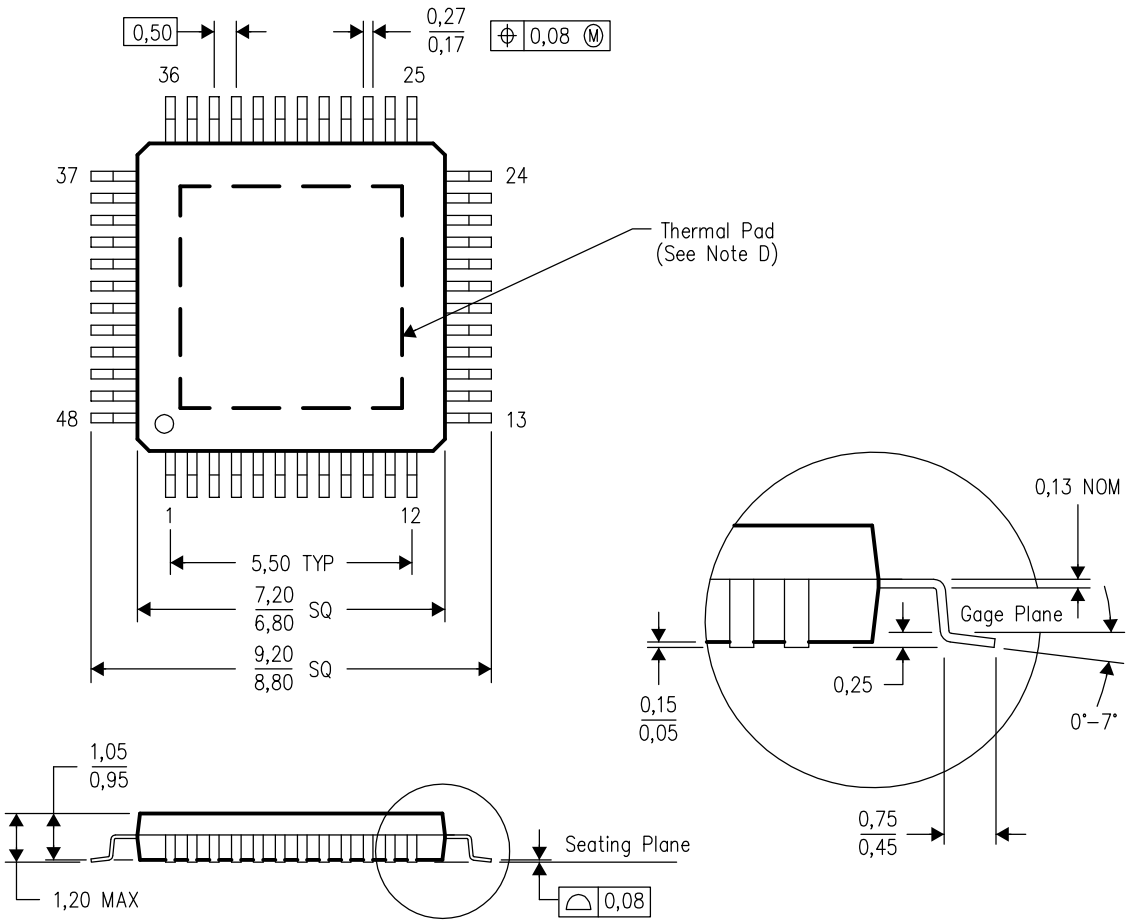
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

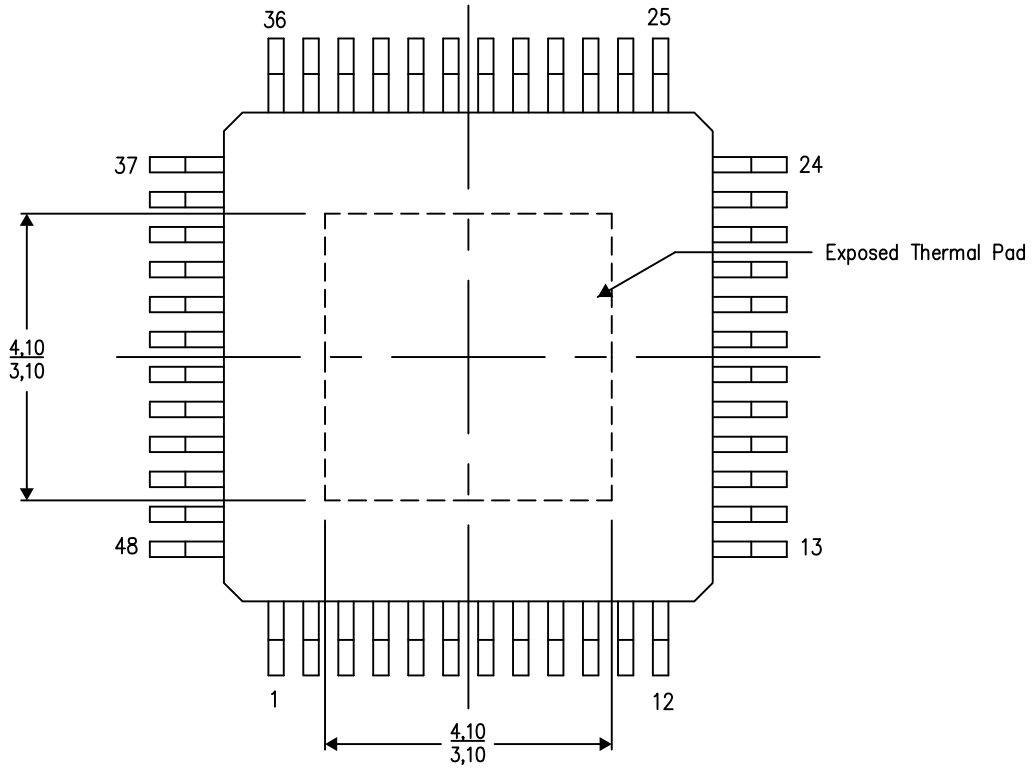
PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

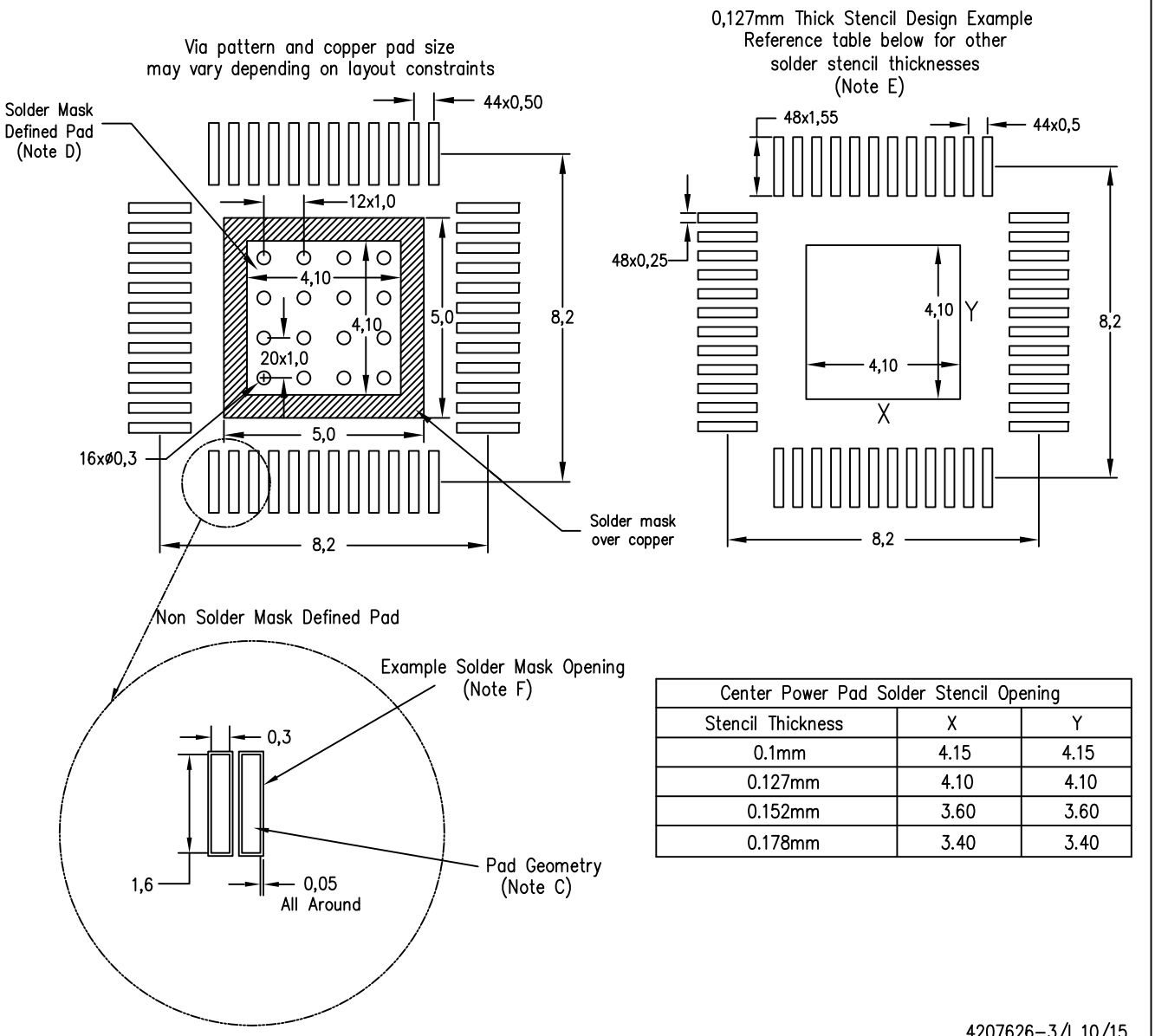
Exposed Thermal Pad Dimensions

4206329–3/P 03/15

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PHP (S–PQFP–G48) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.15	4.15
0.127mm	4.10	4.10
0.152mm	3.60	3.60
0.178mm	3.40	3.40

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting options for vias placed in the thermal pad.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265