

December 1996

Fast CMOS Octal D Registers (Three-State)

Features

- Advanced 0.8 micron CMOS Technology
- Pin Compatible With Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (CD74FCT2374T, CD74FCT2574T only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Description

These devices are 8-bit wide octal registers designed with eight D-type flip-flops with a buffered common clock and buffered three-state outputs. When output enable (\overline{OE}) is LOW, the outputs are enabled. When \overline{OE} is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock input.

All CD74FCT2574T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT374ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT374ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT374CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT374CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT374DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT374DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT374TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT374TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT534ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT534ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT534CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT534CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT534DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT534DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT534TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT534TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT574ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT574ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT574CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT574CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT574DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT574DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT574TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT574TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2374ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2374ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2374CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2374CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2374TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2374TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2574ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2574ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2574CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2574CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2574TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2574TQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

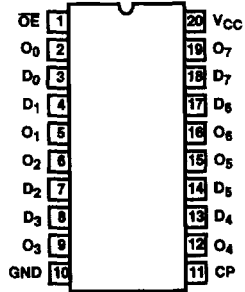
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OCTAL 5V FCT
5V FCT 25Ω

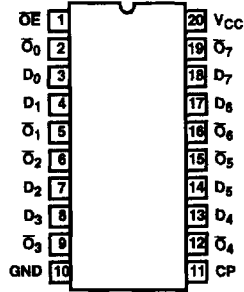
CD74FCT374T, CD74FCT534T, CD74FCT574T, CD74FCT2374T, CD74FCT2574T

Pinouts

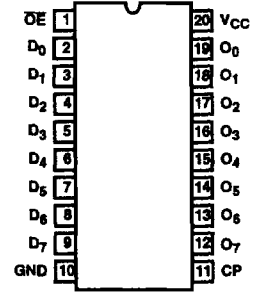
CD74FCT374T, CD74FCT2374T
(QSOP, SOIC)
TOP VIEW



CD74FCT534T
(QSOP, SOIC)
TOP VIEW

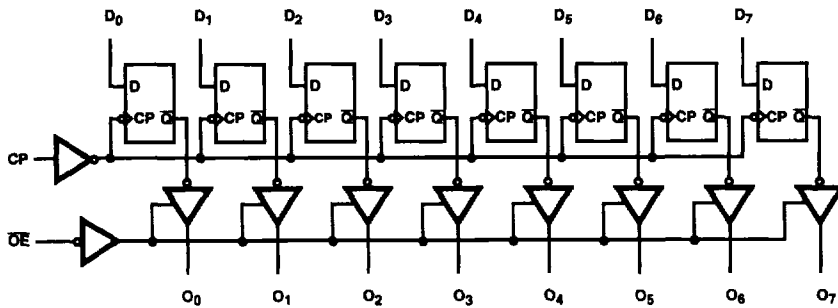


CD74FCT574T, CD74FCT2574T
(QSOP, SOIC)
TOP VIEW

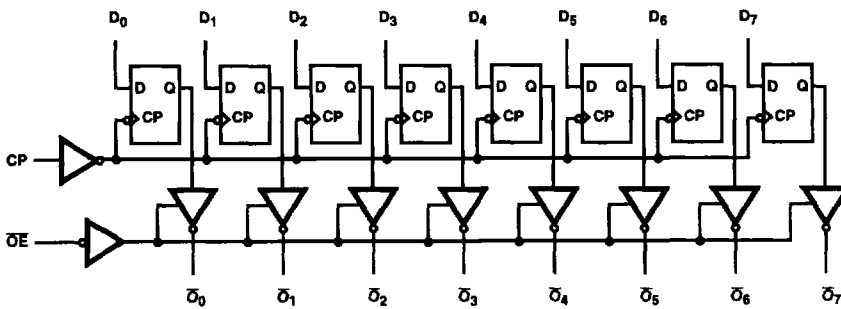


Functional Block Diagrams

CD74FCT374T, CD74FCT2374T, CD74FCT574, CD74FCT2574T



CD74FCT534T



CD74FCT374T, CD74FCT534T, CD74FCT574T, CD74FCT2374T, CD74FCT2574T

TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	\overline{OE}	CP	D_N	$\overline{O_N}$	Q_N
CD74FCT534T					
High-Z	H	L	X	Z	NC
	H	H	X	Z	NC
Load Register	L	↑	L	H	L
	L	↑	H	L	H
	H	↑	L	Z	L
	H	↑	H	Z	H
CD74FCT374T, CD74FCT574T, CD74FCT2374T, CD74FCT2574T					
FUNCTION	\overline{OE}	CP	D_N	O_N	$\overline{Q_N}$
High-Z	H	L	X	Z	NC
	H	H	X	Z	NC
Load Register	L	↑	L	L	H
	L	↑	H	H	L
	H	↑	L	Z	H
	H	↑	H	Z	L

NOTE:

- 1. H = High Voltage Level
- L = Low Voltage Level
- X = Don't Care
- Z = High Impedance
- NC = No Change
- ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
\overline{OE}	Output Enable Input (Active LOW)
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition
D_0 - D_7	Data Inputs
O_0 - O_7	Three-State Outputs (True)
\overline{O}_0 - \overline{O}_7	Three-State Outputs (Inverted)
GND	Ground
VCC	Power

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OCTAL 5V FCT
5V FCT 25Ω

CD74FCT374T, CD74FCT534T, CD74FCT574T, CD74FCT2374T, CD74FCT2574T

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 12)		(NOTE 12)		(NOTE 12)		(NOTE 12)		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
CD74FCT374T, CD74FCT534T, CD74FCT2374T											
Propagation Delay CP to \bar{O}_N	t_{PLH} , t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	2.0	10.0	2.0	6.5	2.0	5.2	2.0	4.5	ns
Output Enable Time OE to \bar{O}_N	t_{PZH} , t_{PZL}		1.5	12.5	1.5	6.5	1.5	5.5	1.5	5.5	ns
Output Disable Time (Note 13) OE to \bar{O}_N	t_{PHZ} , t_{PLZ}		1.5	8.0	1.5	5.5	1.5	5.0	1.5	5.0	ns
Setup Time HIGH or LOW, D_N to CP	t_{SU}		2.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D_N to CP	t_H		1.5	-	1.5	-	1.5	-	1.0	-	ns
CP Pulse Width (Note 13) HIGH or LOW	t_W		7.0	-	5.0	-	5.0	-	3.0	-	ns
CD74FCT574T, CD74FCT2574T											
Propagation Delay CP to \bar{O}_N	t_{PLH} , t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	2.0	8.5	2.0	6.5	2.0	5.2	2.0	4.5	ns
Output Enable Time OE to \bar{O}_N	t_{PZH} , t_{PZL}		1.5	10.0	1.5	6.5	1.5	5.5	1.5	5.5	ns
Output Disable Time (Note 13) OE to \bar{O}_N	t_{PHZ} , t_{PLZ}		1.5	6.5	1.5	5.5	1.5	5.0	1.5	5.0	ns
Setup Time HIGH or LOW, D_N to CP	t_{SU}		2.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D_N to CP	t_H		1.5	-	1.5	-	1.5	-	1.0	-	ns
CP Pulse Width (Note 13) HIGH or LOW	t_W		7.0	-	5.0	-	5.0	-	3.0	-	ns

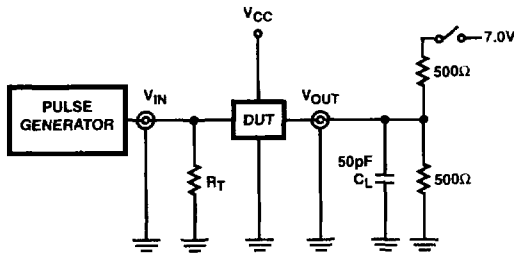
NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at $V_{CC} = 5.0V$, $25^\circ C$ ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
 $I_{CC} =$ Quiescent Current
 $\Delta I_{CC} =$ Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)
 $D_H =$ Duty Cycle for TTL Inputs High
 $N_T =$ Number of TTL Inputs at D_H
 $I_{CCD} =$ Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 $f_{CP} =$ Clock Frequency for Register Devices (Zero for Non-Register Devices)
 $f_I =$ Input Frequency
 $N_I =$ Number of Inputs at f_I
 All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

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**OCTAL 5V FCT
5V FCT 25Ω**

Test Circuits and Waveforms



SWITCH POSITION	
TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
 R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_f, t_r \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

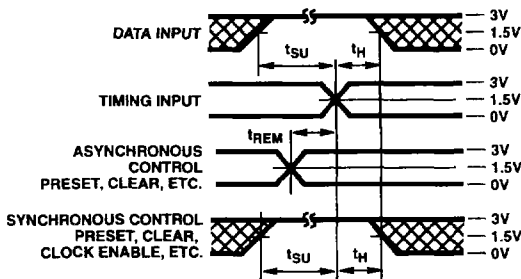


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

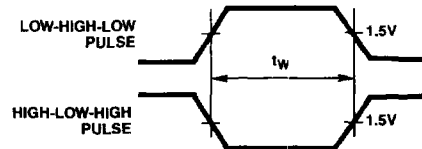


FIGURE 3. PULSE WIDTH

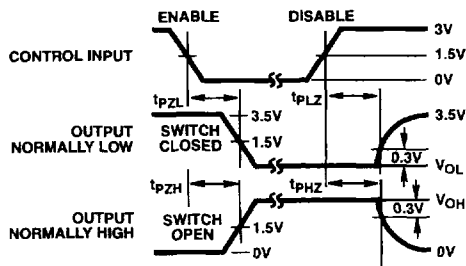


FIGURE 4. ENABLE AND DISABLE TIMING

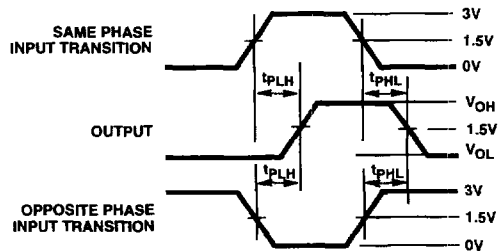


FIGURE 5. PROPAGATION DELAY