

# Component Analog TV Sync Separator

## General Description

The MAX9568 video sync separator extracts sync timing information from standard-definition (SDTV), extended-definition (EDTV), and high-definition (HDTV) component video signals. This device is designed for reliable operation in the presence of copy protection schemes such as MACROVISION®.

The MAX9568 is a stand-alone device and requires no external components for timing or biasing. High-impedance video inputs prevent loading of the input signal and eliminate the need for buffering.

The MAX9568 is available in a 16-pin QSOP package. The device is specified over the -40°C to +85°C temperature range.

## Applications

|                  |                 |
|------------------|-----------------|
| Video Digitizers | LCD Panels      |
| Instrumentation  | Frame Grabbers  |
| PDP Television   | Video Recorders |

## Features

- ◆ Stand-Alone Operation—No Timing Element Required
- ◆ Covers All Major Standards: SDTV, EDTV, and HDTV
- ◆ Identification of Input Standard
- ◆ Loss of Video Signal Detection
- ◆ Coast and Clamp Pulse Outputs
- ◆ High-Impedance Bridging Video Input
- ◆ No Distortion to Video Signal
- ◆ Low Quiescent Current (< 10mA)
- ◆ 2.7V to 5.5V Single Supply

## Ordering Information

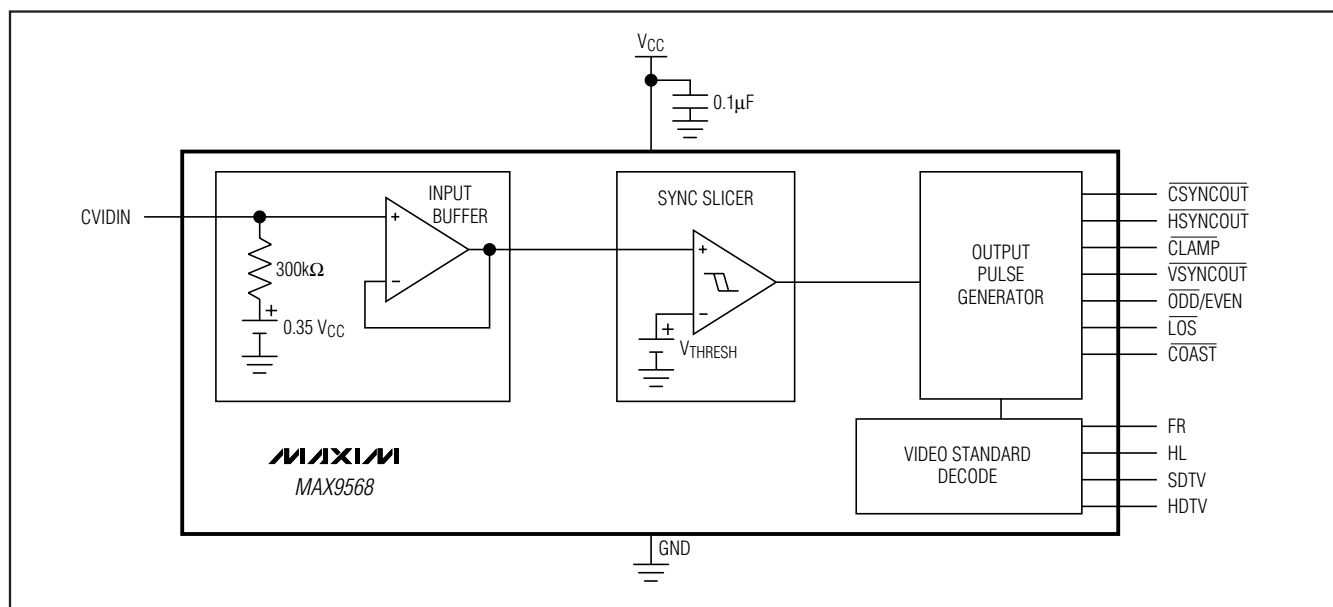
| PART         | PIN-PACKAGE | TOP MARK |
|--------------|-------------|----------|
| MAX9568EEE+T | 16 QSOP     | —        |

**Note:** All devices are specified over the -40°C to +85°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.  
T = Tape and reel.

MACROVISION is a registered trademark of Macrovision Corp.

## Functional Diagram



# Component Analog TV Sync Separator

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ( $V_{CC}$  to GND) .....-0.3V to +6V  
 All Other Pins to GND .....-0.3V to ( $V_{CC} + 0.3V$ )  
 Continuous Power Dissipation ( $T_A = +70^\circ\text{C}$ )  
 16-Pin QSOP (derate 8.3mW/ $^\circ\text{C}$  above +70 $^\circ\text{C}$ ) .....667mW

Operating Temperature Range .....-40 $^\circ\text{C}$  to +85 $^\circ\text{C}$   
 Junction Temperature .....+150 $^\circ\text{C}$   
 Storage Temperature Range .....-65 $^\circ\text{C}$  to +150 $^\circ\text{C}$   
 Lead Temperature (soldering, 10s) .....+300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{CC} = +5V$ ,  $V_{GND} = 0V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $T_A = +25^\circ\text{C}$ .) (Note 1)

| PARAMETER                            | SYMBOL           | CONDITIONS   | MIN             | TYP | MAX             | UNITS      |
|--------------------------------------|------------------|--|-----------------|-----|-----------------|------------|
| <b>DC ELECTRICAL CHARACTERISTICS</b> |                  |  |                 |     |                 |            |
| Supply Voltage Range                 | $V_{CC}$         | Inferred from horizontal pulse delay   | 2.7             |     | 5.5             | V          |
| Supply Current                       | $I_{CC}$         | With 720p video standard input   |                 | 8.5 | 13.5            | mA         |
| Input-Voltage Range (Note 2)         | $V_{IN}$         | Peak-to-peak video amplitude   | 0.5             |     | 2.0             | V          |
|                                      |                  | Absolute range   | 0.2             |     | $V_{CC} - 0.2$  |            |
| Slice Level                          | $V_{SLICE\_BI}$  | Bilevel syncs  | 60              | 95  | 130             | mV         |
|                                      | $V_{SLICE\_TRI}$ | Trilevel syncs   | 110             | 145 | 180             |            |
| Input Resistance                     | $R_{IN}$         |  |                 | 300 |                 | k $\Omega$ |
| Input DC Bias Voltage                | $V_B$            |  | 0.31 x $V_{CC}$ |     | 0.39 x $V_{CC}$ | V          |
| <b>DIGITAL LOGIC OUTPUTS</b>         |                  |  |                 |     |                 |            |
| Output-Voltage High                  | $V_{OH}$         | $I_{OUT} = 1.6\text{mA}$   | $V_{CC} = 5V$   | 4.6 |                 | V          |
|                                      |                  |  | $V_{CC} = 2.7V$ | 2.1 |                 |            |
| Output-Voltage Low                   | $V_{OL}$         | $I_{OUT} = 1.6\text{mA}$   | $V_{CC} = 5V$   |     | 0.4             | V          |
|                                      |                  |  | $V_{CC} = 2.7V$ |     | 0.5             |            |
| <b>AC ELECTRICAL CHARACTERISTICS</b> |                  |  |                 |     |                 |            |
| Input Capacitance                    | $C_{IP}$         |  |                 | 8   |                 | pF         |
| Jitter                               | $t_{JITTER}$     | $\overline{HSYNCOUT}$ output jitter with respect to sync input for 720p video signal |                 | 500 |                 | ps         |
| Output Logic Rise and Fall Times     | $t_R, t_F$       | $C_L = 15\text{pF}$  |                 | 5   |                 | ns         |

# Component Analog TV Sync Separator

MAX9568

## TIMING CHARACTERISTICS

(V<sub>CC</sub> = +5V, V<sub>GND</sub> = 0V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>. Typical values are at T<sub>A</sub> = +25°C) (Note 1)

| PARAMETER                                 | SYMBOL           | CONDITIONS     | MIN | TYP     | MAX | UNITS |
|---|------------------|----------------|-----|---------|-----|-------|
| <b>525i (Figures 1a and 2a)</b>           |                  |                |     |         |     |       |
| Horizontal Pulse Delay                    | t <sub>HP</sub>  |                |     | 20      |     | ns    |
| Horizontal Pulse Width                    | t <sub>HPW</sub> |                |     | 4.8     |     | μs    |
| Clamp Pulse Delay                         | t <sub>CP</sub>  |                |     | 570     |     | ns    |
| Clamp Pulse Width                         | t <sub>CPW</sub> |                |     | 3.7     |     | μs    |
| Composite Sync Output Leading Edge Delay  | t <sub>LE</sub>  |                |     | 15      |     | ns    |
| Composite Sync Output Trailing Edge Delay | t <sub>TE</sub>  |                |     | 15      |     | ns    |
| Vertical Pulse Delay                      | t <sub>VP</sub>  |                |     | 20      |     | ns    |
| Vertical Pulse Width                      | t <sub>VPW</sub> | Odd/even field |     | 190/122 |     | ns    |
| <b>625i (Figures 1b and 2a)</b>           |                  |                |     |         |     |       |
| Horizontal Pulse Delay                    | t <sub>HP</sub>  |                |     | 20      |     | ns    |
| Horizontal Pulse Width                    | t <sub>HPW</sub> |                |     | 4.8     |     | μs    |
| Clamp Pulse Delay                         | t <sub>CP</sub>  |                |     | 570     |     | ns    |
| Clamp Pulse Width                         | t <sub>CPW</sub> |                |     | 3.7     |     | μs    |
| Composite Sync Output Leading Edge Delay  | t <sub>LE</sub>  |                |     | 15      |     | ns    |
| Composite Sync Output Trailing Edge Delay | t <sub>TE</sub>  |                |     | 15      |     | ns    |
| Vertical Pulse Delay                      | t <sub>VP</sub>  |                |     | 20      |     | ns    |
| Vertical Pulse Width                      | t <sub>VPW</sub> |                |     | 160/192 |     | ns    |
| <b>525p/480p (Figures 1c and 2a)</b>      |                  |                |     |         |     |       |
| Horizontal Pulse Delay                    | t <sub>HP</sub>  |                |     | 20      |     | ns    |
| Horizontal Pulse Width                    | t <sub>HPW</sub> |                |     | 2.4     |     | μs    |
| Clamp Pulse Delay                         | t <sub>CP</sub>  |                |     | 290     |     | ns    |
| Clamp Pulse Width                         | t <sub>CPW</sub> |                |     | 1.6     |     | μs    |
| Composite Sync Output Leading Edge Delay  | t <sub>LE</sub>  |                |     | 15      |     | ns    |
| Composite Sync Output Trailing Edge Delay | t <sub>TE</sub>  |                |     | 15      |     | ns    |
| Vertical Pulse Delay                      | t <sub>VP</sub>  |                |     | 20      |     | ns    |
| Vertical Pulse Width                      | t <sub>VPW</sub> |                |     | 190     |     | ns    |
| <b>625p/576p (Figures 1d and 2a)</b>      |                  |                |     |         |     |       |
| Horizontal Pulse Delay                    | t <sub>HP</sub>  |                |     | 20      |     | ns    |
| Horizontal Pulse Width                    | t <sub>HPW</sub> |                |     | 2.4     |     | μs    |
| Clamp Pulse Delay                         | t <sub>CP</sub>  |                |     | 290     |     | ns    |

# Component Analog TV Sync Separator

## TIMING CHARACTERISTICS (continued)

( $V_{CC} = +5V$ ,  $V_{GND} = 0V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ . Typical values are at  $T_A = +25^\circ C$ ) (Note 1)

| PARAMETER                                 | SYMBOL    | CONDITIONS | MIN | TYP     | MAX | UNITS   |
|---|-----------|------------|-----|---------|-----|---------|
| Clamp Pulse Width                         | $t_{CPW}$ |            |     | 1.6     |     | $\mu s$ |
| Composite Sync Output Leading Edge Delay  | $t_{LE}$  |            |     | 15      |     | ns      |
| Composite Sync Output Trailing Edge Delay | $t_{TE}$  |            |     | 15      |     | ns      |
| Vertical Pulse Delay                      | $t_{VP}$  |            |     | 20      |     | ns      |
| Vertical Pulse Width                      | $t_{VPW}$ |            |     | 192     |     | ns      |
| <b>720p (Figures 1e and 2b)</b>           |           |            |     |         |     |         |
| Horizontal Pulse Delay                    | $t_{HP}$  |            |     | 20      |     | ns      |
| Horizontal Pulse Width                    | $t_{HPW}$ |            |     | 540     |     | $\mu s$ |
| Clamp Pulse Delay                         | $t_{CP}$  |            |     | 1.0     |     | ns      |
| Clamp Pulse Width                         | $t_{CPW}$ |            |     | 1.25    |     | $\mu s$ |
| Composite Sync Output Leading Edge Delay  | $t_{LE}$  |            |     | 15      |     | ns      |
| Composite Sync Output Trailing Edge Delay | $t_{TE}$  |            |     | 15      |     | ns      |
| Vertical Pulse Delay                      | $t_{VP}$  |            |     | 25      |     | ns      |
| Vertical Pulse Width                      | $t_{VPW}$ |            |     | 110     |     | ns      |
| <b>1080i (Figures 1f and 2b)</b>          |           |            |     |         |     |         |
| Horizontal Pulse Delay                    | $t_{HP}$  |            |     | 20      |     | ns      |
| Horizontal Pulse Width                    | $t_{HPW}$ |            |     | 585     |     | $\mu s$ |
| Clamp Pulse Delay                         | $t_{CP}$  |            |     | 1.1     |     | ns      |
| Clamp Pulse Width                         | $t_{CPW}$ |            |     | 1.2     |     | $\mu s$ |
| Composite Sync Output Leading Edge Delay  | $t_{LE}$  |            |     | 15      |     | ns      |
| Composite Sync Output Trailing Edge Delay | $t_{TE}$  |            |     | 15      |     | ns      |
| Vertical Pulse Delay                      | $t_{VP}$  |            |     | 25      |     | ns      |
| Vertical Pulse Width                      | $t_{VPW}$ |            |     | 160/192 |     | ns      |

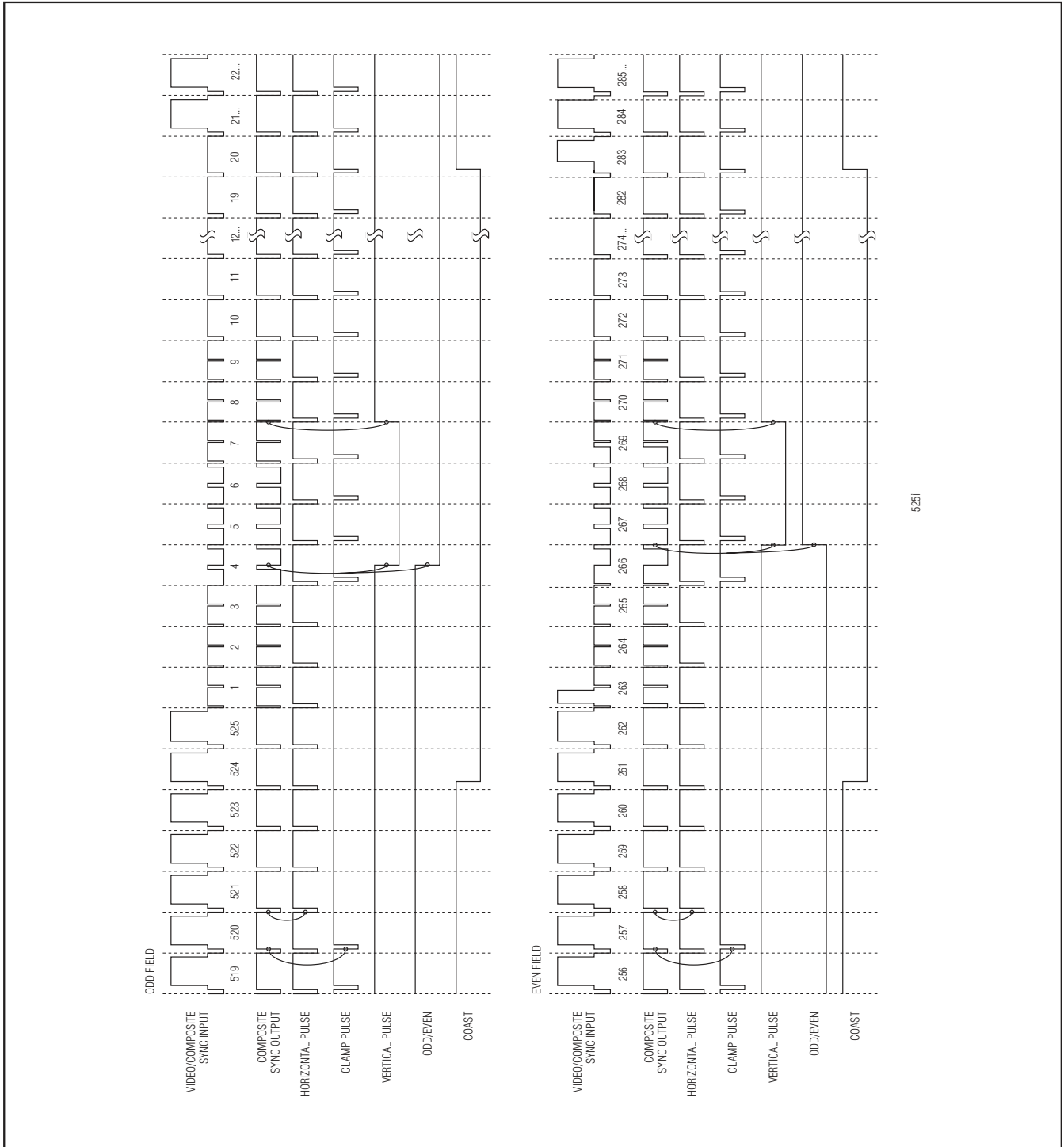
**Note 1:** All devices are production tested at  $T_A = +25^\circ C$ . Specifications over temperature are guaranteed by design.

**Note 2:** Input voltage range is guaranteed by the horizontal pulse delay.

# Component Analog TV Sync Separator

## Timing Diagrams

**MAX9568**

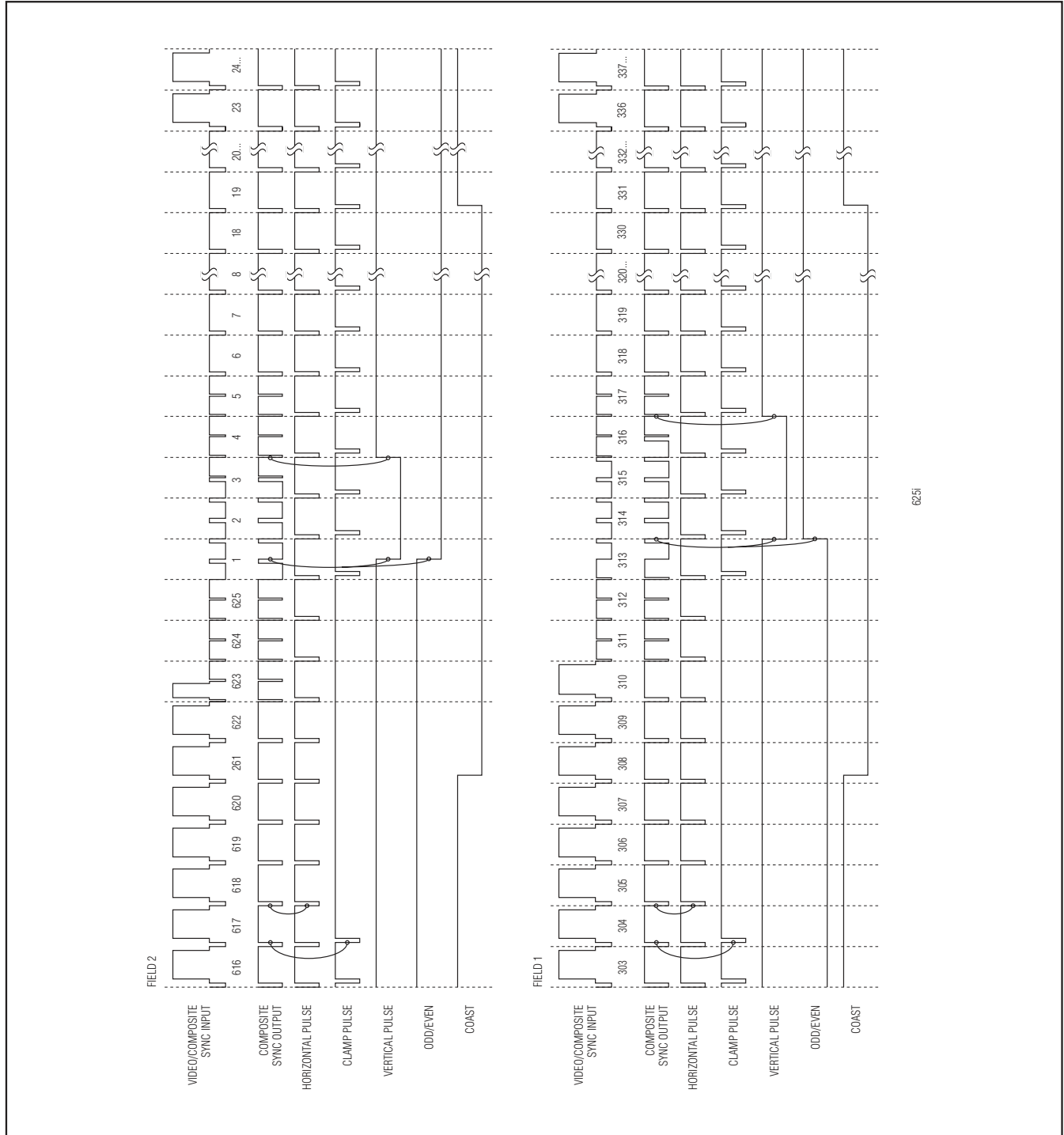


525i

Figure 1a. Standard Interlaced 525i (NTSC) Component Video

# Component Analog TV Sync Separator

## Timing Diagrams (continued)



625i

Figure 1b. Standard Interlaced 625i (PAL) Component Video

# Component Analog TV Sync Separator

## Timing Diagrams (continued)

**MAX9568**

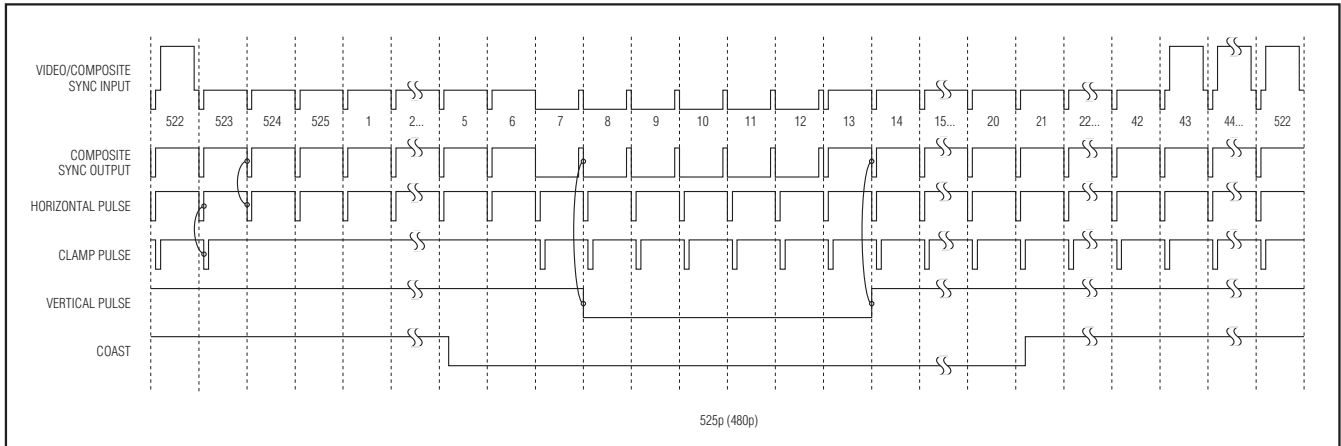


Figure 1c. Extended Standard Progressive 525p (480p) Component Video

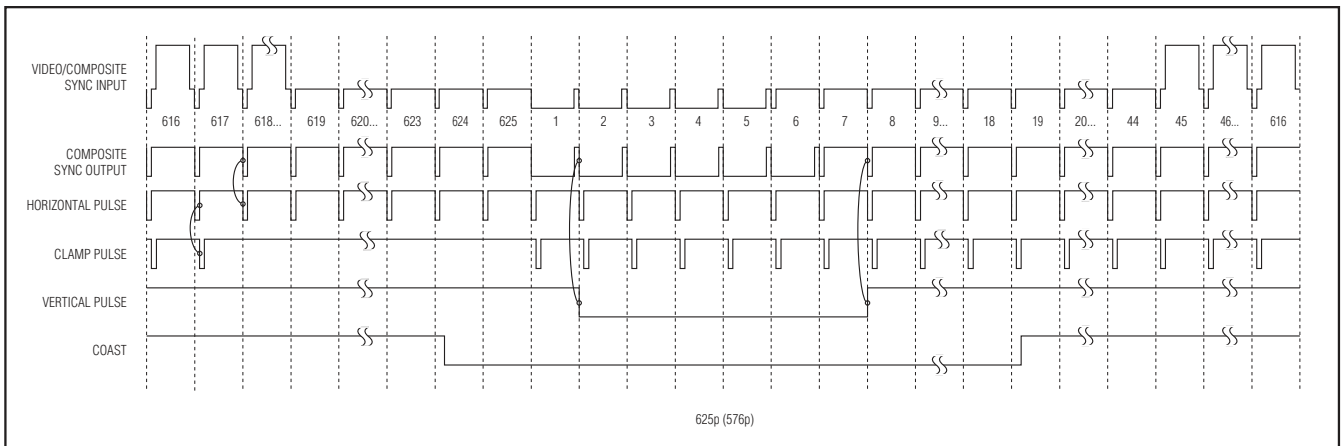


Figure 1d. Extended Standard Progressive 625p (576p) Component Video

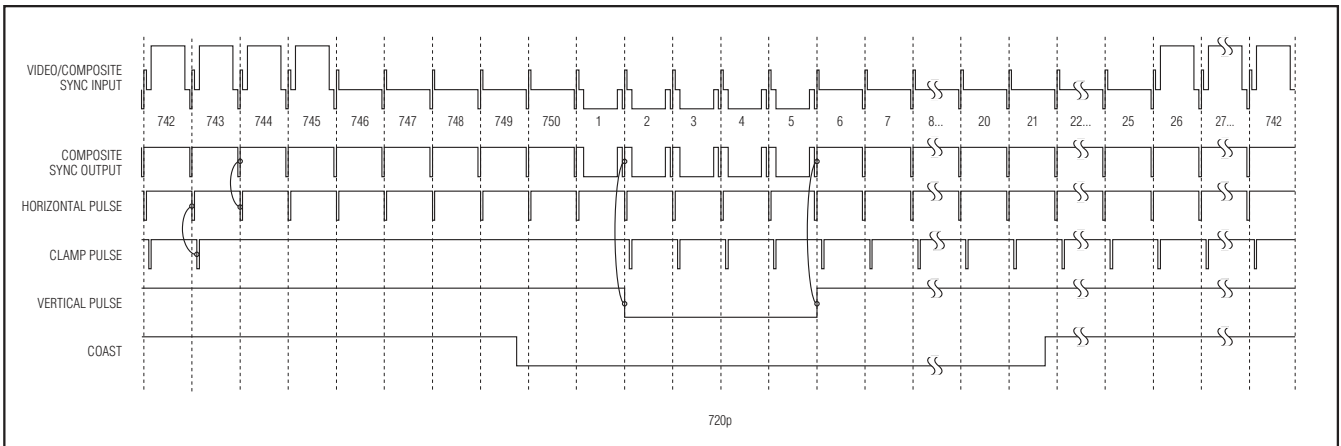


Figure 1e. High-Definition Progressive 720p Composite Video

# Component Analog TV Sync Separator

## Timing Diagrams (continued)

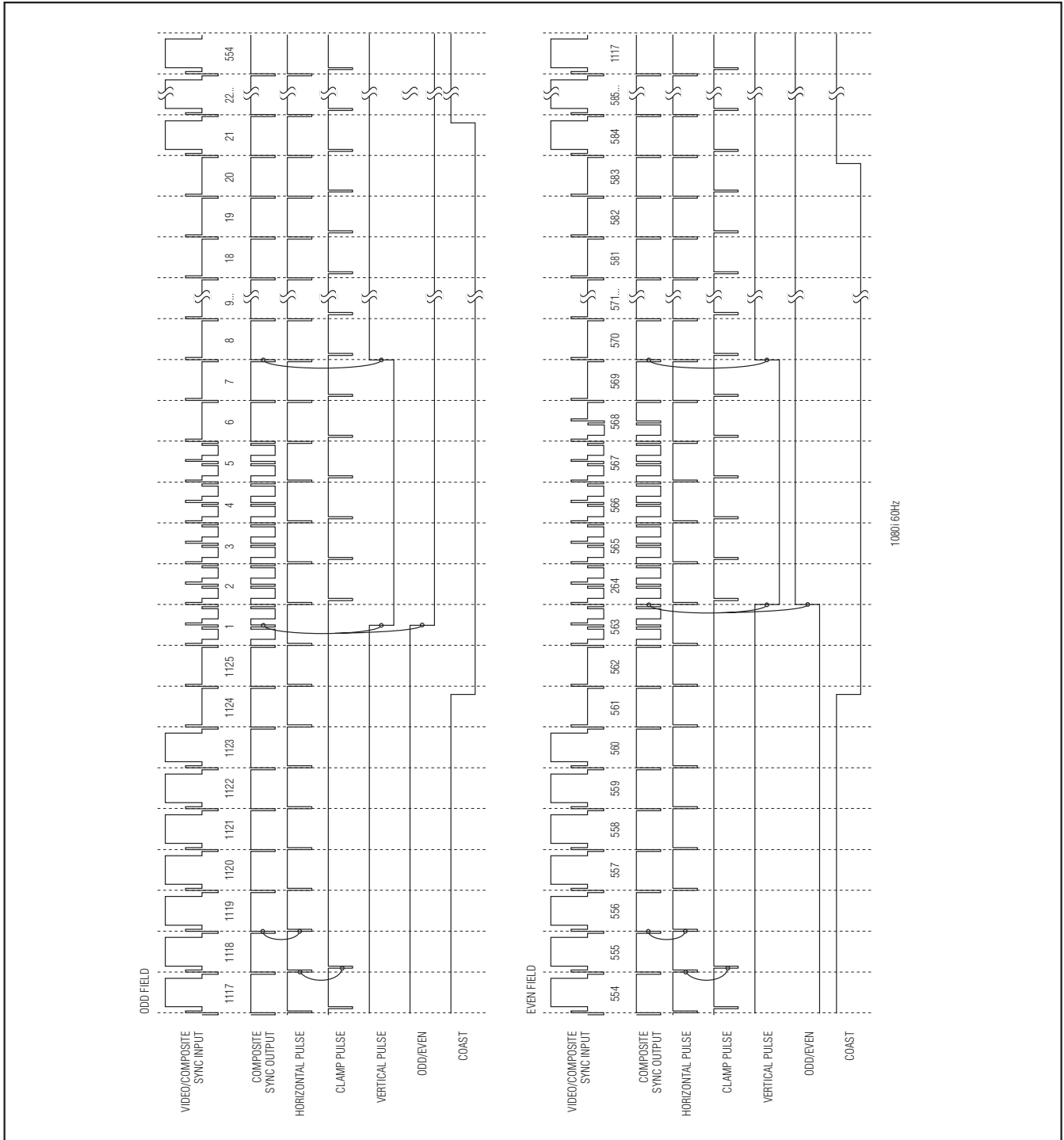


Figure 1f. High-Definition Progressive 1080i Composite Video



# Component Analog TV Sync Separator

MAX9568

## Timing Diagrams (continued)

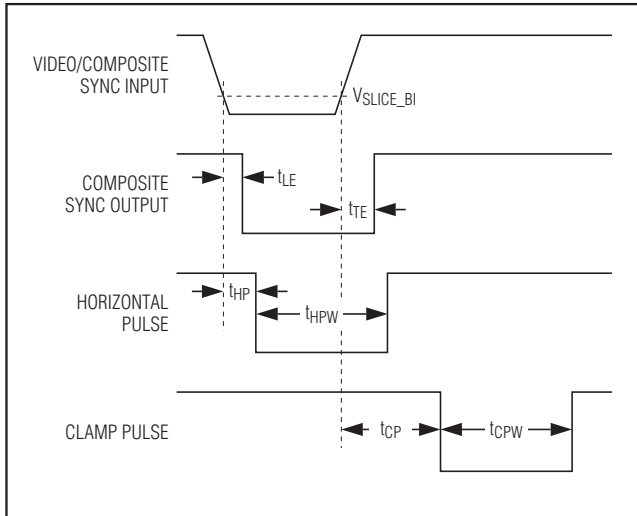


Figure2a. 525/625i 525/625p (480p/576p) Horizontal Timing

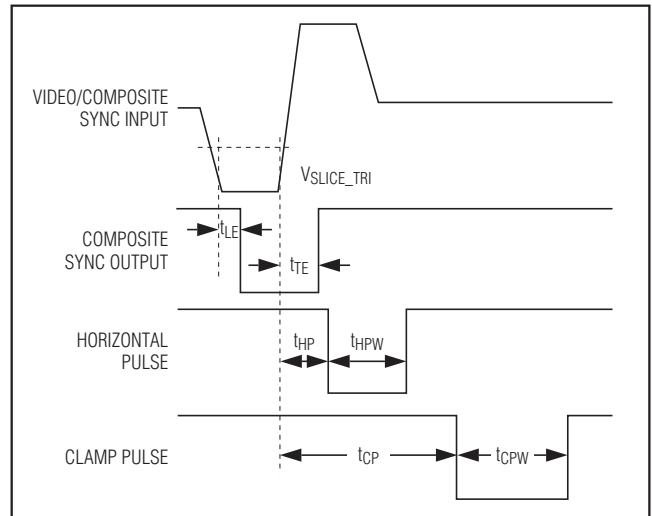
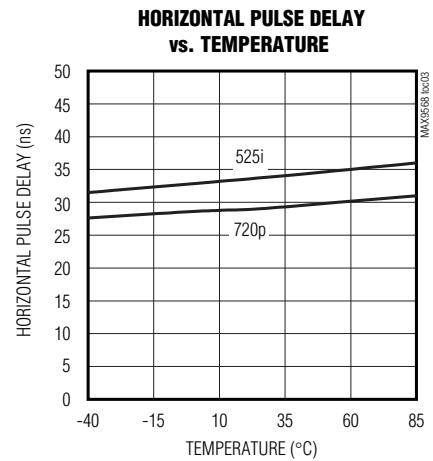
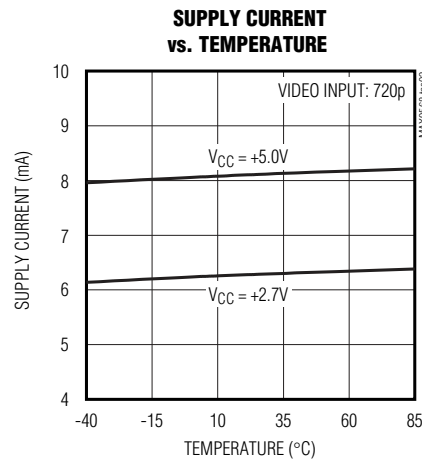
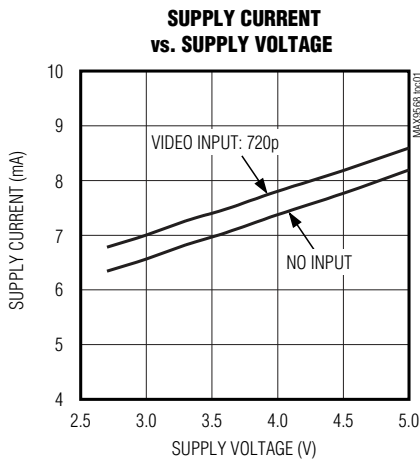


Figure2b. 720p/1080i Horizontal Timing

## Typical Operating Characteristics

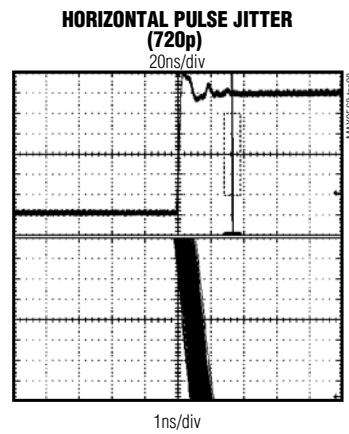
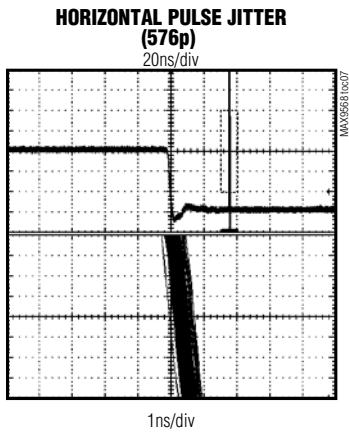
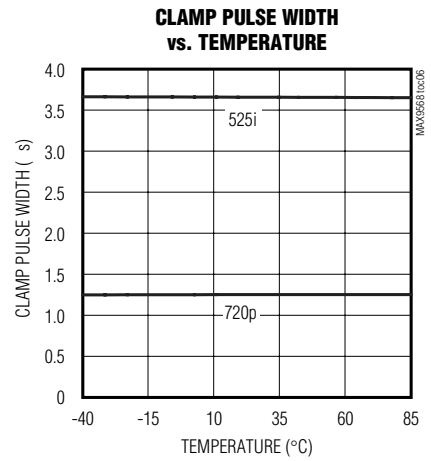
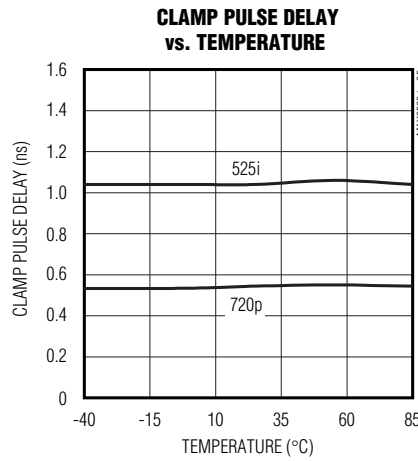
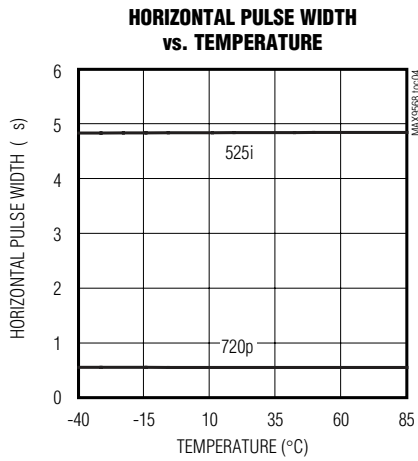
( $V_{CC} = +5V$ ,  $V_{GND} = 0V$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



# Component Analog TV Sync Separator

## Typical Operating Characteristics (continued)

(VCC = +5V, VGND = 0V, TA = +25°C, unless otherwise noted.)



# Component Analog TV Sync Separator

## Pin Description

**MAX9568**

| PIN  | NAME                         | FUNCTION   |
|------|------------------------------|--|
| 1    | $\overline{\text{CSYNCOUT}}$ | Composite Sync Output. Active low.   |
| 2    | CVIDIN                       | Component Video Input  |
| 3    | $\overline{\text{VSYNCOUT}}$ | Vertical Timing Pulse Output. Active low.  |
| 4    | $\overline{\text{COAST}}$    | Coast Output. Active low.  |
| 5, 8 | GND                          | Ground   |
| 6    | FR                           | Frame Rate Output. FRAME high indicates 60Hz and low indicates 50Hz. See Table 1.  |
| 7    | HL                           | Standard Output 3. HL high indicates 625i, 625p (576p), and 1080i standards. HL low indicates 525i, 525p (480p), and 720p standards. See Table 1.                                    |
| 9    | N.C.                         | No Connection. Not internally connected.   |
| 10   | SDTV                         | Standard Output 1. SDTV high indicates standard-definition television. SDTV low indicates extended definition or high-definition television. See Table 1.                            |
| 11   | HDTV                         | Standard Output 2. HDTV high indicates high-definition television. HDTV low indicates standard-definition or extended definition television. See Table 1.                            |
| 12   | $\overline{\text{CLAMP}}$    | Clamp Pulse Output. Active low during the back porch portion of component video.   |
| 13   | $\overline{\text{LOS}}$      | Loss-of-Sync Output. Indicates the presence of a video input signal. Active low.   |
| 14   | $\overline{\text{ODD/EVEN}}$ | Odd and Even Line Field Output. Indicates odd or even field for interlaced video standards. $\overline{\text{ODD/EVEN}}$ is logic-high for even fields and logic-low for odd fields. |
| 15   | $\overline{\text{HSYNCOUT}}$ | Horizontal Timing Pulse Output. Active low.  |
| 16   | V <sub>CC</sub>              | Positive Supply. Bypass V <sub>CC</sub> to GND with a 0.1μF capacitor.   |

**Table 1. Video Standard Output Decoding**

| TV STANDARD | CLASSIFICATION | OUTPUT PINS |       |       |      |
|-------------|----------------|-------------|-------|-------|------|
|             |                | FR          | SDTV* | HDTV* | HL   |
| 525i        | SDTV           | High        | High  | Low   | Low  |
| 625i        | SDTV           | Low         | High  | Low   | High |
| 525p/480p   | EDTV           | High        | Low   | Low   | Low  |
| 625p/576p   | EDTV           | Low         | Low   | Low   | High |
| 720p        | HDTV           | High        | Low   | High  | Low  |
| 1080i/60    | HDTV           | High        | Low   | High  | High |
| 1080i/50    | HDTV           | Low         | Low   | High  | High |

# Component Analog TV Sync Separator

## Detailed Description

The MAX9568 sync separator extracts sync timing information from SDTV, EDTV, and HDTV component video signals. The MAX9568 is a stand-alone device, and requires no external components to set timing or bias voltage. The MAX9568 has high input impedance, eliminating the need for a low-impedance video source at the input.

The MAX9568 provides composite sync, vertical sync, and horizontal sync outputs. The MAX9568 provides automatic SDTV, EDTV, and HDTV detection logic outputs to indicate the type of TV standard being processed. The MAX9568 provides a back-porch clamp output signal.

The MAX9568 provides a loss-of-sync output to indicate a loss-of-video input signal. The MAX9568 provides an output to indicate odd and even fields. The MAX9568 provides a vertical interval coast output which allows control of a PLL oscillator when coasting through the vertical interval.

## Component Video Input (CVIDIN)

CVIDIN provides a high input impedance to the analog video source. This eliminates the requirement for a low-impedance video source. Following the input buffer is the sync slicer block. This block establishes a DC level for the incoming video signal. The sync information is stripped by using a comparator with threshold or slice level that automatically adjusts to the incoming signal. When the incoming signal has bilevel syncs, the slice is made 95mV above the sync tip. When the incoming signal has trilevel syncs, the slice is made 145mV above the sync tip. The device's wide dynamic range, 0.2V to  $V_{CC} - 0.2V$ , allows the video signal from 0.5V<sub>P-P</sub> to 2V<sub>P-P</sub> to be processed and operate in the linear range. The mentioned threshold levels are independent of the signal amplitude.

CVIDIN is biased to  $0.35 \times V_{CC}$  through a 300k $\Omega$  resistor. Use a 0.1 $\mu$ F capacitor to AC-couple at the input if the input signal is not within the input-voltage range, as shown Figure 3.

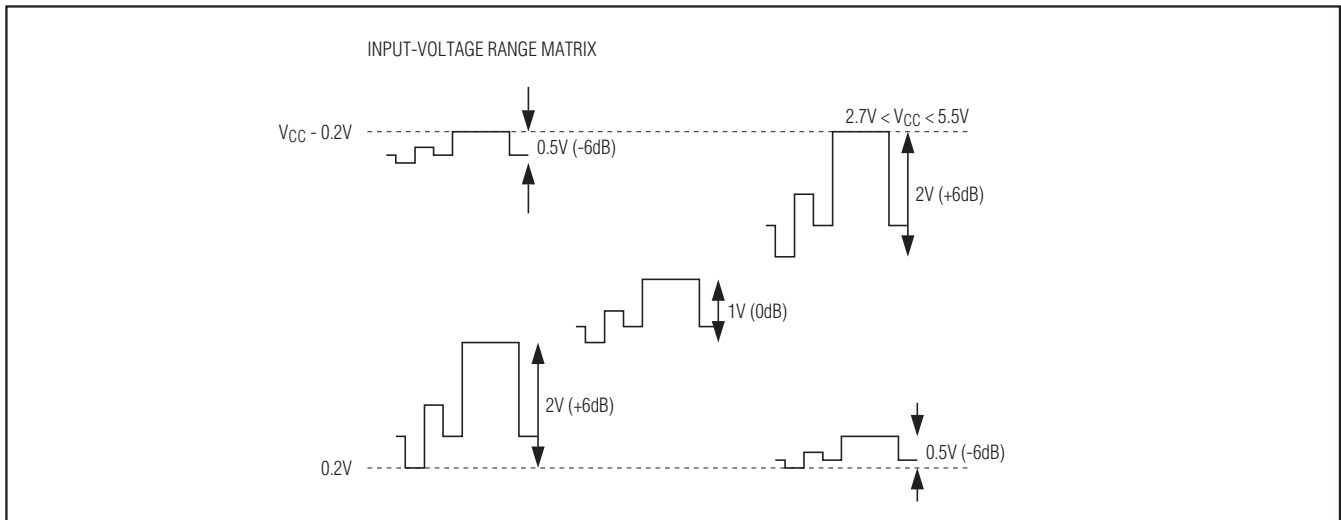


Figure 3. Input-Voltage Range Matrix

# Component Analog TV Sync Separator

## Composite Sync Output ( $\overline{\text{CSYNCOUT}}$ )

$\overline{\text{CSYNCOUT}}$  reproduces the component video input waveform with the active video removed. This output contains all the information below the component video black level.  $\overline{\text{CSYNCOUT}}$  is pulled high whenever sync is not detected at the component video input. See Figures 2a and 2b for composite sync output timing diagrams.

## Vertical Sync Output ( $\overline{\text{VSYNCOUT}}$ )

$\overline{\text{VSYNCOUT}}$  produces a pulse signal that defines the beginning of a new field in interlaced systems or frame in progressive systems. This output pulses low whenever the vertical sync pulse interval is detected. See Figure 4 for vertical sync output timing diagrams.

## Horizontal Sync Output ( $\overline{\text{HSYNCOUT}}$ )

$\overline{\text{HSYNCOUT}}$  produces a pulse signal that defines the beginning of the horizontal line. This output pulses low whenever a horizontal sync pulse is detected. For interlace standards, the horizontal pulse output rate remains constant. See Figures 2a and 2b for horizontal sync output timing diagrams.

## Standard- and High-Definition TV Detection (SDTV, HDTV, HL)

SDTV, HDTV, and HL produce logic outputs that indicate the standard of the component video signal at the input. SDTV output high indicates standard-definition television while SDTV output low indicates extended definition or high-definition television.

HDTV output high indicates high-definition television while HDTV output low indicates standard-definition or extended definition television.

HL output high indicates 625i, 625p (576p), and 1080i standards while HL output low indicates 525i, 525p (480p), and 720p standards. See Table 1.

## Loss-of-Sync Output ( $\overline{\text{LOS}}$ )

$\overline{\text{LOS}}$  produces logic output that indicates the presence of a video input signal.  $\overline{\text{LOS}}$  output high indicates that there is a sync or video signal at the input while  $\overline{\text{LOS}}$  low indicates the presence of a component video signal at CVIDIN.

## Clamp Pulse Output ( $\overline{\text{CLAMP}}$ )

$\overline{\text{CLAMP}}$  produces a pulse signal that is generally used to drive a black-level clamp circuit which restores the DC component to a video signal. This output pulses low during black-level (back porch) of each video line. See Figures 2a and 2b for clamp pulse output timing diagrams.

## Coast

The MAX9568 provides a vertical interval coast output which allows the PLL oscillator to coast through the vertical interval. This output pulses low during vertical blanking interval.

## Odd and Even Field Detection ( $\overline{\text{ODD/EVEN}}$ )

$\overline{\text{ODD/EVEN}}$  produces a square wave that identifies the present field of an interlaced video source.  $\overline{\text{ODD/EVEN}}$  output low indicates odd field while  $\overline{\text{ODD/EVEN}}$  output high indicates even field. This square wave changes coincidentally with the beginning of the vertical pulse.

## Applications Information

### Chroma Filter

If the input signal is standard-definition composite video, a simple lowpass filter is recommended in front of the input to attenuate the chroma signal, or any high-frequency noise below the black level. As shown in Figure 5, when the input is standard-definition video, SDTV is logic-high and Q1 is turned on. When Q1 is on, R1 and C2 form a 600kHz lowpass filter to attenuate high-frequency noise and improve the performance of the MAX9568. When the input is high-definition video or extended definition video, SDTV is logic-low and Q1 is turned off, disabling the RC input filter.

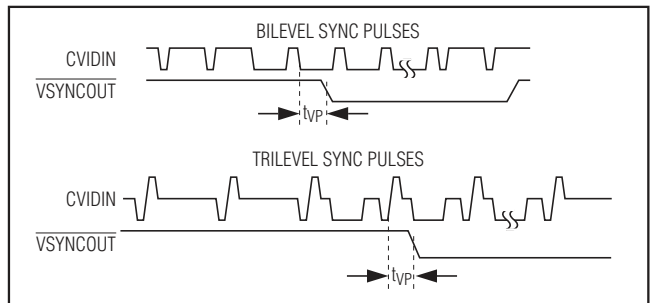


Figure 4. Vertical Sync Output Timing Diagrams

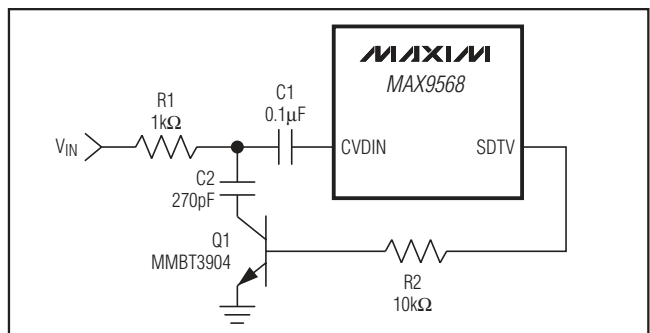


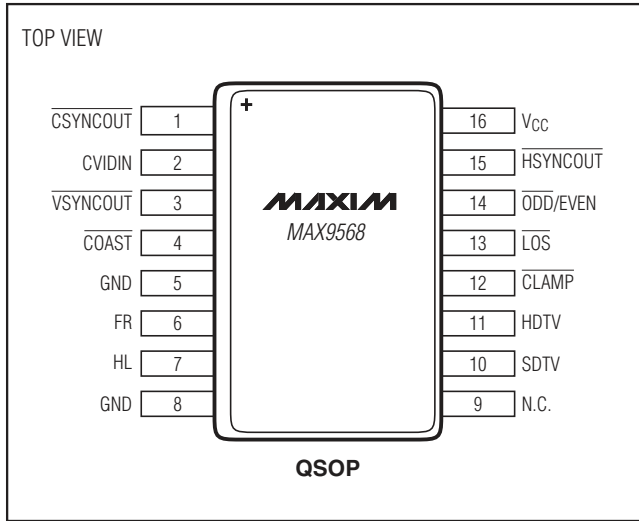
Figure 5. Chroma Filter

# Component Analog TV Sync Separator

## Pin Configuration

## Chip Information

PROCESS: BiCMOS



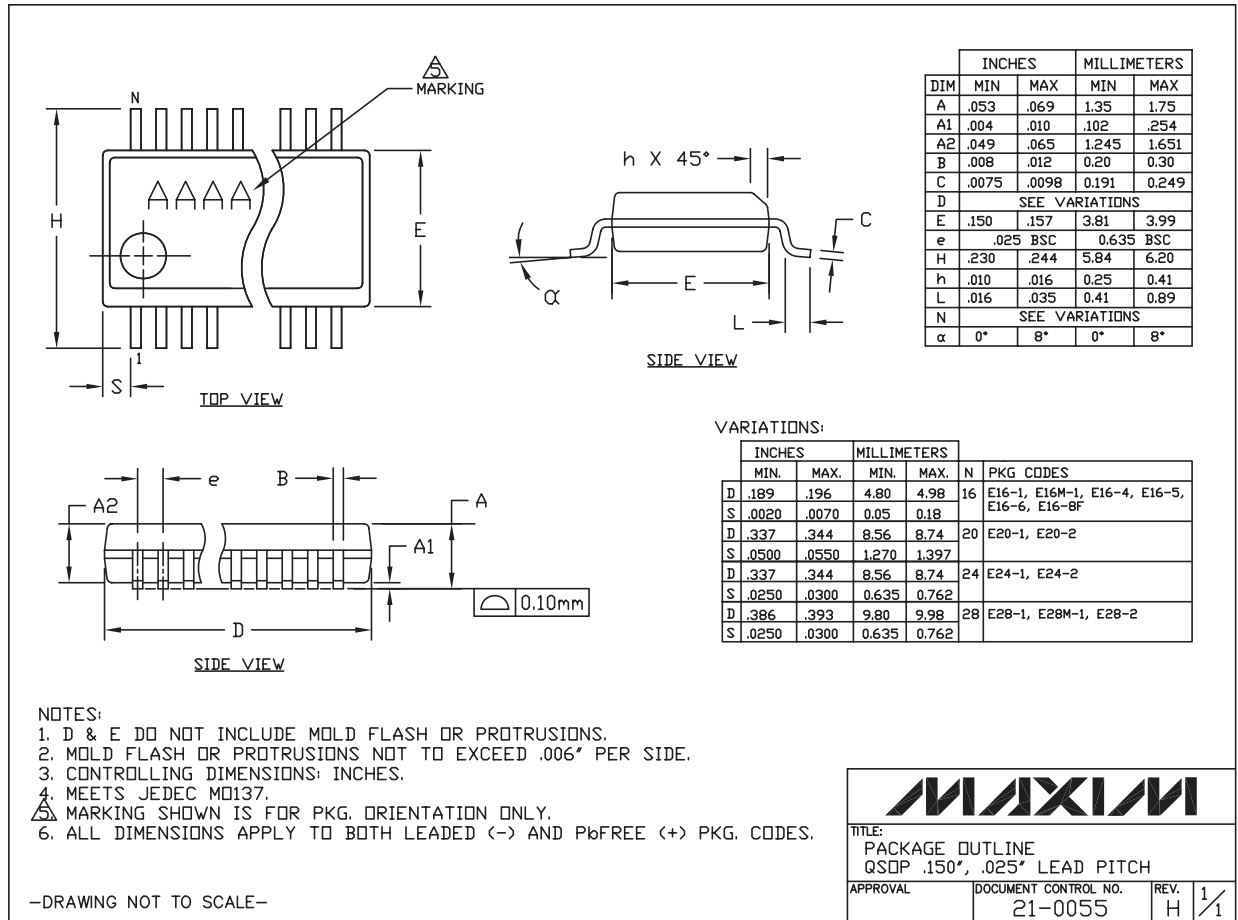
# Component Analog TV Sync Separator

## Package Information

For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

| PACKAGE TYPE | PACKAGE CODE | DOCUMENT NO.            |
|--------------|--------------|-------------------------|
| 16 QSOP      | E16-1        | <a href="#">21-0055</a> |

MAX9568



# Component Analog TV Sync Separator

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION                                 | PAGES CHANGED |
|-----------------|---------------|---|---------------|
| 0               | 5/08          | Initial release                             | —             |
| 1               | 12/08         | Removed MAX9566, MAX9567, and MAX9569 parts | 1–15          |

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

16 **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**