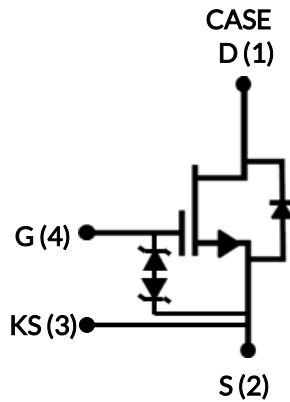


DATASHEET

UJ4SC075006K4S



750V-5.9mΩ SiC FET

Rev. B, July 2021

Description

The UJ4SC075006K4S is a 750V, 5.9mΩ G4 SiC FET. It is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-4L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- ◆ On-resistance $R_{DS(on)}$: 5.9mΩ (typ)
- ◆ Operating temperature: 175°C (max)
- ◆ Excellent reverse recovery: Q_{rr} = 440nC
- ◆ Low body diode V_{FSD} : 1.03V
- ◆ Low gate charge: Q_G = 164nC
- ◆ Threshold voltage $V_{G(th)}$: 4.7V (typ) allowing 0 to 15V drive
- ◆ Low intrinsic capacitance
- ◆ ESD protected, HBM class 2
- ◆ TO-247-4L package for faster switching, clean gate waveforms

Part Number	Package	Marking
UJ4SC075006K4S	TO-247-4L	UJ4SC075006K4S

Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-20 to +20	V
		AC (f > 1Hz)	-25 to +25	V
Continuous drain current ¹	I_D	$T_C < 125^\circ\text{C}$	120	A
Pulsed drain current ²	I_{DM}	$T_C = 25^\circ\text{C}$	588	A
Single pulsed avalanche energy ³	E_{AS}	L=15mH, $I_{AS} = 6.5\text{A}$	316	mJ
Short circuit withstand time ⁴	t_{SC}	$V_{DS} = 400\text{V}$, $T_{J(\text{START})} = 175^\circ\text{C}$	5	μs
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \leq 500\text{V}$	100	V/ns
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	714	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	$^\circ\text{C}$

1. Limited by bondwires

2. Pulse width t_p limited by $T_{J,max}$

3. Starting $T_J = 25^\circ\text{C}$

4. Short circuit current is independent of the gate voltage $V_{GS} > 12\text{V}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.16	0.21	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS}=0V, I_D=1mA$	750			V
Total drain leakage current	I_{DSS}	$V_{DS}=750V,$ $V_{GS}=0V, T_J=25^\circ\text{C}$		6	130	μA
		$V_{DS}=750V,$ $V_{GS}=0V, T_J=175^\circ\text{C}$		45		
Total gate leakage current	I_{GSS}	$V_{DS}=0V, T_J=25^\circ\text{C},$ $V_{GS}=-20V / +20V$		6	± 20	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS}=12V, I_D=80A,$ $T_J=25^\circ\text{C}$		5.9	7.4	m Ω
		$V_{GS}=12V, I_D=80A,$ $T_J=125^\circ\text{C}$		9.8		
		$V_{GS}=12V, I_D=80A,$ $T_J=175^\circ\text{C}$		12.9		
Gate threshold voltage	$V_{G(th)}$	$V_{DS}=5V, I_D=10mA$	4	4.7	6	V
Gate resistance	R_G	f=1MHz, open drain		0.8	1.5	Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current ¹	I_S	$T_C < 125^\circ\text{C}$			120	A
Diode pulse current ²	$I_{S,pulse}$	$T_C=25^\circ\text{C}$			588	A
Forward voltage	V_{FSD}	$V_{GS}=0V, I_F=50A,$ $T_J=25^\circ\text{C}$		1.03	1.16	V
		$V_{GS}=0V, I_F=50A,$ $T_J=175^\circ\text{C}$		1.06		
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=80A,$ $V_{GS}=0V, R_{G,EXT}=5\Omega$ $di/dt=2800A/\mu\text{s},$ $T_J=25^\circ\text{C}$		440		nC
Reverse recovery time	t_{rr}	$T_J=25^\circ\text{C}$		31		ns
Reverse recovery charge	Q_{rr}	$V_R=400V, I_F=80A,$ $V_{GS}=0V, R_{G,EXT}=5\Omega$ $di/dt=2800A/\mu\text{s},$ $T_J=150^\circ\text{C}$		525		nC
Reverse recovery time	t_{rr}	$T_J=150^\circ\text{C}$		37		ns

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS}=400V, V_{GS}=0V$ $f=100kHz$		8374		pF
Output capacitance	C_{oss}			362		
Reverse transfer capacitance	C_{rss}			4		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		475		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		950		pF
C_{OSS} stored energy	E_{oss}	$V_{DS}=400V, V_{GS}=0V$		38		μJ
Total gate charge	Q_G	$V_{DS}=400V, I_D=80A,$ $V_{GS} = -0V$ to 15V		164		nC
Gate-drain charge	Q_{GD}			24		
Gate-source charge	Q_{GS}			46		
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=400V, I_D=80A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1.5\Omega,$ Turn-off $R_{G,EXT}=5\Omega,$ inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega,$ RC snubber: $R_S=5\Omega$ and $C_S=680pF,$ $T_J=25^\circ C$		37		ns
Rise time	t_r			40		
Turn-off delay time	$t_{d(off)}$			110		
Fall time	t_f			13		
Turn-on energy including R_S energy	E_{ON}			514		
Turn-off energy including R_S energy	E_{OFF}		170		μJ	
Total switching energy	E_{TOTAL}		684			
Snubber R_S energy during turn-on	E_{RS_ON}		9.6			
Snubber R_S energy during turn-off	E_{RS_OFF}		50			
Turn-on delay time	$t_{d(on)}$	Notes 5 and 6, $V_{DS}=400V, I_D=80A,$ Gate Driver =0V to +15V, Turn-on $R_{G,EXT}=1.5\Omega,$ Turn-off $R_{G,EXT}=5\Omega,$ inductive Load, FWD: same device with $V_{GS} = 0V$ and $R_G = 5\Omega,$ RC snubber: $R_S=5\Omega$ and $C_S=680pF,$ $T_J=150^\circ C$		36		ns
Rise time	t_r			44		
Turn-off delay time	$t_{d(off)}$			121		
Fall time	t_f			16		
Turn-on energy including R_S energy	E_{ON}			640		
Turn-off energy including R_S energy	E_{OFF}		189		μJ	
Total switching energy	E_{TOTAL}		829			
Snubber R_S energy during turn-on	E_{RS_ON}		9			
Snubber R_S energy during turn-off	E_{RS_OFF}		51			

5. Measured with the switching test circuit in Figure 29.

6. In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.

Typical Performance Diagrams

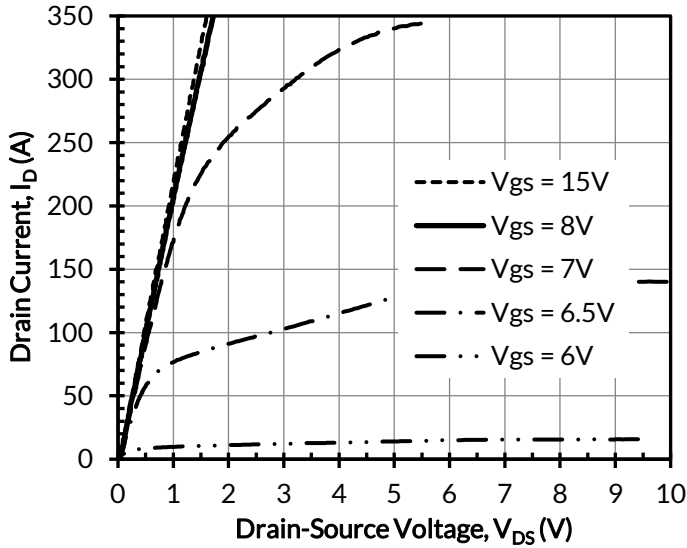


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

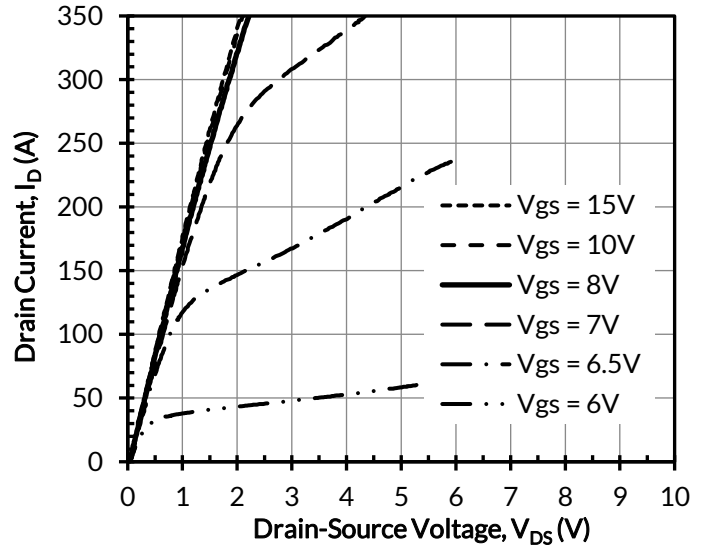


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

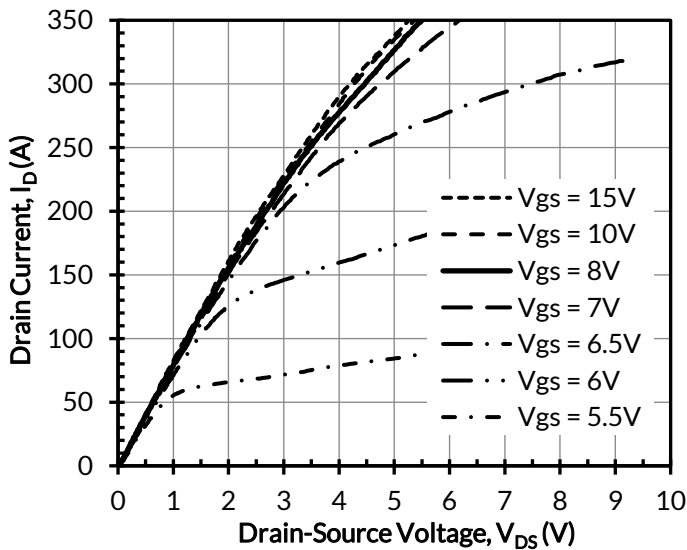


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

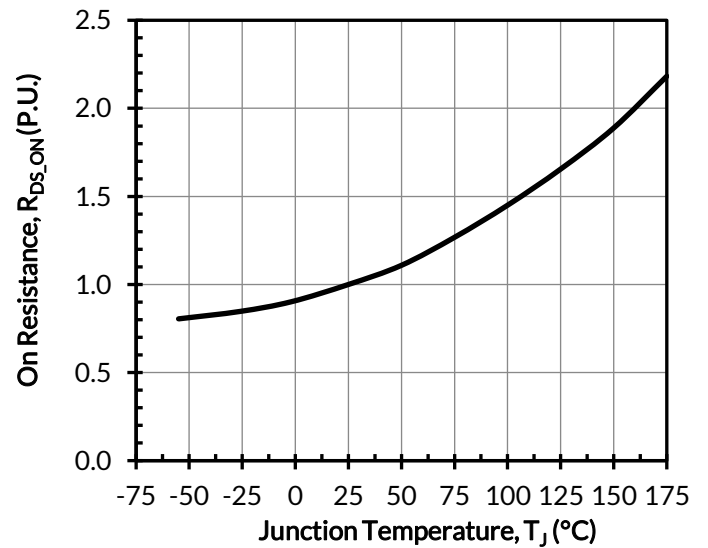


Figure 4. Normalized on-resistance vs. temperature at $V_{GS} = 12\text{V}$ and $I_D = 80\text{A}$

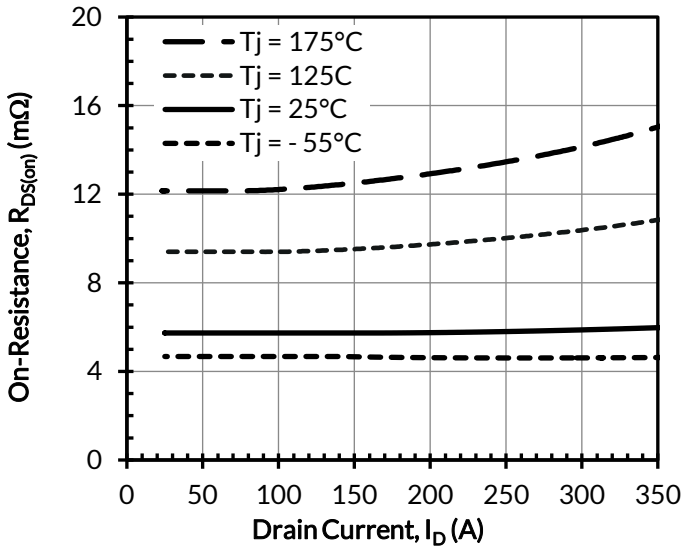


Figure 5. Typical drain-source on-resistances at $V_{GS} = 12V$

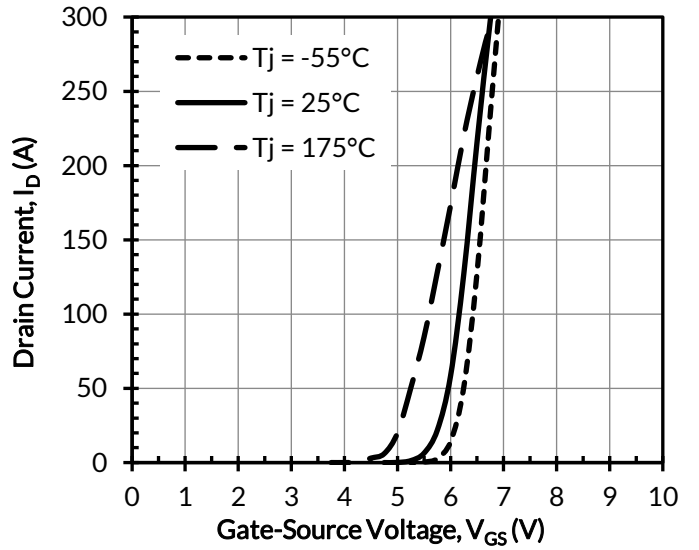


Figure 6. Typical transfer characteristics at $V_{DS} = 5V$

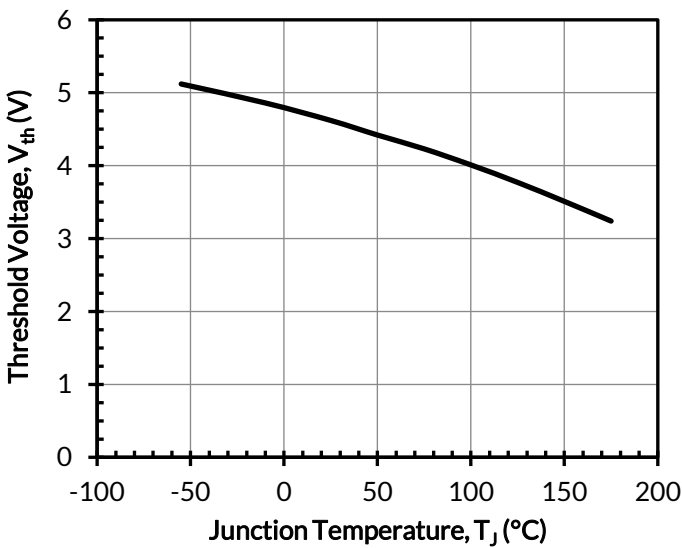


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 10mA$

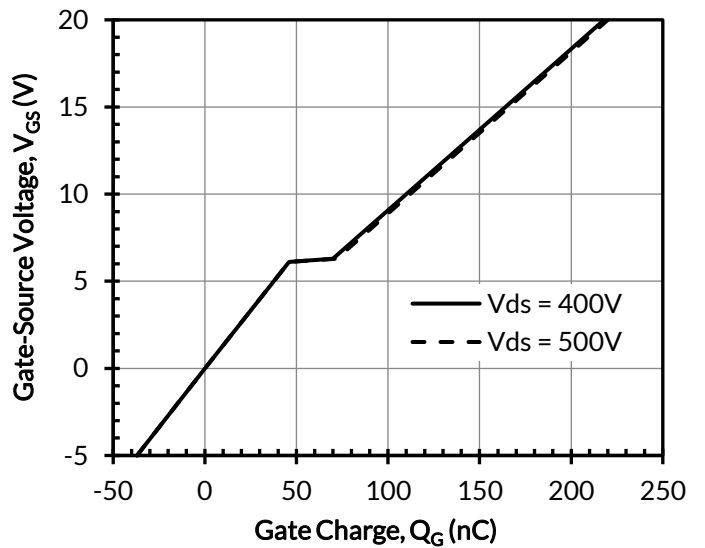


Figure 8. Typical gate charge at $I_D = 80A$

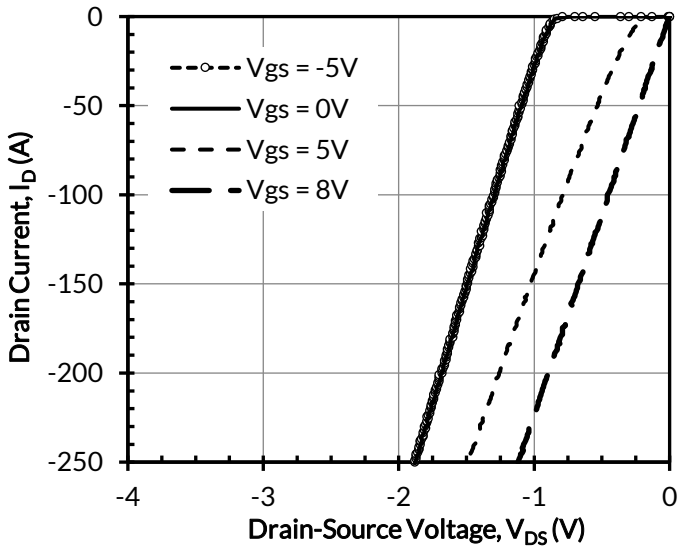


Figure 9. 3rd quadrant characteristics at $T_j = -55^\circ\text{C}$

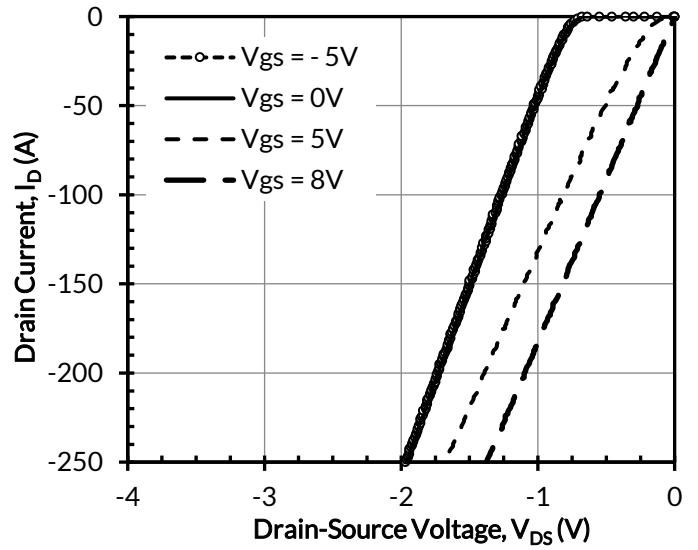


Figure 10. 3rd quadrant characteristics at $T_j = 25^\circ\text{C}$

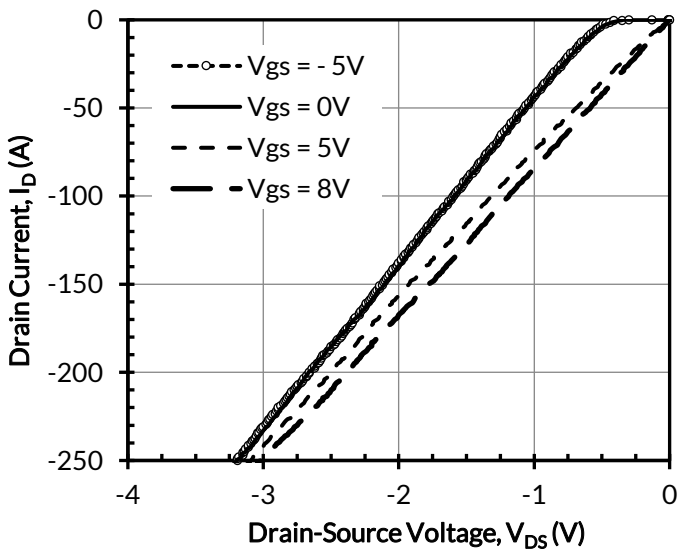


Figure 11. 3rd quadrant characteristics at $T_j = 175^\circ\text{C}$

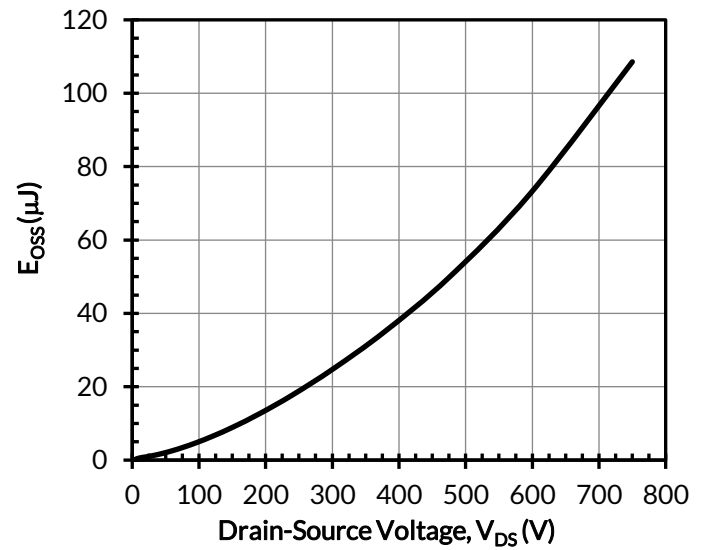


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0\text{V}$

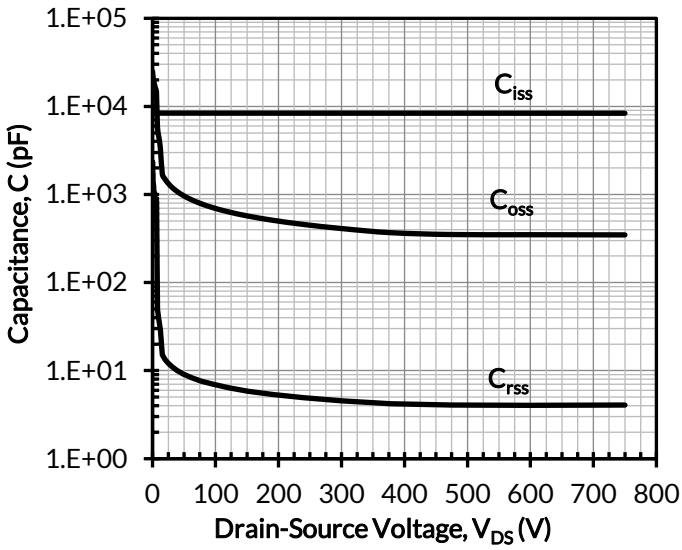


Figure 13. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = 0\text{V}$

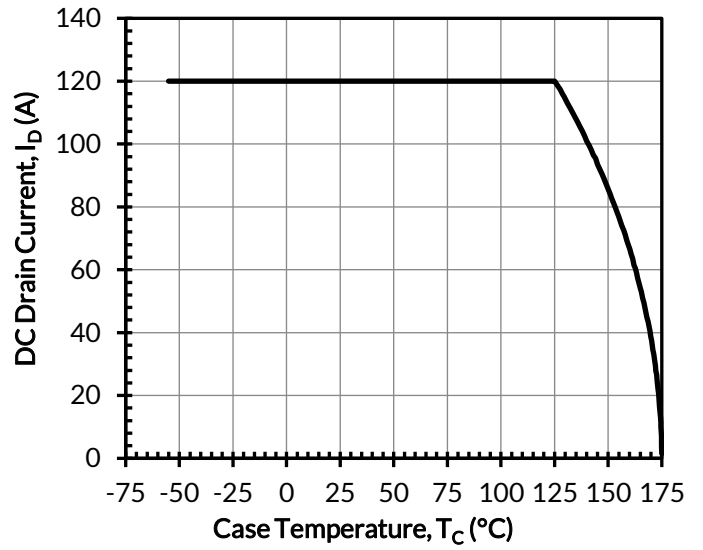


Figure 14. DC drain current derating

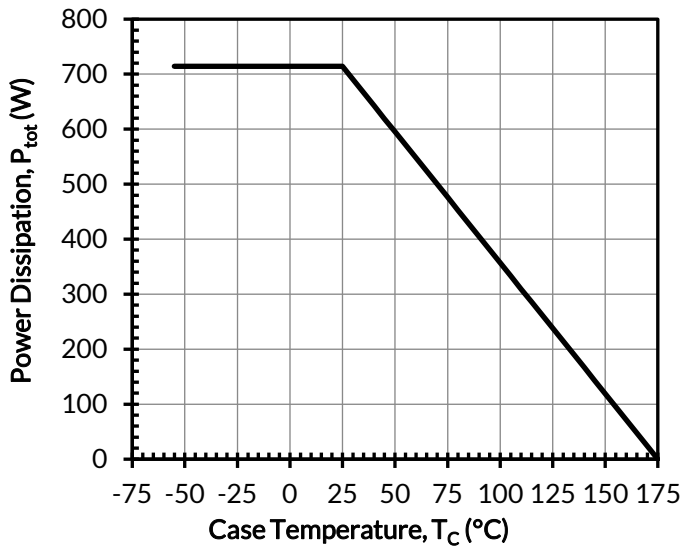


Figure 15. Total power dissipation

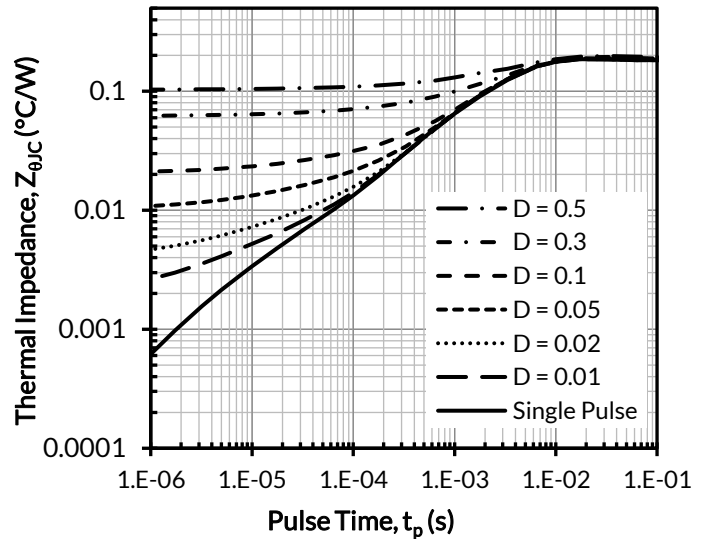


Figure 16. Maximum transient thermal impedance

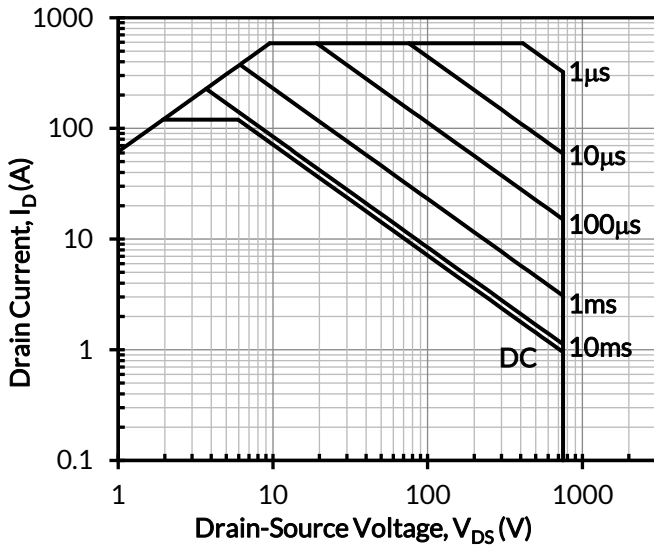


Figure 17. Safe operation area at $T_C = 25^\circ\text{C}$, $D = 0$, Parameter t_p

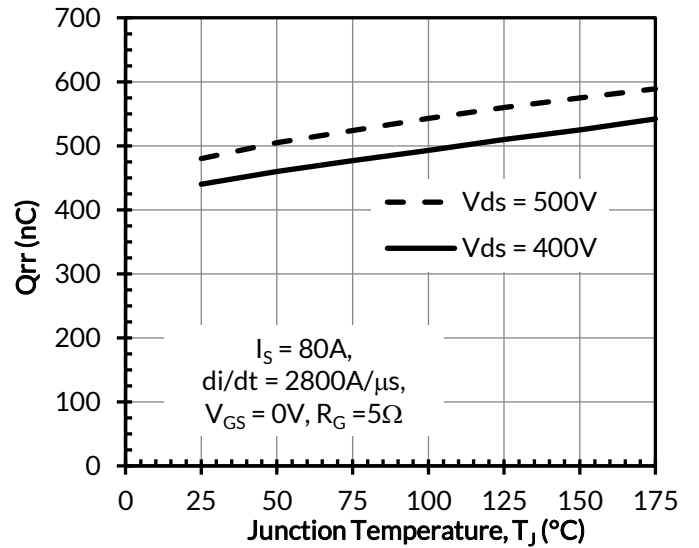


Figure 18. Reverse recovery charge Q_{rr} vs. junction temperature

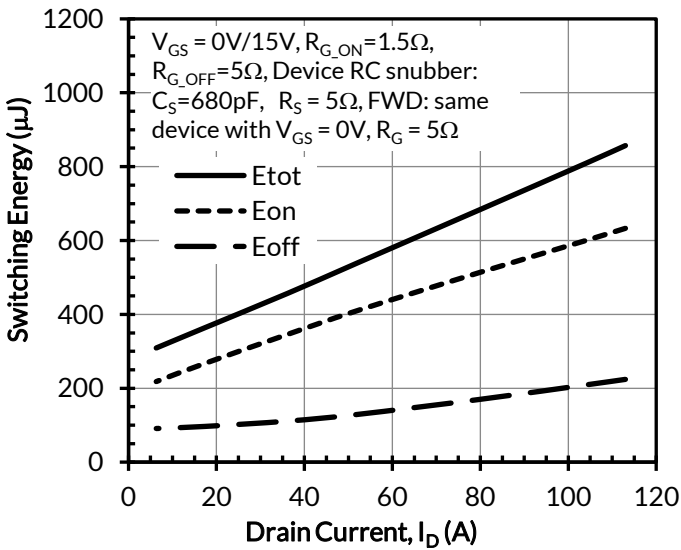


Figure 19. Clamped inductive switching energy vs. drain current at $V_{DS} = 400\text{V}$ and $T_J = 25^\circ\text{C}$

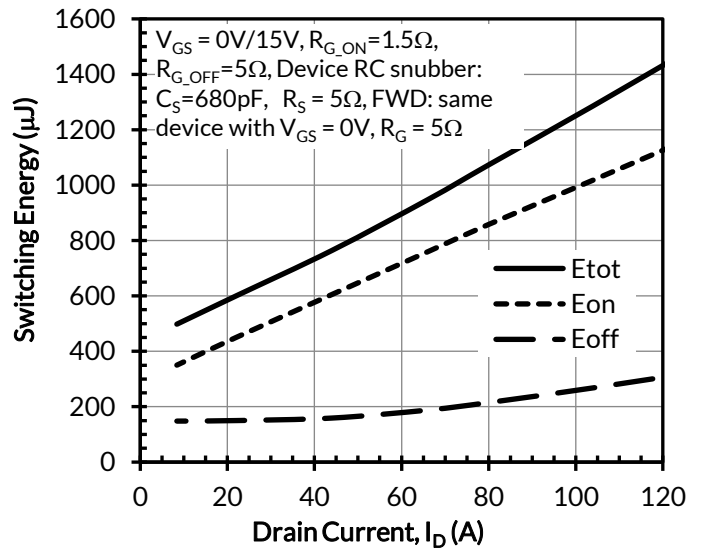


Figure 20. Clamped inductive switching energy vs. drain current at $V_{DS} = 500\text{V}$ and $T_J = 25^\circ\text{C}$

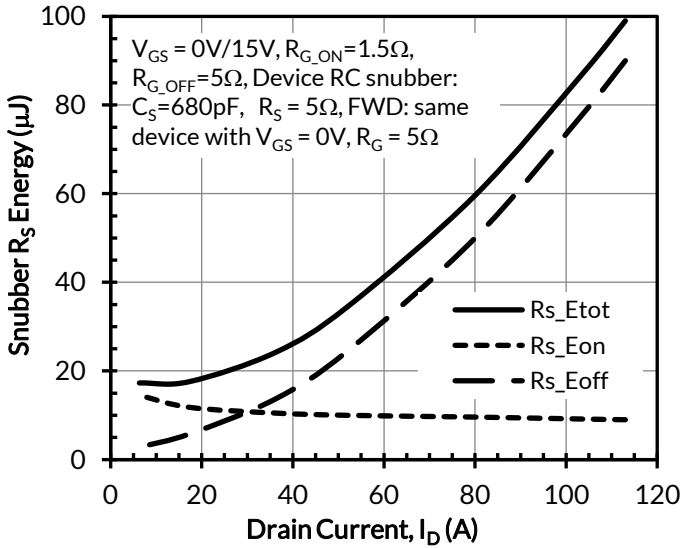


Figure 21. RC snubber energy loss vs. drain current at $V_{DS} = 400V$ and $T_J = 25^\circ C$

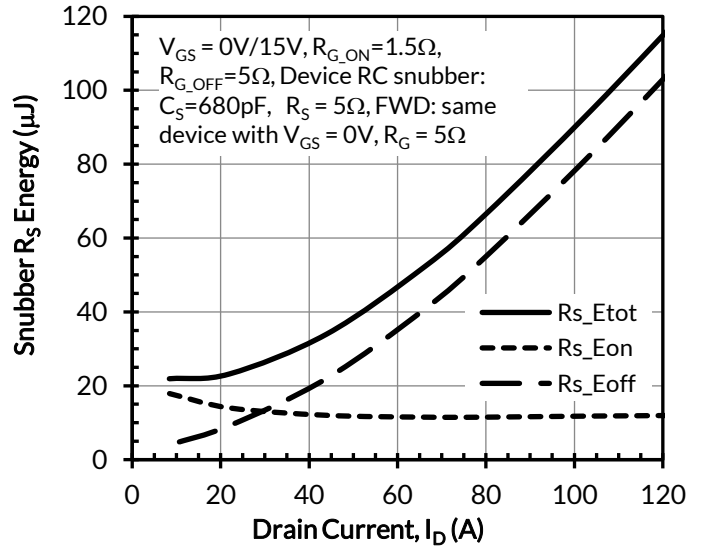


Figure 22. RC snubber energy losses vs. drain current at $V_{DS} = 500V$ and $T_J = 25^\circ C$

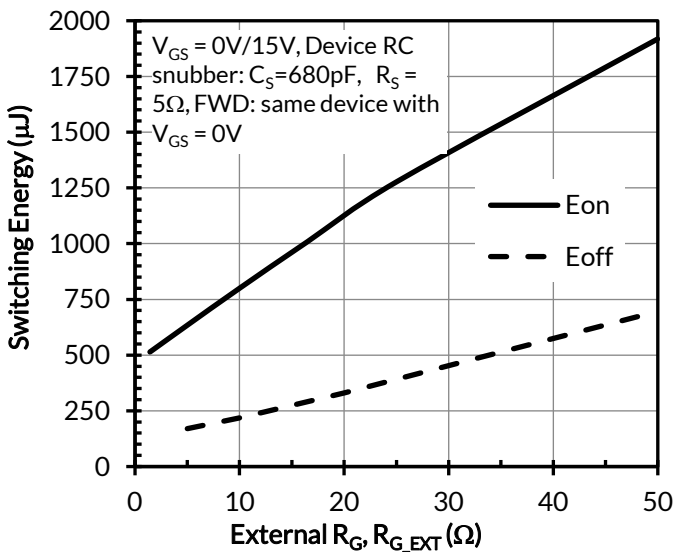


Figure 23. Clamped inductive switching energies vs. $R_{G,EXT}$ at $V_{DS} = 400V$, $I_D = 80A$, and $T_J = 25^\circ C$

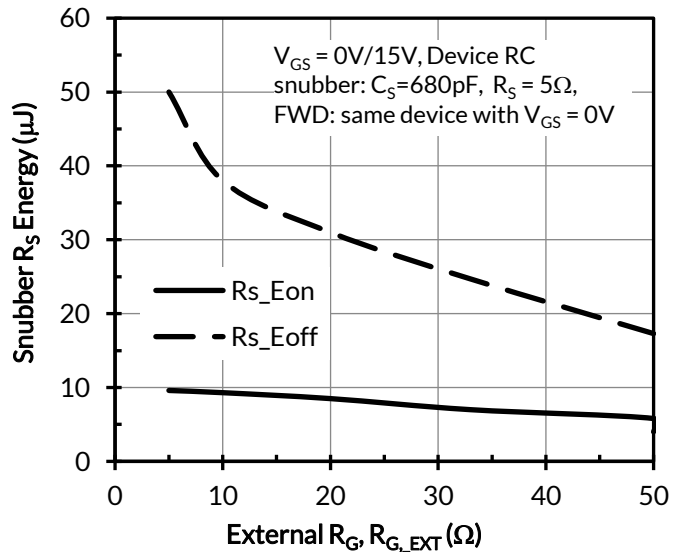


Figure 24. RC snubber energy losses vs. $R_{G,EXT}$ at $V_{DS} = 400V$, $I_D = 80A$, and $T_J = 25^\circ C$

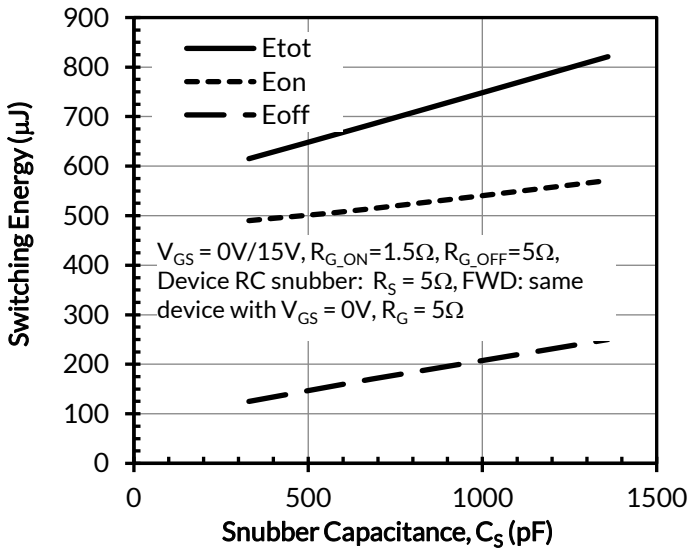


Figure 25. Clamped inductive switching energies vs. snubber capacitance C_S at $V_{DS} = 400V$, $I_D = 80A$, and $T_J = 25^\circ C$

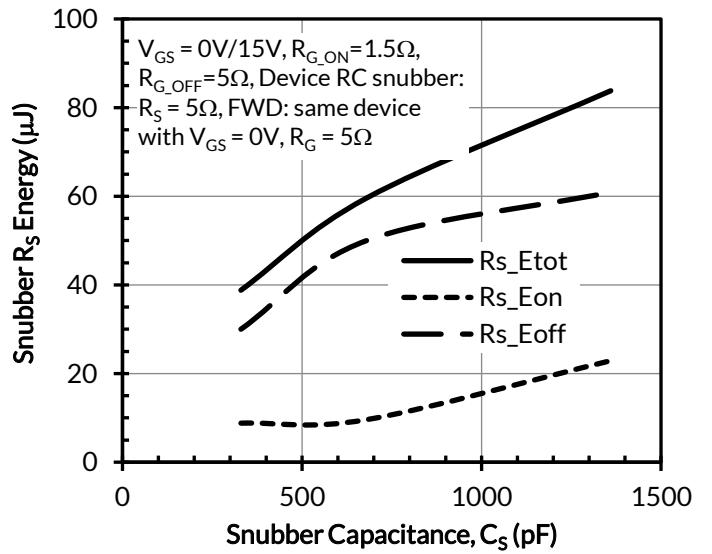


Figure 26. RC snubber energy losses vs. snubber capacitance C_S at $V_{DS} = 400V$, $I_D = 80A$, and $T_J = 25^\circ C$

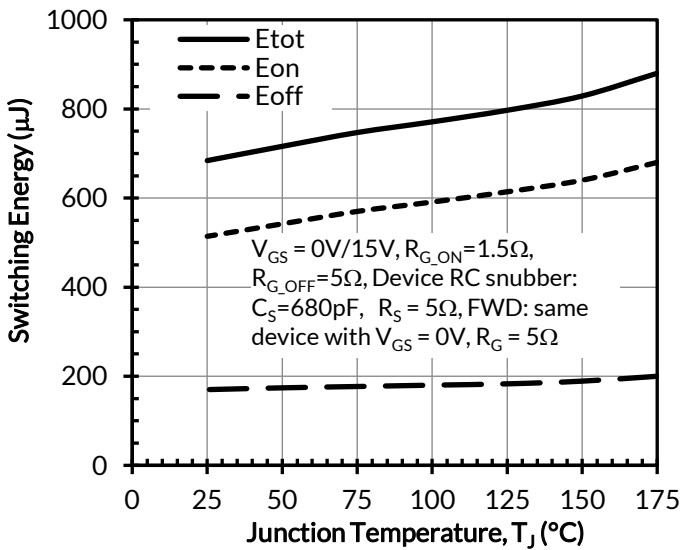


Figure 27. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 400V$ and $I_D = 80A$

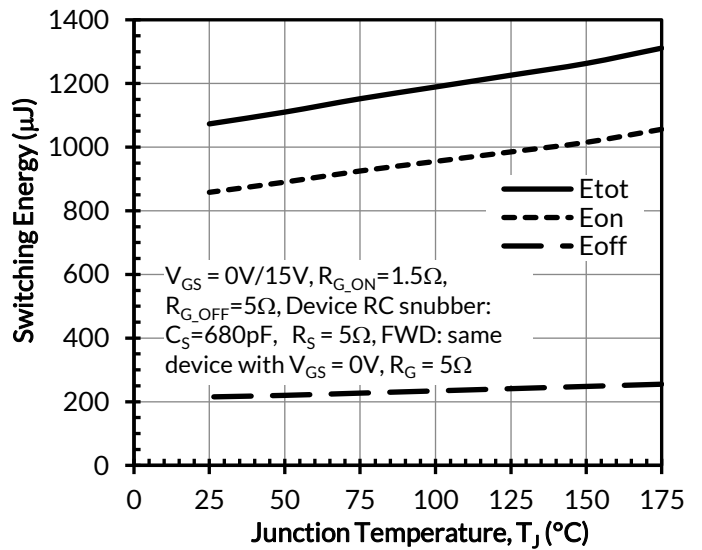


Figure 28. Clamped inductive switching energy vs. junction temperature at $V_{DS} = 500V$ and $I_D = 80A$

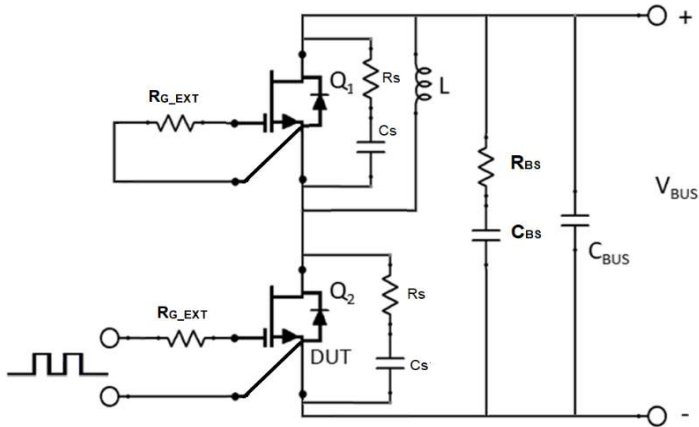


Figure 29. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber ($R_{BS} = 1\Omega$, $C_{BS} = 100\text{nF}$) is used to reduce the power loop high frequency oscillations.

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

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