User's Guide

TPSM41625 2-Phase Power Module Evaluation Module User's Guide

ABSTRACT

The TPSM41625-2X evaluation module (EVM) is designed as an easy-to-use platform that facilitates an extensive evaluation of the features and performance of two TPSM41625 devices combined to operate together in a stack-able configuration for increased current. The EVM operates over the entire input voltage range, 4-V to 16-V, of the TPSM41625. The output voltage can be set to several popular values by using configuration jumpers. Similarly, the switching frequency can be set to one of four values with a jumper. The full shared output current rating (50-A) of the device can be supplied by the EVM. Input and output capacitors are included on the board to accommodate the entire range of input and output voltages. Monitoring test points are provided to allow measurement of the following:

- Efficiency
- Power dissipation
- Input ripple
- Output ripple
- Line and load regulation
- Transient response

Control test points and component footprints are provided for use of the enable (EN), power good (PGOOD), SYNC, current sharing (ISH) and voltage sharing (VSH) features of the device. The EVM uses a recommended PCB layout that maximizes theermal performance and minimizes output ripple and noise.

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1 EVM Setup

Figure 1-1 highlights the user interface items associated with the EVM. The PVIN Power terminal block (J5) is used for connection to the host input supply and the VOUT Power terminal block (J3) is used for connection to the load. Terminal block J5 accepts up to a 10-AWG wire, J6 to a 14-AWG, and J3 & J4 accept up to a 6-AWG wire.

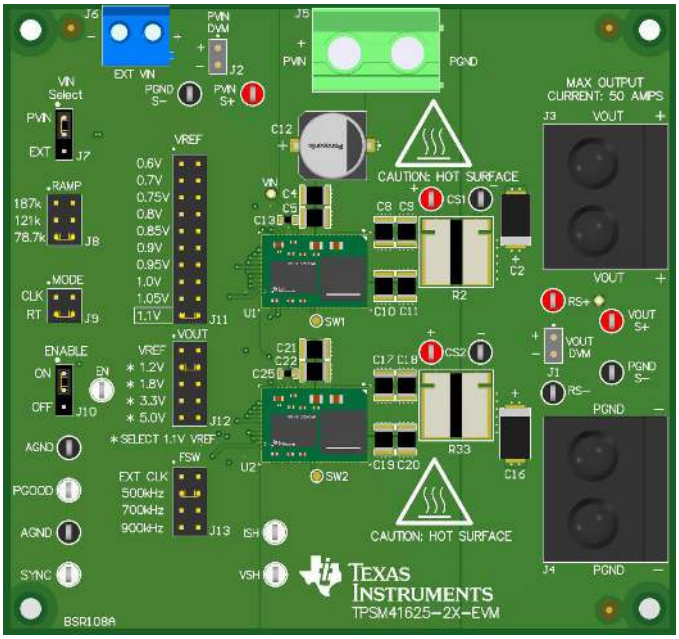

Figure 1-1. EVM User Interface

- The PVIN S+ and PVIN S- input voltage test points as well as the RS+ and RS- output voltage test points, located near the power terminal blocks are intended to be used as voltage monitoring points where voltmeter scan be connected to measure PVIN and VOUT. **Do not use these S+ and S- monitoring test points as the input supply or output load connection points.** The PCB traces connecting to these test points are not designed to support high currents.
- The PVIN Scope (J2) and VOUT Scope (J1) sockets can be used to monitor PVIN and VOUT waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes outfitted with a low inductance ground lead (ground spring) mounted to the scope probe barrel. The two sockets of each test point are on 0.1 inch centers. The scope probe tip should be inserted into the socket marked with a + sign, and the scope ground lead should be inserted into the other socket.
- The control test points located around the device are made available to test the features of the device. Refer to the EVM Connectors and Test Points for more information on the individual control test points. Other features, such as UVLO (R10, R13), ILIM (R12), SS (R15) and MODE (R29) can be altered by manually adding or changing the value on the associated footprints for each component located on the bottom-side of the EVM.
- The VREF jumper (J11), VOUT jumper (J12), FSW jumper (J13), and the RAMP jumper (J8) are provided for selecting the internal reference voltage, switching frequency, desired output voltage, and appropriate RAMP setting. Before applying power to the EVM, make sure that the jumpers are present and properly positioned for the intended output voltage. Ensure to set the internal reference voltage prior to selecting the desired output voltage (selecting the highest reference voltage will result in the most accurate output voltage set point). Refer to Table 1-1 and Table 1-2 for the recommended jumper settings.

Table 1-1. PVIN = 5 V Recommended Jumper Settings

OUTPUT VOLTAGE	VREF SELECT (J11)	VOUT SELECT (J12)	F_{SW} SELECT (J13)	RAMP (J8)
0.6 V - 7.5 V	0.6 V - 0.75 V	V_{REF}	500 kHz	187 kΩ
			700 kHz - 1 MHz	78.7 kΩ
0.8 V - 0.95 V	0.8 V - 0.95 V	V_{REF}	500 kHz - 700 kHz	78.7 kΩ
			1 MHz	78.7 kΩ
1 V - 1.1 V	1 - 1.1 V	V_{REF}	400 kHz - 1 MHz	187 kΩ
1.2 V	1.1 V	1.2 V	400 kHz - 1 MHz	187 kΩ
1.8 V	1.1 V	1.8 V	400 kHz - 1 MHz	187 kΩ
3.3 V	1.1 V	3.3 V	400 kHz - 1 MHz	78.7 kΩ

Table 1-2. 12 V Recommended Jumper Settings

OUTPUT VOLTAGE	VREF SELECT (J11)	VOUT SELECT (J12)	F_{SW} SELECT (J13)	RAMP (J8)
0.6 V - 7.5 V	0.6 V - 0.75 V	V_{REF}	400 kHz - 700 kHz	78.7 kΩ
0.8 V - 0.95 V	0.8 V - 0.95 V	V_{REF}	500 kHz - 700 kHz	78.7 kΩ
1 V - 1.1 V	1 - 1.1 V	V_{REF}	400 kHz - 1 MHz	78.7 kΩ
1.2 V	1.1 V	1.2 V	500 kHz	187 kΩ
			700 kHz - 1 MHz	121 kΩ
1.8 V	1.1 V	1.8 V	500 kHz	187 kΩ
			700 kHz - 1 MHz	78.7 kΩ
3.3 V	1.1 V	3.3 V	700 kHz - 1 MHz	187 kΩ
5.0 V	1.1 V	5.0 V	700 kHz - 1 MHz	187 kΩ

For example, if an output voltage of 1.8 V is desired and is supplied by a 12-V input, then a proper configuration is as follows:

1. Set VREF (J11) as 1.1 V.
2. Set VOUT (J12) as 1.8 V.
3. Set FSW (J13) as 500 kHz, 700 kHz, or 900 kHz.
4. Set RAMP (J8) as 187 kΩ if 500 kHz has been selected, or set RAMP as 78.7 kΩ if 700 kHz or 900 kHz has been selected.

Another example, if an output voltage of 1.0 V is desired and is supplied by a 12-V input, then a proper configuration is as follows:

1. Set VREF (J11) as 1.0 V.
2. Set VOUT (J12) as VREF.
3. Set FSW (J13) as 500 kHz, 700 kHz, or 900 kHz.
4. Set RAMP (J8) as 78.7 kΩ

2 EVM Connectors and Test Points

Wire-loop test points and scope probe sockets are included for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. Table 2-1 describes each test point (1).

Table 2-1. Test Point Descriptions

Test Point	Description
PVIN S+	Input voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency.
PVIN S-	Input voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency.
RS+	Output voltage monitor. Connect the positive lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
RS-	Output voltage monitor. Connect the negative lead of a DVM to this point for measuring efficiency, line regulation and load regulation.
AGND	Analog ground test point.
PGND	Power ground test point.
PVIN Scope (J2)	Input voltage scope monitor. Connect an oscilloscope probe to this set of points to measure input ripple voltage.
VOUT Scope (J1)	Output voltage scope monitor. Connect an oscilloscope probe to this set of points to measure output ripple voltage and transient response.
ENABLE (J10)	Enable test point. This test point can be used to monitor the EN voltage or to connect the EN pin to AGND to disable the device using a jumper wire. Additionally, for ease of use, J10 can be set in the ON position to enable the device or in the OFF position to disable the device.
PGOOD	Monitors the power good signal of the device. This is an open drain signal.
SYNC	Frequency synchronization pin. Connect the clock signal to the SYNC and AGND test points when synchronizing to an external clock. Additionally, set MODE jumper (J9) to CLK.
ISH	Current sharing test point. This test point can be used to monitor the shared current between the two devices.
VSH	Voltage sharing test point. This test point can be used to monitor the shared voltage between the two devices.

(1) Refer to the product data sheet for absolute maximum ratings associated with above features.

3 Test Results

Figure 3-1 and Figure 3-2 demonstrate the enable ON/OFF performance of the EVM. Figure 3-3 shows the typical output voltage ripple with a 25-A load. All figures shown below are under the following conditions: 12-V input voltage, 1.2-V output voltage and a switching frequency of 700 kHz. Additional output capacitor footprints are available on the EVM if an improved load transient response or output voltage ripple is needed. See the data sheet for more information on the respective devices.

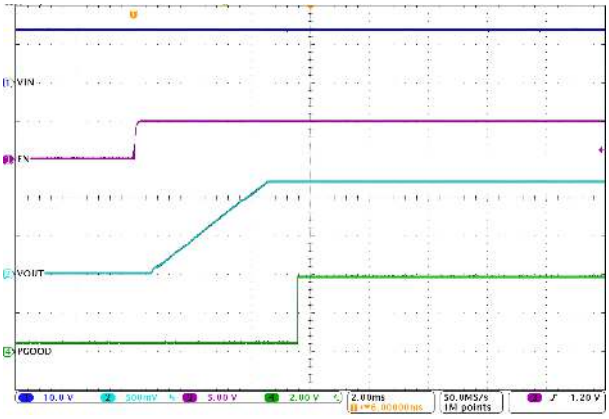

Figure 3-1. ENABLE Start-Up Waveform

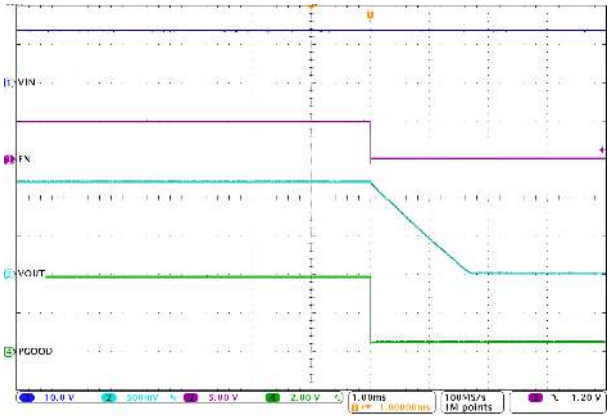

Figure 3-2. ENABLE Shutdown Waveform

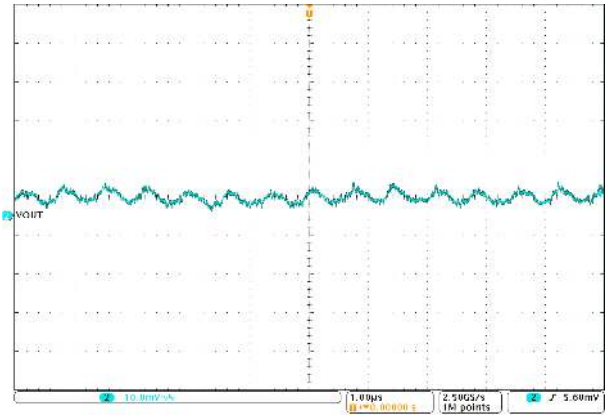

Figure 3-3. 25-A Output Voltage Ripple

4 PCB Layouts

Figure 4-1 through Figure 4-10 show the PCB layers of the EVM.

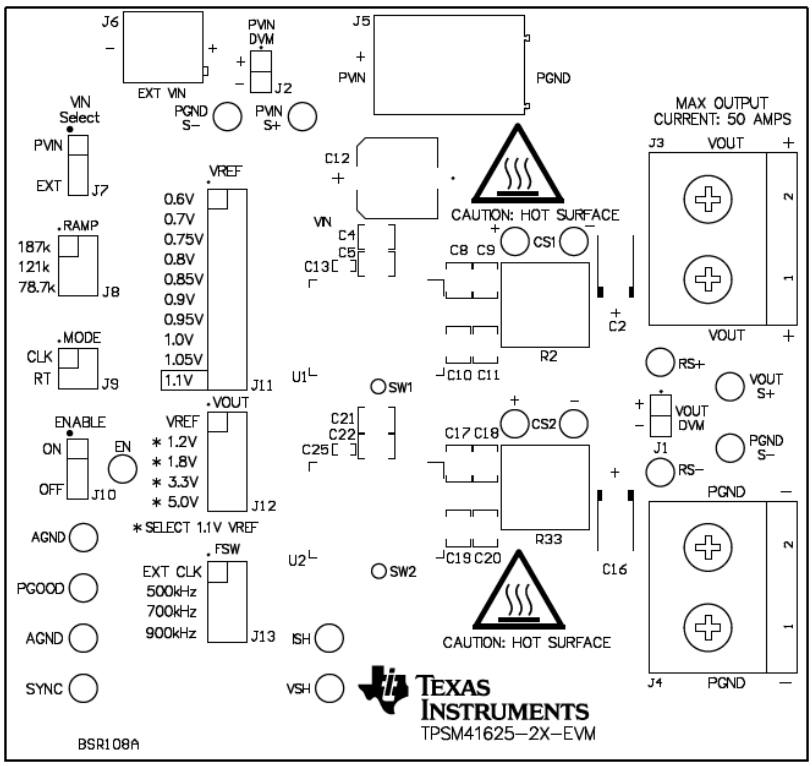

Figure 4-1. Top Silk Screen (Top View)

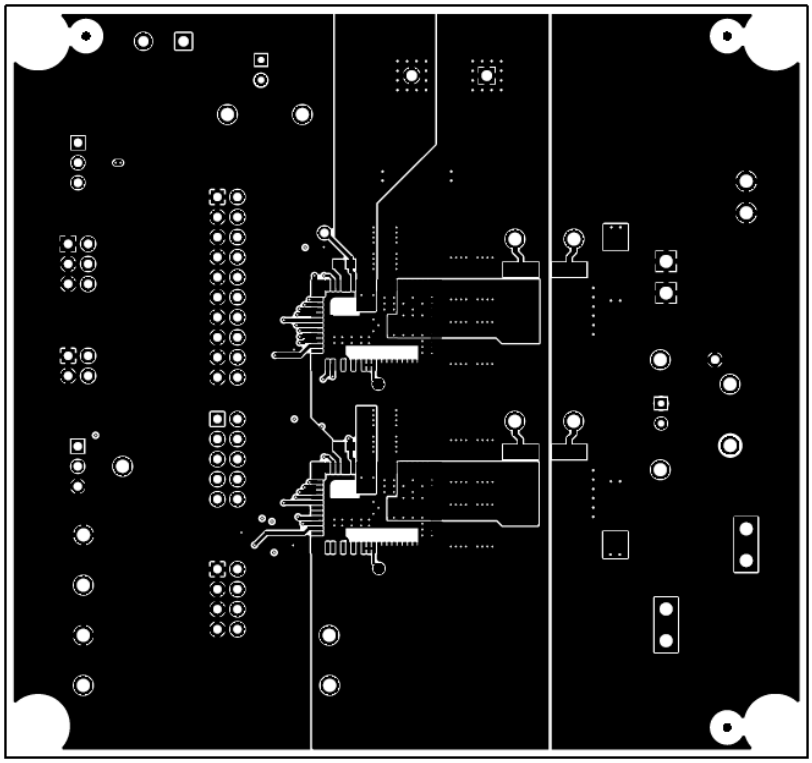

Figure 4-2. Top Layer

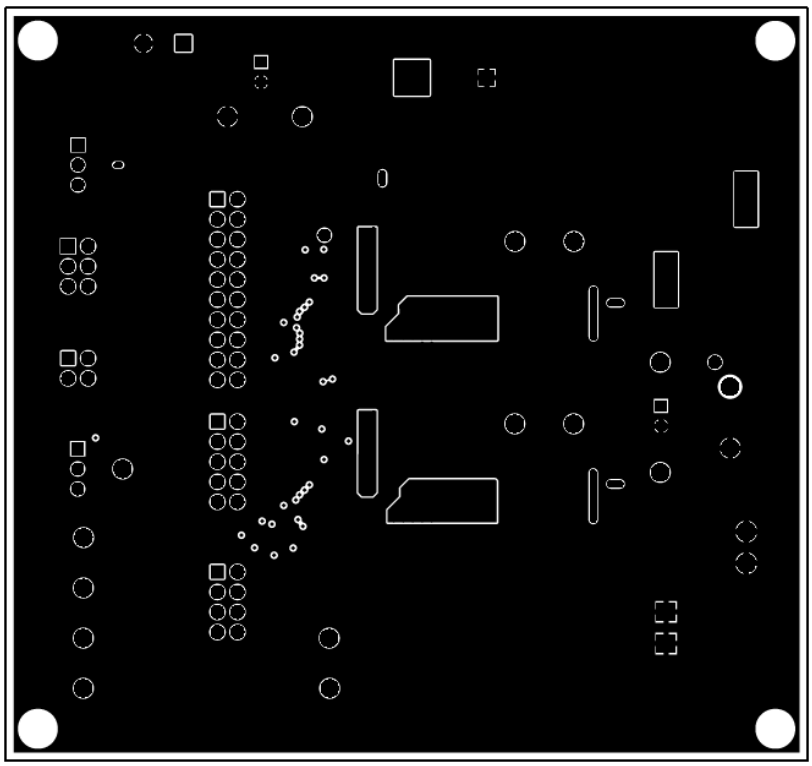

Figure 4-3. Signal Layer 1

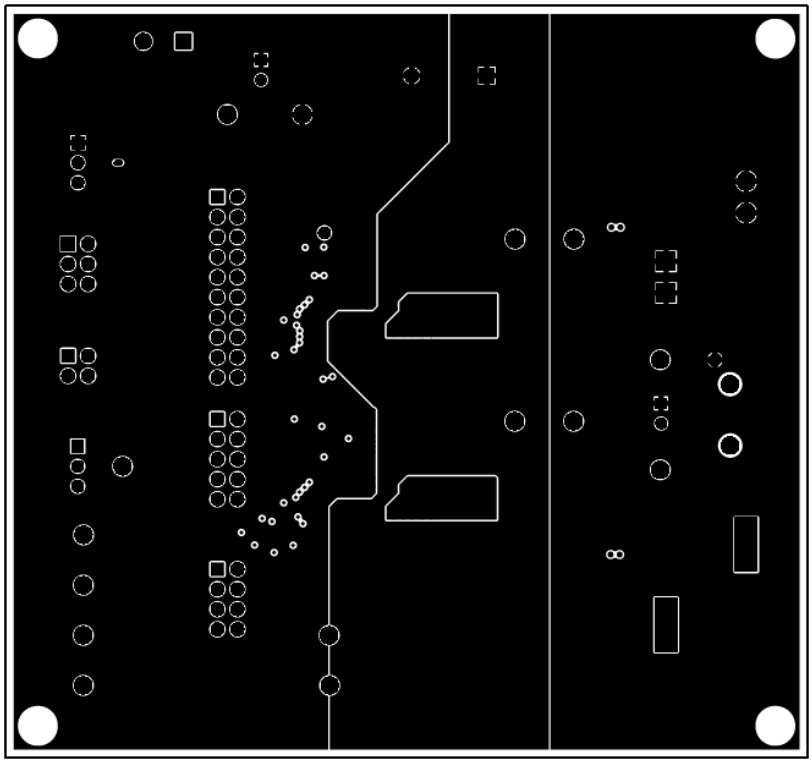

Figure 4-4. Signal Layer 2

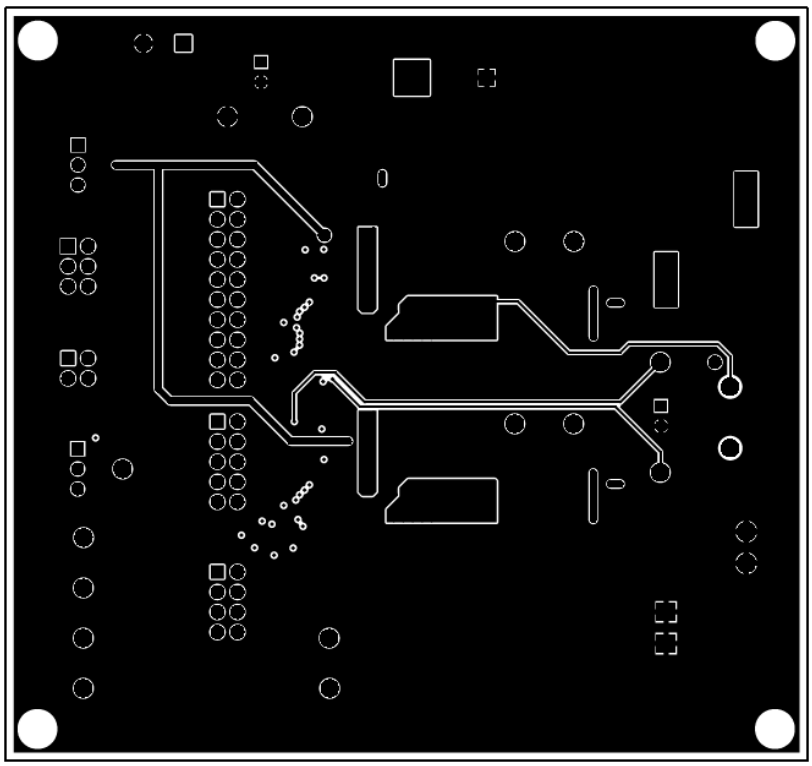

Figure 4-5. Signal Layer 3

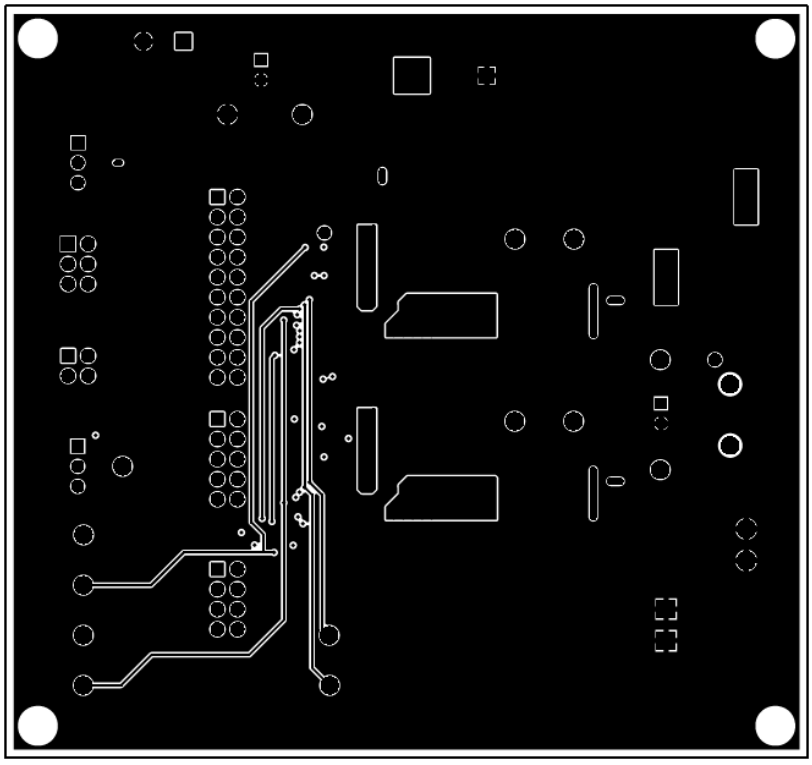

Figure 4-6. Signal Layer 4

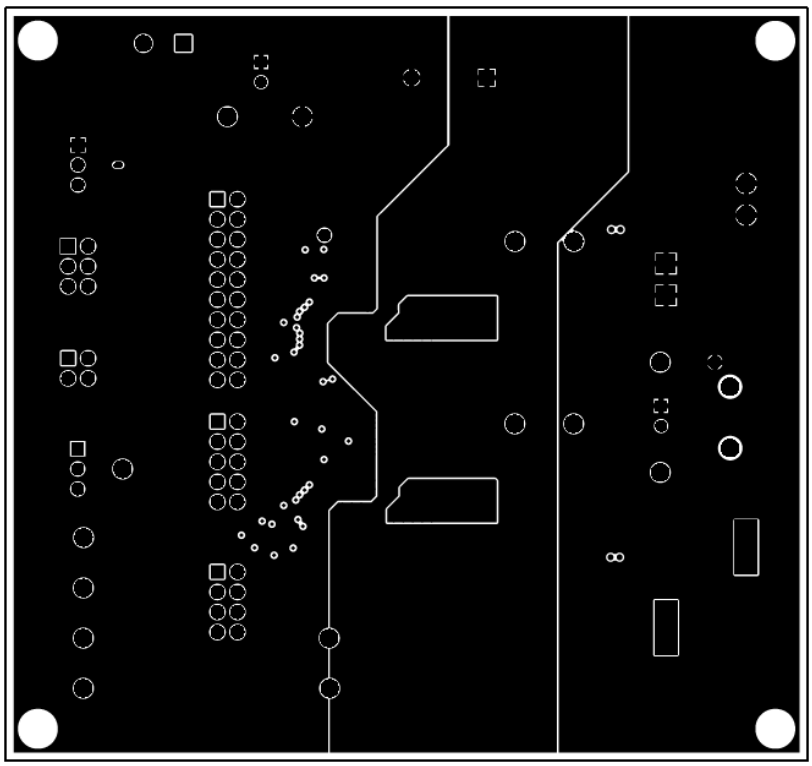

Figure 4-7. Signal Layer 5

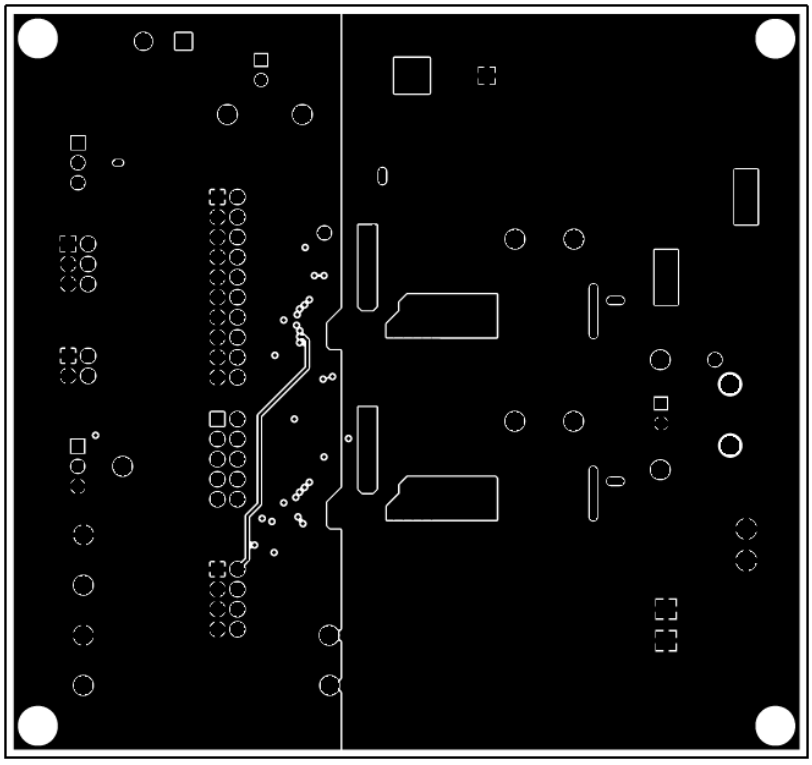

Figure 4-8. Signal Layer 6

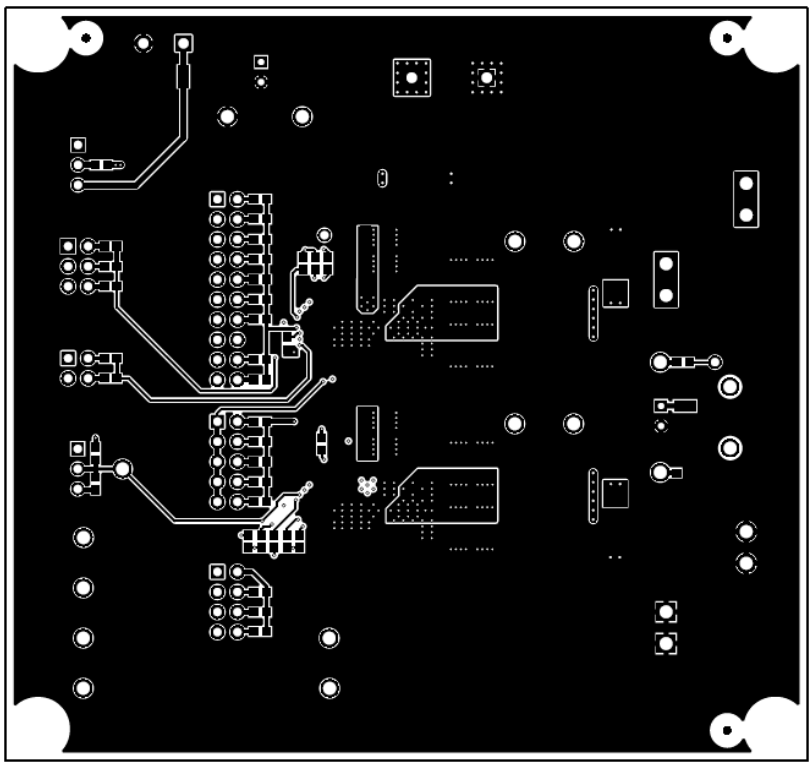

Figure 4-9. Bottom Layer

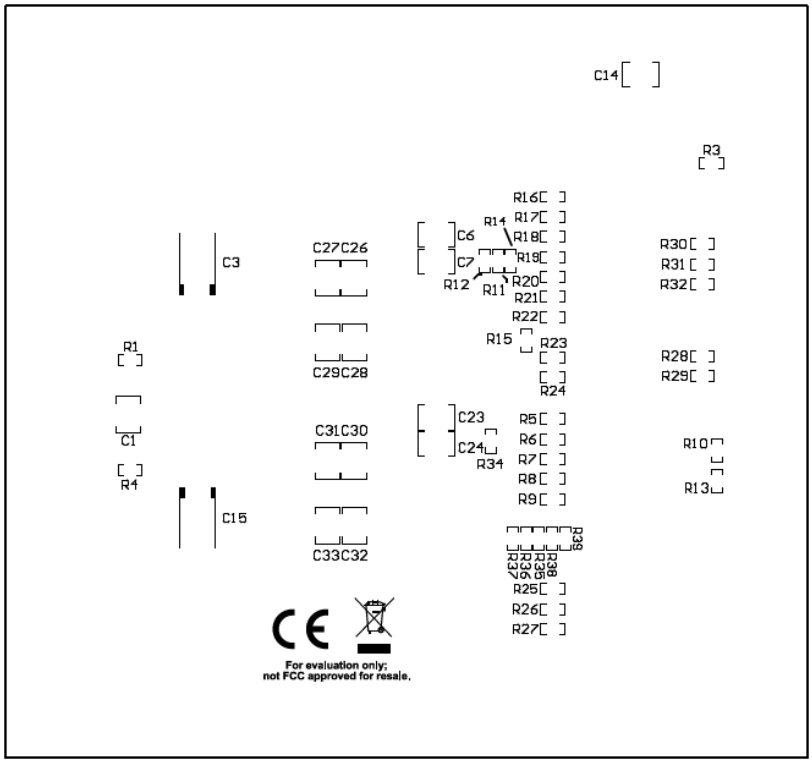

Figure 4-10. Bottom Layer Silk Screen (Bottom View)

5 Schematics

Figure 5-1 is the schematic for the device configured as primary.

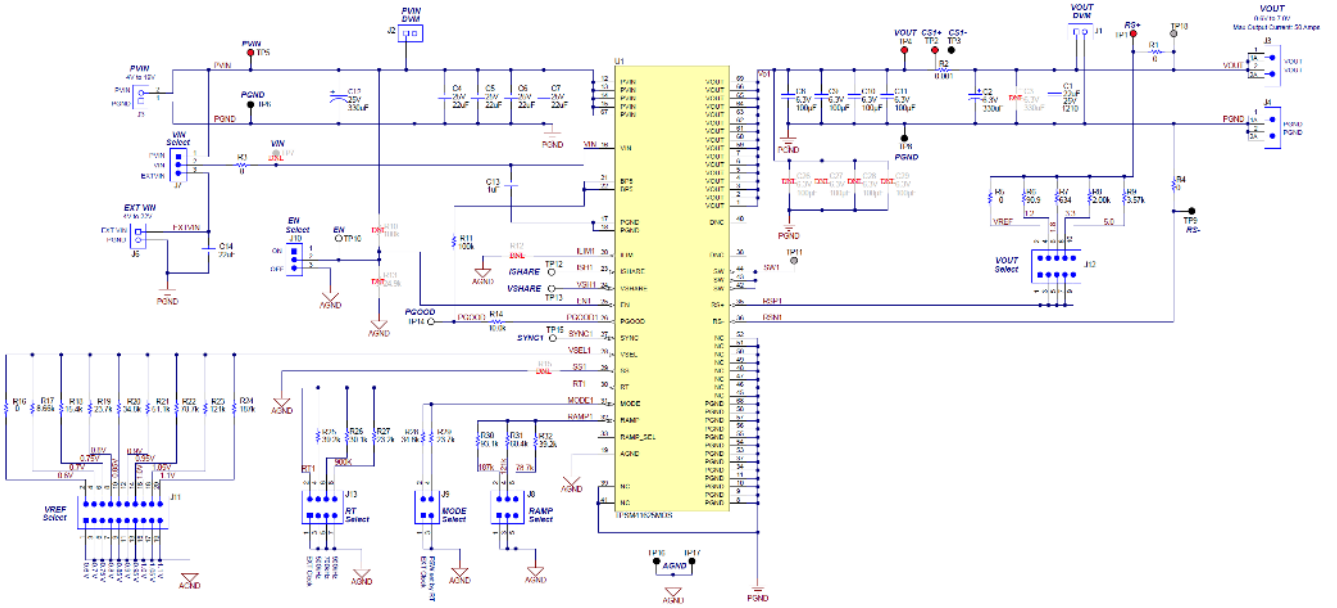

Figure 5-1. Primary Schematic

Figure 5-2 is the schematic for the device configured as secondary.

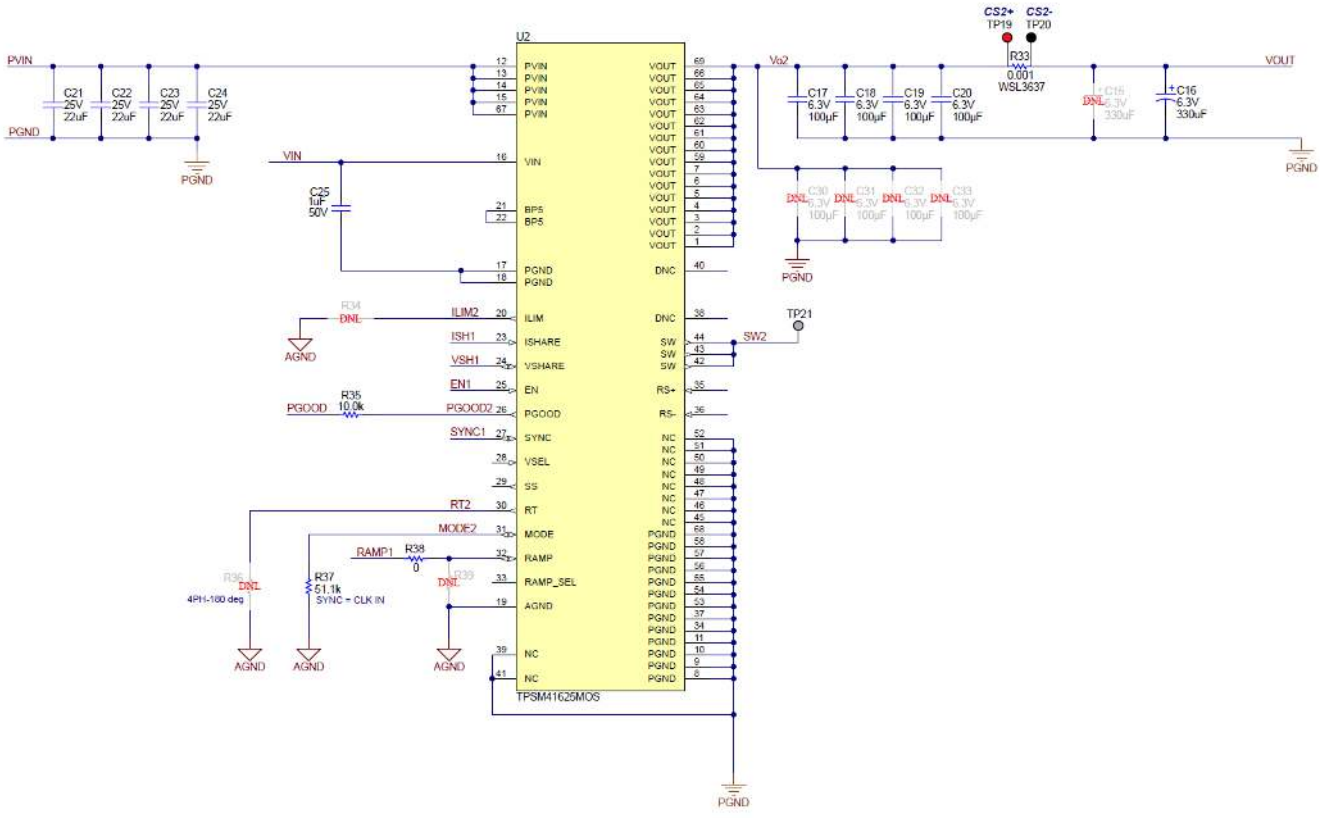

Figure 5-2. Secondary Schematic

6 Bill of Materials

Table 6-1. TPSM41925 Evaluation Module Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number
C1, C4, C5, C6, C7, C14, C21, C22, C23, C24	10	22uF	CAP, CERM, 22 uF, 25 V, X7R	1210	GRM32ER71E226KE15L
C2, C16	2	330uF	CAP, Tantalum Polymer, 330 uF, 6.3 V	2917	6TPE330MAA
C8, C9, C10, C11, C17, C18, C19, C20	8	100uF	CAP, CERM, 100 µF, 6.3 V, X7S	1210	GRM32EC70J107ME15L
C12	1	330µF	330µF 25V Aluminum Electrolytic Capacitors	RADIAL	EEE-FC1E331AP
C13, C25	2	1uF	CAP, CERM, 1 uF, 50 V, X7R,	0603	UMK107AB7105KA-T
J1, J2	2		Socket Strip, 2x1, Black	100mil, 2pin	310-43-102-41-001000
J3, J4	2		Terminal Block, 60A, 10.16mm Pitch, 2-Pos	21.8x30x19 mm	399100102
J5	1		Receptacle	9.52mm, 2x1	1714971
J6	1		Terminal Block	2x1 5.08 mm, 2x1	ED120/2DS
J7, J10	2		Header	3 PIN, 100mil	PEC03SAAN
J8	1		Header	3x2, 100mil	TSW-103-07-G-D
J9	1		Header	2x2, 100mil	TSW-102-07-G-D
J11	1		Header	10x2, 100mil	TSW-110-07-G-D
J12	1		Header	5x2, 100mil	TSW-105-07-G-D
J13	1		Header	4x2, 100mil	TSW-104-07-G-D
R1, R3, R4, R5, R16, R38	6	0	RES, 0, 5%, 0.1 W	0603	CRCW06030000Z0EA
R2, R33	2	0.001	RES, 0.001, 1%, 3W	WSL3637	WSL36371L000FEA
R6	1	90.9	RES, 90.9, 1%, 0.1 W	0603	CRCW060390R9FKEA
R7	1	634	RES, 634, 1%, 0.1 W	0603	CRCW0603634RFKEA
R8	1	2.00k	RES, 2.00 k, 1%, 0.1 W	0603	ERJ3EKF2001V
R9	1	3.57k	RES, 3.57 k, 1%, 0.1 W	0603	CRCW06033K57FKEA
R11	1	100k	RES, 100 k, 1%, 0.1 W	0603	CRCW0603100KFKEA
R14, R35	2	10.0k	RES, 10.0 k, 1%, 0.1 W	0603	CRCW060310K0FKEA
R17	1	8.66k	RES, 8.66 k, 1%, 0.1 W	0603	CRCW06038K66FKEA
R18	1	15.4k	RES, 15.4 k, 1%, 0.1 W	0603	CRCW060315K4FKEA
R19, R29	2	23.7k	RES, 23.7 k, 1%, 0.1 W	0603	CRCW060323K7FKEA
R20, R28	2	34.8k	RES, 34.8 k, 1%, 0.1 W	0603	CRCW060334K8FKEA
R21, R37	2	51.1k	RES, 51.1 k, 1%, 0.1 W	0603	CRCW060351K1FKEA
R22	1	78.7k	RES, 78.7 k, 1%, 0.1 W	0603	CRCW060378K7FKEA
R23	1	121k	RES, 121 k, 1%, 0.1 W	0603	CRCW0603121KFKEA
R24	1	187k	RES, 187 k, 1%, 0.1 W	0603	CRCW0603187KFKEA
R25, R32	2	39.2k	RES, 39.2 k, 1%, 0.1 W	0603	CRCW060339K2FKEA
R26	1	30.1k	RES, 30.1 k, 1%, 0.1 W	0603	RC0603FR-0730K1L
R27	1	23.2k	RES, 23.2 k, 1%, 0.1 W	0603	CRCW060323K2FKEA
R30	1	93.1k	RES, 93.1 k, 1%, 0.1 W	0603	CRCW060393K1FKEA
R31	1	60.4k	RES, 60.4 k, 1%, 0.1 W	0603	CRCW060360K4FKEA
TP1, TP2, TP4, TP5, TP19	5		Test Point, Red	Red Multipurpose Testpoint	5010
TP3, TP6, TP8, TP9, TP16, TP17, TP20	7		Test Point, Black	Black Multipurpose Testpoint	5011
TP10, TP12, TP13, TP14, TP15	5		Test Point, White	White Multipurpose Testpoint	5012

Table 6-1. TPSM41925 Evaluation Module Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number
U1, U2	2		4-V to 16-V Input, 25-A DC/DC power module	QFM69	TPSM41625MOVR
C3, C15	0			2917	
C26, C27, C28, C29, C30, C31, C32, C33	0			1210	
R10, R12, R13, R15, R34, R36, R39	0			0603	

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (May 2021)	Page
• Updated user's guide title	3

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