National Semiconductor

ADVANCE INFORMATION
December 1997

NS486™SXL
Optimized 32-Bit 486-Class Controller with On-Chip Peripherals for Embedded Systems

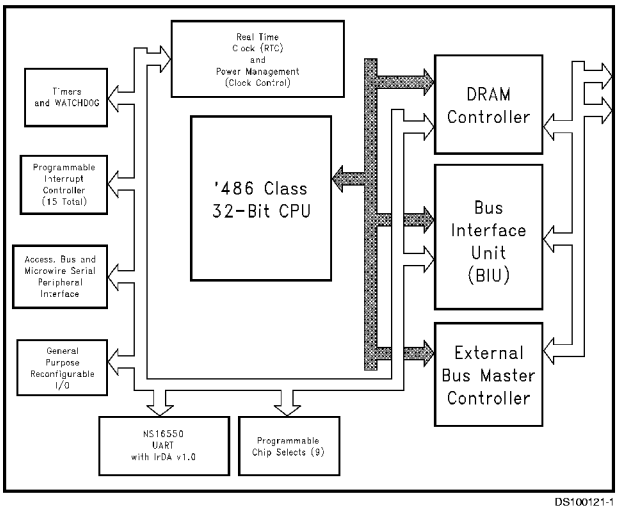
General Description

The NS486SXL is a highly integrated embedded system controller incorporating an Intel486™-class 32-bit processor along with all of the necessary System Service Elements, implementing a true "system on a chip." It is ideally suited for a wide variety of applications running in a segmented protect-mode environment. The NS486SXL is the second member of the NS486 family.

Features

- 100% compatible with VxWorks™, VRTX™, QNX™ Neutrino, pSOS +®, and other popular real-time executives and operating system kernels
- Intel486 instruction set compatible (protected mode only) with optimized performance
- Operation at 25 MHz with 5V supply
- Low cost 132-pin PQFP package
- Industry standard interrupt controller, timers, and real time clock
- Protected WATCHDOG™ timer
- Optimized DRAM Controller (supports two banks, up to 8 Mbytes each)
- Up to nine versatile, programmable chip selects
- Up to eight external interrupts directly supported, and additional interrupt expansion through an external PIC interface
- Glueless interface to ISA-type peripherals
- Arbitration support for auxiliary processor
- Support for External Bus Masters, allowing them to access DRAM and on-chip Peripherals
- MICROWIRE™/Access.bus synchronous serial interfaces
- UART with IrDA v1.0 (Infrared Data Association) port
- Reconfigurable I/O: Up to 28 I/O pins can be used as general purpose bidirectional I/O lines
- Flexible, programmable, multilevel power saving modes maximize power savings
- Programming model compatible with the NS486SXF where possible

Block Diagram NS486SXL Single-Chip Embedded Controller



DS100121-1

MICROWIRE™, NS486™ and WATCHDOG™ are trademarks of National Semiconductor Corporation.
TRI-STATE® is a registered trademark of National Semiconductor Corporation.
Intel486™ is a trademaek of Intel Corporation.
pSOS +™ is a trademark of Integrated Systems, Inc.
VRTX™ is a registered trademark of Microtec Research, Inc.
PowerPack® is a registered trademark of Microtek International.
QNX™ is a registered trademark of QNX Software Systems, Inc.
VxWorks™ is a registered trademark of Wind River Systems, Inc.

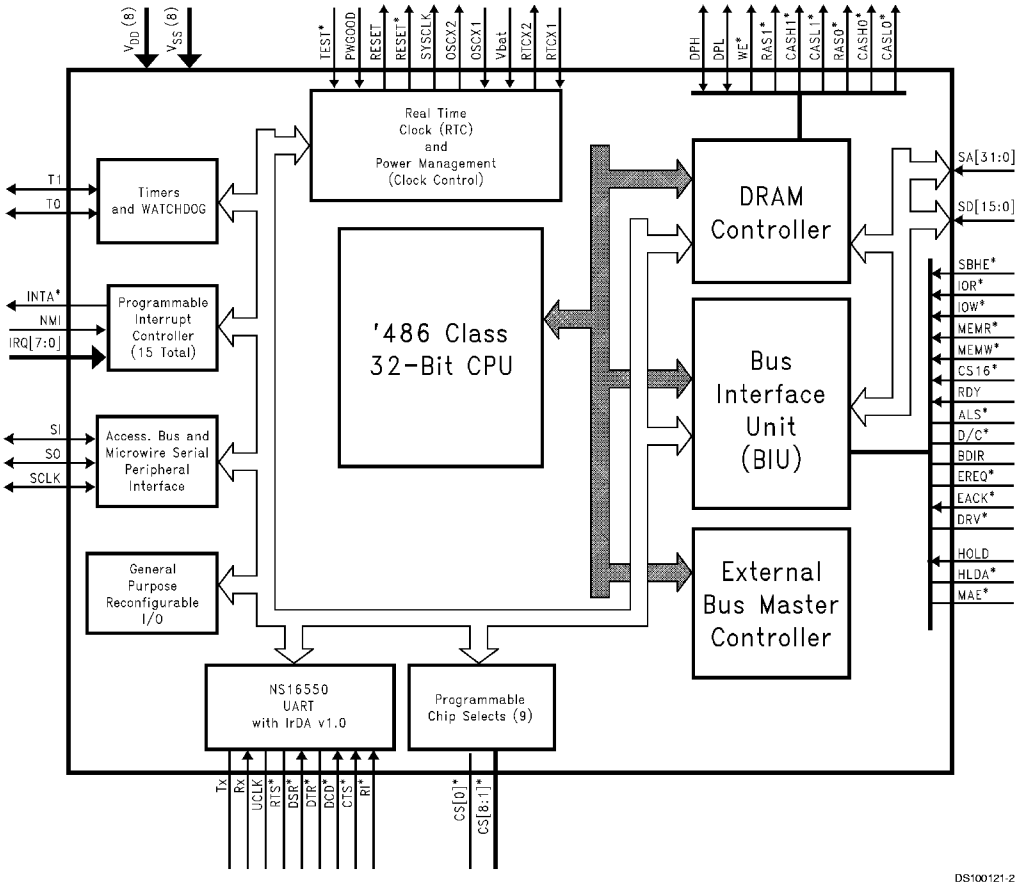
Table of Contents

List of Tables

List of Figures

1.0 System Overview

1.1 NS486SXL SYSTEM OVERVIEW



***Indicates low-true signals

FIGURE 1. NS486SXL Internal Resource to Pins Map

The NS486SXL is a highly integrated embedded system controller. It includes an Intel486-class 32-bit processor, all resources required for the System Service Elements of a Real-Time Executive, and a selection of key I/O peripherals. This "system-on-a-chip" is ideal for implementing a wide variety of embedded applications.

The 32-bit processor core executes all of the Intel486 instructions with a similar number of clocks per instruction. An on-board 1 Kbyte instruction cache provides for efficient execution from ROM. Intel486 debug features are supported. The processor has been optimized for operating system kernels such as VRTX, VxWorks, pSOS+ and QNX. These environments only need the '486 protected mode operation (no real mode or virtual 8086 support), flat or linear memory addressing (no virtual memory paging), and floating point execution in software only (no co-processor interface).

In fact, the NS486SXL includes all of the System Service Elements required by a typical kernel, including an efficient DRAM controller that supports pagemode DRAMs for data cache-like performance; three timer channels (including one configured as a protected WATCHDOG Timer); two programmable 8259 interrupt controllers provide 15 on-chip interrupt sources; an industry standard real time clock and calendar (RTC) with battery backup; and support for comprehensive power management schemes.

In addition, the NS486SXL also incorporates the key I/O peripherals required for implementing a wide variety of embedded applications: an industry standard high-performance NS16550-compatible UART with HP-SIR and IrDA v1.0 infrared option, an 8254 timer, and a general purpose 2- or 3-wire synchronous serial interface for easy interface to low-cost EEPROMs and other serial peripherals. System expansion is supported with nine programmable Chip Select (CS) signals and a generic ISA-type bus interface for external devices and memory.

1.0 System Overview (Continued)

Certain I/O lines not being used by disabled peripherals can be reconfigured for use as general purpose bidirectional I/O lines (up to 28 pins). This gives the designer maximum flexibility in designing various systems using the NS486SXL device. It is expected that an NS486SXL system will minimally include the NS486SXL system controller with on-board processor and I/O devices, boot ROM, and working RAM memory. Many applications will not require any additional I/O support.

Finally, the NS486SXL implements a very flexible power management scheme that permits selective control of individual I/O subsystems, with varying levels of power consumption.

NS486SXL provides a cost-effective hardware platform for the design and implementation of a wide range of internet appliance, networking and communication systems. With its powerful embedded '486-class processor, comprehensive set of on-chip peripheral controllers, flexible power management structure and reconfigurable I/O lines, NS486SXL makes possible a variety of end-user systems based on the same hardware. Because of its optimized design and on-board resources, a very cost effective system can be achieved.

1.2 32-BIT PROCESSOR CORE

The NS486SXL processor core is an implementation of the protected mode '486 instruction set architecture, optimized using a RISC-like design philosophy for embedded applications. Using this approach, the most frequently used instructions are optimized, and on an average execute in a lower number of clock cycles than a '486.

The NS486SXL features a three stage pipeline, efficient instruction prefetching mechanism, and single cycle instruction decoding for most instructions. Additionally, a 1 Kbyte instruction cache and single cycle DRAM access provide higher memory performance than a larger unified cache implementation.

The NS486SXL processor provides the same programming model and register set as the standard '486 except that real mode, virtual memory, and floating point support have been eliminated. These features have little or no impact in embedded applications and save significant silicon real estate. At reset, unlike the standard '486, the NS486SXL starts up in protected mode instead of real mode. All '486 instructions appropriate to protected mode and our hardware configuration are supported, including debug instructions.

The NS486SXL is initially available to run 25 MHz at 5V. The processor clock is obtained by dividing the crystal frequency by two. For example, a 25 MHz NS486SXL runs with a 50 MHz crystal oscillator as the master clock.

As a result of our innovative design, the NS486SXL achieves performance equivalent to a standard '486 with less circuitry. This translates into reduced power consumption and a lower overall system cost. It also makes the NS486SXL ideal for "green" systems and battery operated systems.

1.3 SYSTEM SERVICE ELEMENTS

The NS486SXL controller provides the basic hardware resources required for the O/S-defined System Service Elements. These include a DRAM controller, programmable interval timer, a protected WATCHDOG timer, a programmable interrupt controller, a real-time clock and calendar, and comprehensive power management features.

1.3.1 DRAM Controller

The NS486SXL DRAM controller supports one or two adjustable-sized banks of dynamic RAM using a 16-bit data path. Support is provided for byte parity (if desired), requiring the DRAM banks to be 18-bits wide when parity is enabled. Banks can be up to 8 Mbytes in size. The DRAM controller supports page mode read and write operations and can also support both byte and word accesses. All access control signals for read, write and parity checking are generated as well as an automatic and programmable CAS-before-RAS refresh. If self-refresh DRAMs are used, refresh can be disabled, saving power.

NS486SXL provides flexible support for use of a number of different DRAM configurations, using popular DRAM devices. Access is optimized for fast page mode DRAMs, and they will provide the highest performance with contiguous data. When accessing data bytes or words in the same DRAM page, the data access is in one cycle. This performance provides fast data access times without the overhead of a separate data cache. Page sizes can be 512, 1024, 2048 or 4096 bytes. Flexibility for DRAM timing is provided through programming of the DRAM controller registers: 3 or 4 cycle page miss accesses and extended CAS cycles can be selected.

Memory bank 0 starts at address 0h; memory bank 1 can start at any address in the 128 Mbyte address map that is a multiple of its size.

1.3.2 Programmable Interval Timer

The NS486SXL programmable interval timer is compatible with the Intel 8254 programmable interval timer and contains three identical timers (CH0–CH2). CH0 and CH1 can be used to generate accurate timing delays under software control. CH2 may be configured to provide a WATCHDOG timer function.

1.3.3 WATCHDOG Timer

The NS486SXL WATCHDOG timer, CH2, is a protected 16-bit timer that can be used to prevent system "lockups or hangups." It uses a 1 kHz clock generated by the on-chip real-time clock circuit. If the WATCHDOG timer is enabled and times out, a reset or interrupt will be generated allowing graceful recovery from an unexpected system lockup.

1.3.4 Interrupt Controller

The NS486SXL interrupt controller consists of two cascaded programmable interrupt controllers that are compatible with the Intel 8259A Programmable Interrupt Controller. They provide a total of 15 (out of 16) programmable interrupts. Three interrupts are reserved for a real time clock-tick interrupt, a real time clock interrupt request, and a cascade interrupt channel. The remaining 13 interrupts can be used by internal or external sources. Additional external interrupt controllers can be cascaded as well.

1.3.5 Real Time Clock/Calendar

The NS486SXL Real Time Clock/Calendar is a low power clock that provides a time-of-day clock and 100-year calendar with alarm features and battery operation. Time is kept in BCD or binary format. It includes 50 bytes of general purpose CMOS RAM and 3 maskable interrupt sources. It is compatible with the DS1287 and MC146818 RTC/Calendar devices, except for the general purpose memory size.

1.0 System Overview (Continued)

1.3.6 Power Management Features

The NS486SXL power management structure includes a number of power saving mechanisms that can be combined to achieve comprehensive power savings under a variety of system conditions. First of all, the core processor power consumption can be controlled by varying the processor/system clock frequency. The internal CPU clock can be divided by 4, 8, 16, 32 or 64. In addition, in idle mode, the internal processor clock will be disabled. Finally, if an external crystal oscillator circuit is being used, it can be disabled. For maximum power savings, all internal clocks can be disabled (except for the real-time clock oscillator).

The clocks of the on-board peripherals can be individually or globally controlled. By setting bits in the power management control registers, the internal clocks to the three-wire interface, the timer, the DRAM controller, and the UART can be disabled.

In addition to these internal clocks, the external SYSCLK can be disabled via a bit in the power management control registers.

Using various combinations of these power saving controls with the NS486SXL controller will result in excellent programmable power management for any application.

1.4 NS486SXL SYSTEM BUS

The NS486SXL system bus provides the interface to off-chip peripherals and memory. It offers an ISA compatible interface and is therefore capable of directly interfacing to many ISA peripheral control devices. The interface is accomplished through the Bus Interface Unit (BIU). The BIU generates all of the access signals for both internal and external peripherals and memory. Depending upon whether the access is to internal peripherals, external peripherals or external memory, the BIU generates the timing and control signals to access those resources. The BIU is designed to support a glueless interface to many ISA-type peripherals.

For debug purposes, the NS486SXL can be set to generate external bus cycles at the same time as an internal peripheral access takes place. This gives logic analyzers or other debug tools the ability to track and capture internal peripheral accesses.

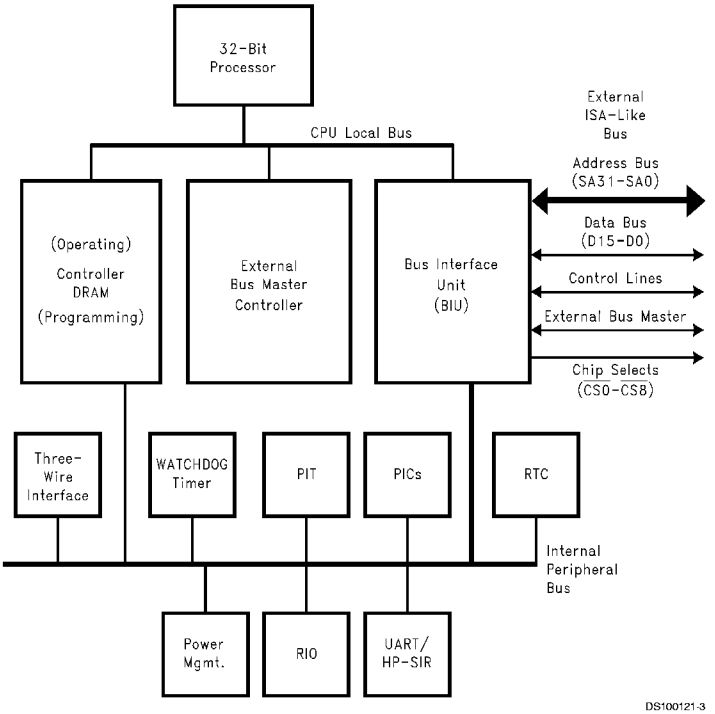


FIGURE 2. NS486SXL Internal Busses

Access to internal peripherals is accomplished in three CPU T-states (clock cycles). The fastest access to off-chip I/O is also three T-states. When accessing off-chip memory and I/O, wait state generation is accomplished through a combination of NS486SXL chip select logic and off-chip peripheral feedback signals.

The ISA-like bus on the NS486SXL also supports External Bus Masters. This feature allows external processors or I/O Peripherals (and customer proprietary ASICs) with built-in DMA controllers to read and write System DRAM supported by the 'SXL DRAM Controller. External Masters can also access any internal or external peripherals or memory as well. The external master address must be at TRI-STATE® (through external address transceivers if necessary) in order to support external master access to the DRAM.

1.0 System Overview (Continued)

Finally, the Bus Interface Unit also provides signals to indicate bus activity and control (optional) data bus transceiver direction. The bus direction signal, and chip selects continue to operate correctly during external master accesses.

1.5 OTHER ON-BOARD PERIPHERALS

In addition to those peripherals and system control elements needed for System Service Elements, the NS486SXL also includes a number of I/O controllers and resources that make implementing a complete embedded system possible with just a single-chip NS486SXL controller. These include a serial UART port, and a MICROWIRE or Access.bus synchronous serial bus interface.

1.5.1 Reconfigurable I/O Lines

The NS486SXL supports reconfigurable I/O. For example, if the UART, interrupts, or other functions are not being used, the I/O pins associated with them can be reconfigured as general purpose bidirectional I/O pins. Up to 28 pins can be reconfigured for this purpose. This capability makes the NS486SXL extremely versatile and ideal for supporting different end product configurations with a single NS486SXL device.

1.5.2 MICROWIRE/Access.bus Interface

The NS486SXL MICROWIRE/Access.bus interface provides for full support of either the three-wire MICROWIRE or the two-wire Access.bus serial interfaces. MICROWIRE has an alternate clock phasing option that supports the SPI bus protocol as well. These industry standard interfaces permit easy interfacing to a wide range of low-cost specialty memories and I/O devices. These include EEPROMs, SRAMs, timers, clock chips, A/D converters, D/A converters, and peripheral device drivers.

1.5.3 UART Serial Port

The NS486SXL UART provides complete NS16550 (PC standard) serial communications port compatibility including the performance enhancing 16-byte deep FIFO. It performs serial-to-parallel conversion from external devices to the NS486SXL and parallel-to-serial conversion from the NS486SXL to external peripherals. Full modem control can be supported.

A serial IrDA v1.0 and HP-SIR (infrared) mode is also supported, making possible low-cost wireless communications between an NS486SXL-based system and other wireless infrared systems.

1.6 ICE SUPPORT

National Semiconductor has worked closely with Microtek International to provide hardware in-circuit emulator support for the NS486SXL. The Microtek product (PowerPack® EA-NS486) uses a special bondout version of the NS486SXL to deliver a full-featured hardware emulator that is capable of tracing on chip activity, including peripheral interrupt and I/O activity. The emulator runs at full speed, and supports overlay memory and multiple triggers.

1.7 OTHER ISSUES

NS486SXL provides a comprehensive set of on-board peripherals. Also, it is designed to easily interface to external peripherals. In addition to this ISA-like bus which supports ISA-compatible peripherals, the NS486SXL provides an interface to an external master with a shared memory space. The external master or auxiliary processor interface allows low cost interfacing to shared external memory belonging to other external masters (including another NS486SXL controller).

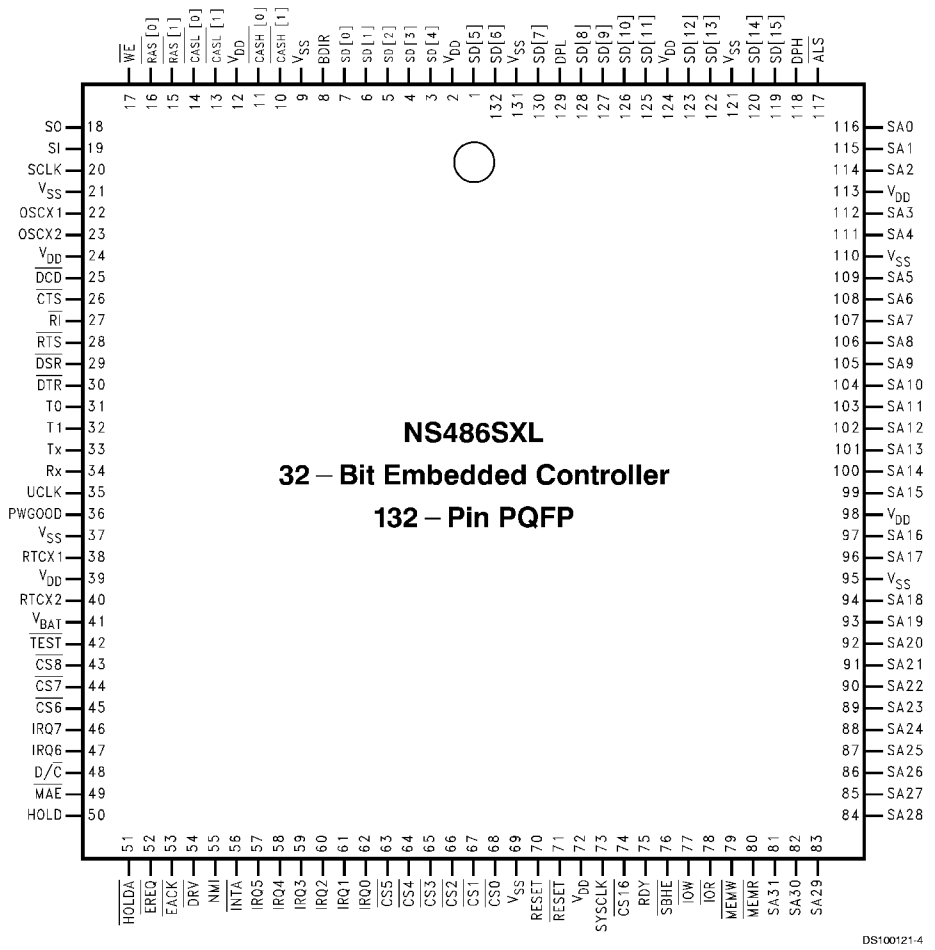
To program the resources of the NS486SXL, a set of internal control registers exists. These registers provide precise control over all internal resources and the setup of external NS486SXL control signals. It is the designer's responsibility to ensure the proper initialization of the registers in this I/O map.

In addition, the NS486SXL core processor itself requires several descriptor tables and initialization parameters that must be set by user-written start-up software.

The NS486SXL is designed from the ground up for optimum price/performance in embedded systems. This makes the NS486SXL the logical choice as the base hardware platform for executing an embedded operating system kernel such as those available from Microtec International, Wind River, ISI, QNX, and many others. Any Operating System or Real-Time Executive that will operate in a segmented or flat memory model protect mode environment is a suitable complement to the NS486SXL.

Also, there are many third party tool sets that will allow an executable application to be built to run directly on the target hardware without an O/S environment.

Connection Diagram



Note: In the above figure and in the following tables, all active low signals are shown with an overbar.

FIGURE 3. NS486SXL Package Pinout Diagram

The NS486SXL single chip controller is provided in a compact 132-pin, industry standard JEDEC PQFP package. The following tables detail the Symbol, Type, and Description of each pin. The tables divide the pins into functional groups as follows: Bus Interface Unit Pins, DRAM Control Pins, Power Pins, Reset Logic Pins, Auxiliary Processor Interface Pins, Test Pins, Interrupt Control Pins, Real Time Clock Pins, Oscillator Pins, UART/IrDA Pins, Timer Pins, 3-Wire Serial I/O Pins, External Bus Master, General Purpose Chip Select Pins, and Reconfigurable I/O Pins. Twenty-eight I/O pins are multipurpose. In their standard modes, they perform specific I/O controller functions. When those particular I/O functions are not required in the system, however, those pins can be reprogrammed to become general purpose, bidirectionsl I/O lines.

Note: In the above figure and in the following tables, all active low signals are shown with an overbar.

2.0 SXL Pin Description Tables

TABLE 1. Bus Interface Unit Pins

Symbol	Pins	Type	Function
SA[31:0]	81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 96, 97, 99, 100, 101, 102, 103, 104, 105, 106, 107, 108, 109, 111, 112, 114, 115, 116	I/O	**S**ystem **A**ddress bus. These input-output signals carry the latched address for the current access. DRAM accesses multiplex the row and column addresses for the DRAMs on the SA[12:1] pins. **Note: An incompatibility was introduced into the first silicon of the 'SXL. During Interrupt Acknowledge cycles, the internal master interrupt controller's cascade line signals, CAS[2:0], are driven onto SA[31:29], respectively. Formerly the CAS[2:0] signals were driven onto SA[25:23] in the 'SXF.** The SA[31:0] pins are inputs when an External Master is in control of the bus, except when the 'SXL does a DRAM access for the External Master (see $\overline{\text{MAE}}$, below).
SD[15:0]	119, 120, 122, 123, 125, 126, 127, 128, 130, 132, 1, 3, 4, 5, 6, 7	I/O	**S**ystem **D**ata bus: This bi-directional data bus provides the data path for all memory and I/O accesses. During transfers with 8-bit devices, the upper data byte is not used (SD[15:8]).
$\overline{\text{ALS}}$	117	O	**A**ddress **L**atch **S**trobe. This pulse is produced by a variety of bus related activities. The ALS strobe will go low every time a bus cycle is initiated by the internal CPU, even if the cycle is killed due to an internal instruction-cache "hit." The strobe will also go active for each DRAM access, and each eight-bit access for 16-to-8 bit translations by the Bus Interface Unit (BIU). The strobe will be produced for internal and external I/O accesses as well. Finally, the strobe will go active low during External Bus Master accesses so the BIU can indicate to the internal CPU that it should "snoop" an access to possibly invalidate cache entries.
$\overline{\text{SBHE}}$	76	I/O	**B**yte **H**igh **E**nable. This active-low signal is driven when the address is asserted by the CPU. External 16-bit devices should use this signal to help them determine that a data byte is to be transferred on the upper byte of the System Data bus (SD[15:8]). Eight-bit devices should ignore this signal. The 'SXL bus interface will automatically translate 16-bit requests from the internal CPU into two eight bit accesses for external memories and peripherals that do not assert $\overline{\text{CS16}}$. This pin becomes an input when an External Master is in control of the bus. An External Master should drive $\overline{\text{SBHE}}$ appropriately according to the type of access it is requesting, and be prepared to handle 8-bit devices if a 16-bit access is attempted and no $\overline{\text{CS16}}$ is produced. The 'SXL bus interface will automatically translate 16-bit accesses from the External Master into two eight-bit accesses for internal peripherals. The 'SXL will also respond with $\overline{\text{CS16}}$ on accesses to internal peripherals and accesses to any programmed Chip Select that has the "force 16-bit" feature enabled. **$\overline{\text{SBHE}}$ Truth Table** SBHE SA[0] Function 0 0 The bus master is requesting a 16-bit transfer 1 0 An 8-bit transfer on the low-byte is requested 0 1 An 8-bit transfer on the high-byte is requested 1 1 Illegal case
D/$\overline{\text{C}}$	48	O	Data/$\overline{\text{Control}}$ This output is provided to indicate what kind of access the 'SXL internal CPU is making. During the time that an External Master controls the bus, D/$\overline{\text{C}}$ will be high, indicating Data accesses. D/$\overline{\text{C}}$ is high for I/O and Memory accesses that are considered "data" by executing instructions. D/$\overline{\text{C}}$ is low for code fetches from memory, interrupt acknowledge cycles and Halt/Special bus events.

2.0 SXL Pin Description Tables (Continued)

TABLE 1. Bus Interface Unit Pins (Continued)

Symbol	Pins	Type	Function
BDIR	8	O	**B**uffer **DIR**ection. This output is provided to reduce external logic if an external data-bus buffer is required in the user's design. The BDIR signal is high whenever the buffer should be driving from the 'SXL pins out to the buffered ISA-like bus. BDIR also works correctly if an External Master is designed into the system, however, the External Master must always be on the buffered side of the bus in this case. BDIR will only go low during reads from the buffered bus, or accesses to internal peripherals or DRAM by an External Master.
$\overline{IOR}$	78	I/O	**IO R**ead command. This active-low signal instructs an I/O device to place data onto the system data bus. An input when an External Master controls the bus.
$\overline{IOW}$	77	I/O	**IO W**rite command. This active-low signal indicates to an I/O device that a write operation is in process on the system bus. An input when an External Master controls the bus.
$\overline{MEMR}$	80	I/O	**MEM**ory **R**ead command. This active-low signal instructs a memory mapped device to place data onto the system data bus. An input when an External Master controls the bus.
$\overline{MEMW}$	79	I/O	**MEM**ory **W**rite command. This active-low signal indicates to a memory mapped device that a write operation is in process on the system bus. An input when an External Master controls the bus.
$\overline{CS16}$	74	I/O	**C**hip **S**elect **16**-bit. This active-low feedback signal indicates that the device being accessed is a 16-bit device. This signal should be pulled-up and driven by external devices with an open collector driver. If a chip select is programmed to force 16-bit accesses, this signal will be asserted (low) during the access. When an External Master controls the bus, the 'SXL will also drive this signal low for accesses to internal peripherals or DRAM.
$\overline{RDY}$	75	I/O	**R**ea**DY**. An external device may drive this signal inactive low to insert wait states and extend the external bus cycle. This signal should be pulled-up and driven with an open collector or be TRI-STATE driven. When an External Master controls the bus, it must honor the $\overline{RDY}$ signal as the 'SXL will drive this signal low as appropriate for accesses to internal peripherals or DRAM and bus snooping.

TABLE 2. External Bus Master Interface Pins

Symbol	Pins	Type	Function
HOLD	50	I	**HOLD** Request from External Master. The external master will assert this signal high in order to request the bus from the 'SXL CPU. The external master can hold the bus indefinitely, so care should be taken to ensure that the HOLD is released in time for the CPU to service any real-time requirements (e.g. Interrupts, etc.).
$\overline{HLDA}$	51	O	**HoLD A**cknowledge from 'SXL. When the 'SXL CPU grants the bus to an external master, then this signal is asserted (low). Once $\overline{HLDA}$ is asserted, the external master is responsible for driving the address and control signals ($\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$, $\overline{IOW}$, $\overline{SBHE}$) on the bus. If there are bi-directional buffers on the address and control lines, then $\overline{HLDA}$ should be used to set the direction of the buffers.
$\overline{MAE}$	49	O	**M**aster **A**ddress **E**nable. During $\overline{HLDA}$, if the 'SXL requires that the External Master TRI-STATE its addresses (e.g. to complete a DRAM access) then $\overline{MAE}$ will be de-asserted (high). $\overline{MAE}$ should be used to control the External Master's TRI-STATE address lines or for the enable of the bi-directional address bus buffer chips. $\overline{MAE}$ will normally be asserted (low).

TABLE 3. DRAM Control Pins

2.0 SXL Pin Description Tables (Continued)

TABLE 3. DRAM Control Pins (Continued)

Symbol	Pins	Type	Function
$\overline{RAS}$[1:0]	15, 16	O	**R**ow **A**ddress **S**trobe. On the falling edge of these active-low signals, Bank 1 and Bank 0 respectively, should latch in the row address off of SA[12:1]. If only one bank of DRAM is supported, $\overline{RAS0}$ will support that bank and $\overline{RAS1}$ will be unused
$\overline{CASH}$[1:0]	10, 11	O	**C**olumn **A**ddress **S**trobe (**H**igh Byte). These active-low signals indicate when the column access is being made to the high byte of DRAM Bank 1 and DRAM Bank 0 respectively. If only one bank of DRAM is supported, $\overline{CASH0}$ will support the high byte of that bank and $\overline{CASH1}$ will be unused.
$\overline{CASL}$[1:0]	13, 14	O	**C**olumn **A**ddress **S**trobe (**L**ow Byte). These active-low signals indicate when the column access is being made to the low byte of DRAM Bank 1 and DRAM Bank 0, respectively. If only one bank of DRAM is supported, $\overline{CASL0}$ will support the low byte of that bank and $\overline{CASL1}$ will be unused.
$\overline{WE}$	17	O	**W**rite **E**nable. Active low signal for write operations on DRAM.
DPH, DPL	118, 129	I/O	DRAM **D**ata **P**arity. DRAM data parity may be enabled or disabled; if disabled these two pins will be unused. Otherwise, for DRAM writes the SXL's DRAM Controller will generate odd parity and drive the odd parity onto these two pins. For DRAM reads the SXL's DRAM Controller will read the values driven on these two pins and check it for odd parity in association with the appropriate data byte.

TABLE 4. Power Pins

Symbol	Pins	Type	Function
V_{DD}	2, 12, 24, 39, 72, 98, 113, 124	Power	+5V power to core and I/O.
V_{SS}	9, 21, 37, 69, 95, 110, 121, 131	Ground	Ground to core and I/O.

TABLE 5. Reset Logic Pins

Symbol	Pins	Type	Function
RESET	70	O	**RESET** system output driver: This active high signal resets or initializes system peripheral logic during power up (PWGOOD) or due to a WATCHDOG Reset.
$\overline{RESET}$	71	O	Inverse of **RESET** for peripherals requiring active low reset.
PWGOOD	36	I	**P**o**W**er **GOOD**. This active-high (schmitt trigger) input will cause a hardware reset to the NS486SXL whenever this input goes low. This pin will typically be driven by the power supply and PWGOOD will remain low until the power supply determines that stable and valid voltage levels have been achieved.

TABLE 6. General Purpose Chip Select Pins

Symbol	Pins	Type	Function
$\overline{CS}$[0]	68	O	**C**hip **S**elect **0**: This output is used as the chip-select for the system boot ROM. It defaults to the upper 64k Bytes of memory.
$\overline{CS}$[8:1]	43, 44, 45, 63, 64, 65, 66, 67	O	**C**hip **S**elect **1 to 8**. These pins can be programmed to be either memory or I/ O mapped chip selects, which are used for glueless connection to external peripherals.

2.0 SXL Pin Description Tables (Continued)

TABLE 7. Auxiliary Processor Interface Pins

Symbol	Pins	Type	Function
$\overline{\text{EREQ}}$	52	O	**E**xternal bus **REQ**uest (active-low) to an auxiliary processor. This signal is asserted whenever the auxiliary processor feature of a programmable chip select is enabled. This is used to request access to a shared memory from another processor.
$\overline{\text{EACK}}$	53	I	**E**xternal bus **ACK**nowledge (active-low) from an auxiliary processor.
$\overline{\text{DRV}}$	54	O	Auxiliary processor shared memory **DR**i**V**e control signal. Once access is granted to the shared memory, this signal is asserted to enable the address, data and control signal buffers to drive the shared memory pins.

TABLE 8. Test Pins

Symbol	Pins	Type	Function
$\overline{\text{TEST}}$	42	I	Reserved for testing and development system support. Normally pulled high. A small number of test modes are documented for use by the customer. While $\overline{\text{TEST}}$ is asserted, all output pins except OSCX2 and RTCX2 are TRI-STATE.

TABLE 9. Interrupt Control Pins

Symbol	Pins	Type	Function
NMI	55	I	**N**on-**M**askable **I**nterrupt. This active-high signal will generate a non-maskable interrupt to the CPU when it is active high. Normally this signal is used to indicate a serious system error.
$\overline{\text{INTA}}$	56	O	**INT**errupt **A**cknowledge. During each interrupt acknowledge cycle this signal will strobe low; it should be used by external cascaded interrupt controllers.
IRQ[7:0]	46, 47, 57, 58, 59, 60, 61, 62	I	**I**nterrupt **Re**ques**t**s. These inputs are either rising edge or low-level sensitive interrupt requests, depending on the configuration of the internal interrupt controllers. These interrupt requests may also be programmed to support externally cascaded interrupt controller(s). The IRQ pins are also used to select a particular test in test mode.

TABLE 10. Real Time Clock Pins

Symbol	Pins	Type	Function
RTCX1	38	I	**R**eal **T**ime **C**lock crystal oscillator input: 32 kHz crystal.
RTCX2	40	O	**R**eal **T**ime **C**lock crystal oscillator output: 32 kHz crystal.
Vbat	41	I	External + battery input for real time clock.

TABLE 11. Oscillator Pins

Symbol	Pins	Type	Function
SYSCLK	73	O	**SYS**tem **CL**oc**K**. This clock output pin will either be driven with a signal half the frequency of the OSCX1 input clock frequency or the CPU's clock frequency, which is determined in the Power Management Control Register 1. The source selection for this signal is determined by bit 1 of the Power Management Control Register 3.
OSCX1	22	I	**OSC**illator Crystal **1** input. This pin should either be driven by a TTL oscillator or be connected to an external crystal circuit. This signal is the fundamental clock source for all clocked elements in the NS486SXL, except the Real-Time Clock, which has its own crystal pins.

2.0 SXL Pin Description Tables (Continued)

TABLE 11. Oscillator Pins (Continued)

Symbol	Pins	Type	Function
OSCX2	23	O	**OSC**illator Crystal **2** output. This is the output side of the NS486SXL on-chip circuitry provided to support an external crystal circuit. If a TTL oscillator drives OSCX1, this pin should be a no connect.

TABLE 12. 16550 UART Pins

Symbol	Pins	Type	Function
Tx	33	O	UART **T**ransmit data. In IrDA and HP-SIR mode this pin is the UART out-put encoded for the serial infrared link. Otherwise it is the transmit output of the 16550 UART.
Rx	34	I	UART **R**eceive data. In IrDA and HP-SIR mode this pin is routed through the serial infrared decoder. Otherwise, it is the receive input to the 16550.
UCLK	35	O	**U**art **CL**oc**K**. Output of programmable rate UART/MODEM clock. Typically used for the Infrared Modulator.
$\overline{RTS}$	28	O	**R**equest **T**o **S**end. When low, this signal informs the MODEM or data set that the UART is ready to exchange data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 2 (RTS) of the MODEM Control Register. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{DSR}$	29	I	**D**ata **S**et **R**eady. When low, it indicates that the MODEM or data set is ready to link with the UART. The $\overline{DSR}$ signal is a MODEM status input whose condition can be tested by reading bit 5 (DSR) of the MODEM Status Register. Bit 5 is the complement of the $\overline{DSR}$ signal. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register. **Note:** Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.
$\overline{DTR}$	30	O	**D**ata **T**erminal **R**eady. When low, this signal informs the MODEM or data set that the UART is ready to establish a communications link. The $\overline{DTR}$ output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. A Master Reset operation sets this signal to its inactive (high) state. Loop mode operation holds this signal in its inactive state.
$\overline{DCD}$	25	I	**D**ata **C**arrier **D**etect. When low, this input signal indicates that the data carrier has been detected by the MODEM or data set. The $\overline{DCD}$ signal is a MODEM status input whose condition can be tested by reading bit 7 (DCD) of the MODEM Status Register. Bit 7 is the complement of the $\overline{DCD}$ signal. Bit 3 (DDCD) of the MODEM Status Register indicates whether the $\overline{DCD}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{DCD}$ has no effect on the receiver. **Note:** Whenever the DCD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled
$\overline{CTS}$	26	I	**C**lear **T**o **S**end. When low, this input signal indicates that the MODEM or data set is ready to exchange data. The $\overline{CTS}$ signal is a MODEM status input whose conditions can be tested by reading bit 4 (CTS) of the MODEM Status Register. Bit 4 is the complement of the $\overline{CTS}$ signal. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register. $\overline{CTS}$ has no effect on the Transmitter. **Note:** Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

2.0 SXL Pin Description Tables (Continued)

TABLE 12. 16550 UART Pins (Continued)

Symbol	Pins	Type	Function
$\overline{RI}$	27	I	**R**ing **I**ndicator. When low, this input signal indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM status input whose condition can be tested by reading bit 6 (RI) of the MODEM Status Register. Bit 6 is the complement of the $\overline{RI}$ signal. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input signal has changed from a low to high state since the previous reading of the MODEM Status Register. **Note:** Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled. **Note:** Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

TABLE 13. Timer Pins

Symbol	Pins	Type	Function
T0	31	I/O	Programmable **T**imer pin **0**. This Bidirectional pin may be selected to control one of the following four functions via bits 1-0 of the Timer I/O Control Register: 1) The GATE input into Timer 0. 2) The GATE input into Timer 1. 3) The OUT output from Timer 0. 4) The CLK input into Timer 1.
T1	32	I/O	Programmable **T**imer pin **1**. This Bidirectional pin may be selected to control one of the following four functions via bits 3-2 of the Timer I/O Control Register: 1) The GATE input into Timer 0. 2) The GATE input into Timer 1. 3) The OUT output from Timer 1. 4) The CLK input into Timer 0.

TABLE 14. 3-Wire Serial I/O Pins

Symbol	Pins	Type	Function
SO	18	I/O	The **S**erial data **O**utput signal for MICROWIRE.
SI	19	I/O	The **S**erial data **I**nput signal for MICROWIRE or the serial data I/O for Access.bus.
SCLK	20	O	The **S**erial **CL**oc**K** signal for MICROWIRE and Access.bus.

Note 1: For MICROWIRE Slave Mode, a pin must be selected to be the Chip Select Input.

Absolute Maximum Ratings (Notes 3, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{DD}, V_{DDA}	−0.5V to +7.0V
Input Voltage, V_I	−0.5V to V_{DD} +0.5V
Output Voltage, V_O	−0.5V to V_{DD} +0.5V
Storage Temperature, T_{STG}	−65˚C to +165˚C
Lead Temperature, T_L	
Soldering (10 seconds)	+260˚C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage, V_{DD}	4.75	5.0	5.25	V
Operating Temperature, T_A	0		+70	˚C
ESD Tolerance	2000			V
C_{ZAP} = 100 pF				
R_{ZAP} = 1.5 kΩ				
(Note 4)				

Capacitance

T_A = 25˚C, f = 1 MHz

Symbol	Parameter	Condition	Min	Typ	Max	Units
C_{IN}	Input Pin Capacitance			5	7	pF
C_{IN1}	Clock Input Capacitance			8	10	pF
C_{IO}	I/O Pin Capacitance			10	12	pF
C_O	Output Pin Capacitance			6	8	pF

DC Characteristics

(Under Recommended Operating Conditions)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input High Voltage		2.0		V_{DD}	V
V_{IL}	Input Low Voltage		-0.5		0.8	V
I_{CC}	V_{DD} Average Supply Current	V_{IL} = 0.5V, V_{IH} = 2.4V No Load				mA

Note 2: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 3: Unless otherwise specified all voltages are referenced to ground.

Note 4: Value based on test complying with NSC SOP5-028 human body model ESD testing using the ETS-910 tester.

External Bus

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −6 mA (Nch Quiet-drive) or I_{OH} = −24 mA (High-drive) on: SA12-1, DP1-0, SD15-0 I_{OH} = −12 mA on: SA0, SA25-13 [SA0 - min. 10 kΩ pullup] (Note 5)	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 20 mA on: SA12-1, DP1-0, SD15-0 I_{OL} = 12 mA on: SA0, SA25-13, $\overline{BHE}$		0.4	V

Note 5: Max load on SA12-1 is 50 pF, and SD0–15 is 50 pF.

DRAM Control Unit

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −6 mA (Nch Quiet-drive) or I_{OH} = −24 mA (High-drive) on: $\overline{RAS}$0–1, $\overline{CASH}$0–1, $\overline{CASL}$0–1, $\overline{WE}$ (Note 6)	2.4		V

DRAM Control Unit (Continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output Low Voltage	I_{OL} = 20 mA on: $\overline{RAS}$1–0, $\overline{CASH}$1–0, $\overline{CASL}$1–0, $\overline{WE}$ (Note 7)		0.4	V

Note 6: Max load $\overline{RAS}$1–0. $\overline{CASH}$1–0, and $\overline{CASL}$1–0 is 63 pF.

Note 7: Max load on $\overline{WE}$ is 50 pF.

Auxiliary Processor Interface

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –6 mA on: $\overline{EACK}$ I_{OH} = –4 mA on: $\overline{DRV}$, $\overline{EREQ}$	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = –6 mA on: $\overline{EACK}$ I_{OL} = –4 mA on: $\overline{DRV}$, $\overline{EREQ}$		0.4	V

IrDA Infra Red/UART

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –100 µA I_{OH} = –6 mA on: Tx, UCLK, Rx	V_{CC} - 0.2 2.4		V V
V_{OL}	Output Low Voltage	I_{OL} = –100 µA I_{OL} = 6 mA on: Tx, UCLK, Rx		0.2 0.4	V V

External Bus Control

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –12 mA on: $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$ RESET, $\overline{RESET}$, $\overline{CS16}$, $\overline{BHE}$ [$\overline{CS16}$ - min. 10 kΩ pullup]	2.4		V
V_{OL}	Output Low Voltage	I_{OH} = 12 mA on: $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$ RESET, $\overline{RESET}$, $\overline{CS16}$, $\overline{BHE}$		0.4	V

Oscillator (CPUX1/CLK)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –12 mA on: SYSCLK	2.4		V
V_{OL}	Output Low Voltage	I_{OH} = 12 mA on: SYSCLK		0.4	V
V_{IH}	OSCX1 Input High Voltage	(Note 8)	2.0		
V_{IL}	OSCX2 Input Low Voltage			0.4	V

Note 8: OSCX2 is the output.

Real Time Clock (RTCX1/CLK)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	RTCX1 Input High Voltage	(Note 9)	2.0		
V_{IL}	RTCX1 Input Low Voltage			0.4	V
V_{BAT}	Battery Voltage	(Note 10)	2.4		V
I_{BAT}	Battery Current				

Note 9: RTCX2 is the output.

Note 10: Lithium Battery.

Timer

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –6 mA on: T0, T1	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 6 mA on: T0, T1		0.4	V

General Purpose Chip Selects

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –6 mA on: $\overline{CS}$5–0	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 6 mA on: $\overline{CS}$5–0		0.4	V

Interrupt Controller

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –12 mA on: $\overline{INTA}$	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA on: $\overline{INTA}$		0.4	V

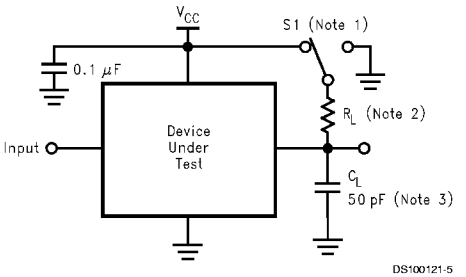
3-Wire I/O (and Access.bus)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = –12 mA on: SO, SI, SCLK	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA on: SO, SI, SCLK		0.4	V

General AC Specifications

AC TEST CONDITIONS

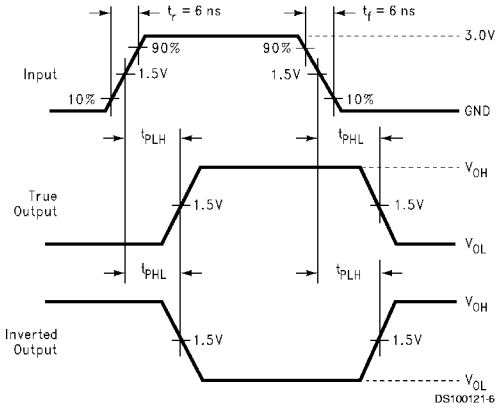
Test Circuit for Output Tests



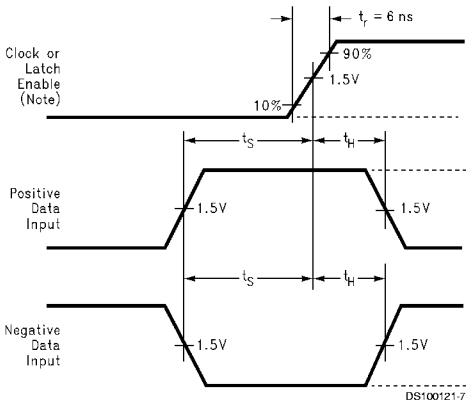
Note 1: $S_1 = V_{CC}$ for t_{PZL}, anf t_{PLZ} measurements.
S_1 = GND for t_{PZH}, and t_{PHZ} measurements
S_1 = Open for push pull outputs
Note 2: R_L = 1.1k
Note 3: C_L includes scope and jig capacitance

General AC Specifications (Continued)

Propagation Delay Waveforms

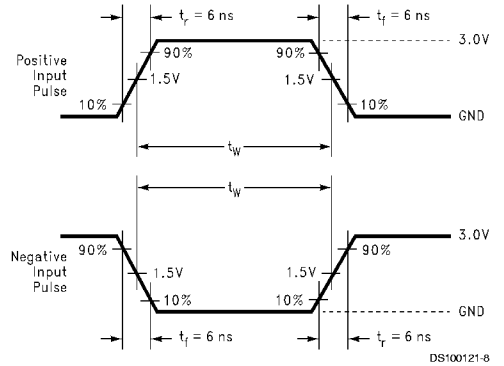


Setup and Hold Time Waveforms



Note: Waveform for negative edge sensitive circuits will be inverted.

Input Pulse Width Waveforms Except for Clock Pins



TRI-STATE Output Enable and Disable Waveforms

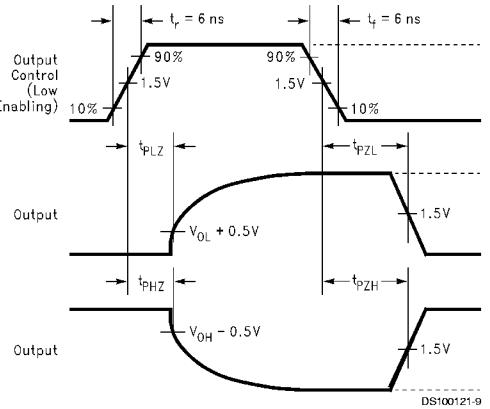
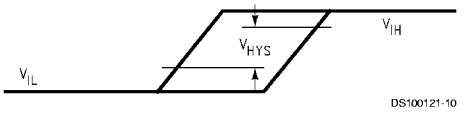


FIGURE 4. Switching Characteristic Measurement Waveforms



V_{HYS} = 200 mV
Switching thresholds not specified

FIGURE 5. More Switching Specifications

Power Ramp Times

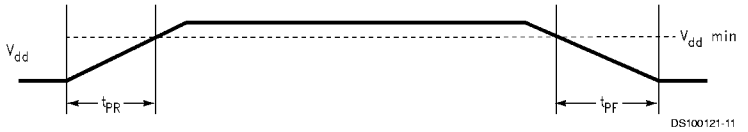


FIGURE 6. Power Supply Rise and Fall

Power Ramp Times (Continued)

TABLE 15. V_{DD} Rise and Fall Times

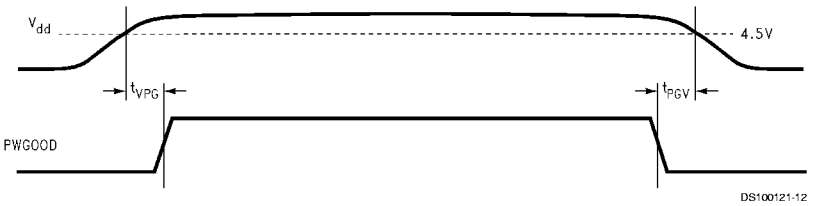
Symbol	Parameter	Min	Max	Units
t_{PF}	V_{DD} Falling Time from 4.5V to 0V	5		ms
t_{PR}	V_{DD} Rising Time from 0V to 4.5V	5		ms

Note 11: The rising/falling rate is assumed linear.

PWRGOOD and Power Rampdown Timing

TABLE 16. V_{DD} Rampdown vs PWRGOOD

Symbol	Parameter	Min	Max	Units
t_{VPG}	V_{DD} (4.5V) to PWGOOD High	1		µs
t_{PGV}	PWGOOD Falling to V_{DD} (4.5V)	1		µs



Note: The rising/falling rate is assumed linear.

FIGURE 7. PWGOOD in Relation to V_{DD}

AC Switching Specifications

The following pages list some of the preliminary AC Specifications for the NS486SXL. All parameters are listed in alphabetical order according to their Symbol.

The Tables consist of the following:

Parameter— A short description of the specification being documented.

Symbol— A quick reference between the timing diagram and the Table entries.

Formula— An equation, which in addition to the Minimum and Maximum Specifications can be used to determine the actual timing provided at any operating frequency.

Min— Minimum Specification when added to the value produced by the formula.

Max— Maximum Specification when added to the value produced by the formula.

How to calculate the actual specification at a given frequency:

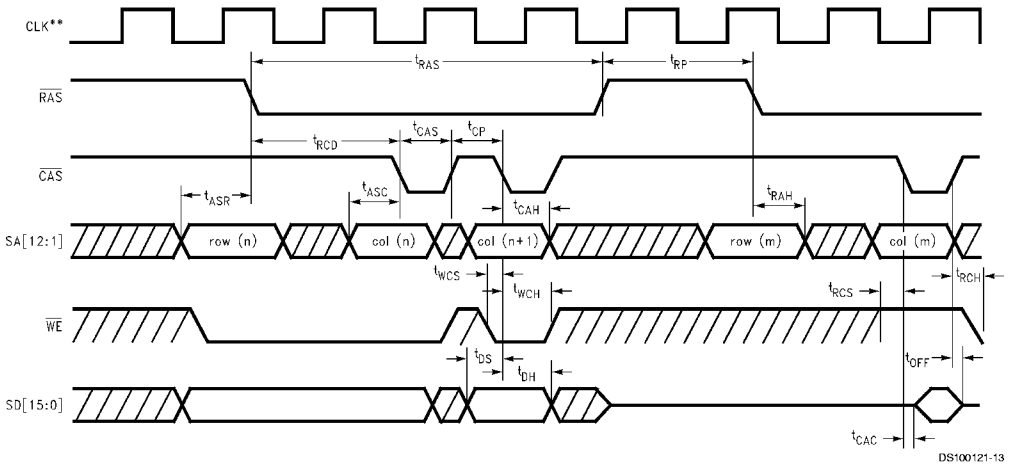
In the formula column, one will see many formulae, which contain the variable T. The T represents one period (or one T-state) of the CPU Clock. So if the CPU is running at 25 MHz, T is equavalent to 40 ns; similarly if the CPU is running at 20 MHz, T is equavalent to 50 ns.

EXAMPLE: Calculate the minimum guaranteed Column Address Setup Time.

At 25 MHz	Formula + Min Spec	=
	(0.5T) + (–20 ns)	=
	0.5 (40 ns) + (–20 ns)	=
	20 ns - 20 ns	= 0 ns
At 20 MHz	Formula + Min Spec	=
	(0.5T) + (–20 ns)	=
	0.5 (50 ns) + (–20 ns)	=
	25 ns - 20 ns	= 5 ns

As the frequency varies, so will many of the specifications. One should always calculate the specification based on the CPU's operating frequency.

DRAM Interface Timing Specification



**The CLK signal is only included as a reference; no specifications are guarantee to this signal.

FIGURE 8. DRAM Timing Diagram

TABLE 17. 4 Cycle Page Miss Preliminary Specifications

Symbol	Parameter	Formula	Min	Max
t_{ASC}	Column Address Setup Time	0.5T +	−20	
t_{ASR}	Row Address Setup Time	0.5T +	−20	
t_{CAC}	Access Time from CAS	0.5T +		−5
t_{CAH}	Column Address Hold Time	0.5T +	−5	
t_{CAS}	$\overline{CAS}$ Pulse Width	0.5T +	0	10
t_{CP}	Page Mode $\overline{CAS}$ Precharge	0.5T +	−10	
t_{DH}	Write Data Hold Time	0.5T +	−5	
t_{DS}	Write Data Setup Time	0.5T +	−20	
t_{OFF}	Read Data Valid Hold Time		0	
t_{RAS}	$\overline{RAS}$ Pulse Width	2.5T +	−15	Progr'm'ble
t_{RAH}	Row Address Hold Time	0.5T +	−10	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	1.5T +	−20	
t_{RCH}	Read Command Hold Time		0	
t_{RCS}	Read Command Setup Time	0.5T +	−20	
t_{RP}	$\overline{RAS}$ Precharge Time	1.5T +	−10	
t_{WCH}	Write Command Hold Time	0.5T +	−5	
t_{WCS}	Write Command Setup Time	0.5T +	−20	

TABLE 18. 3 Cycle Miss Preliminary Specifications

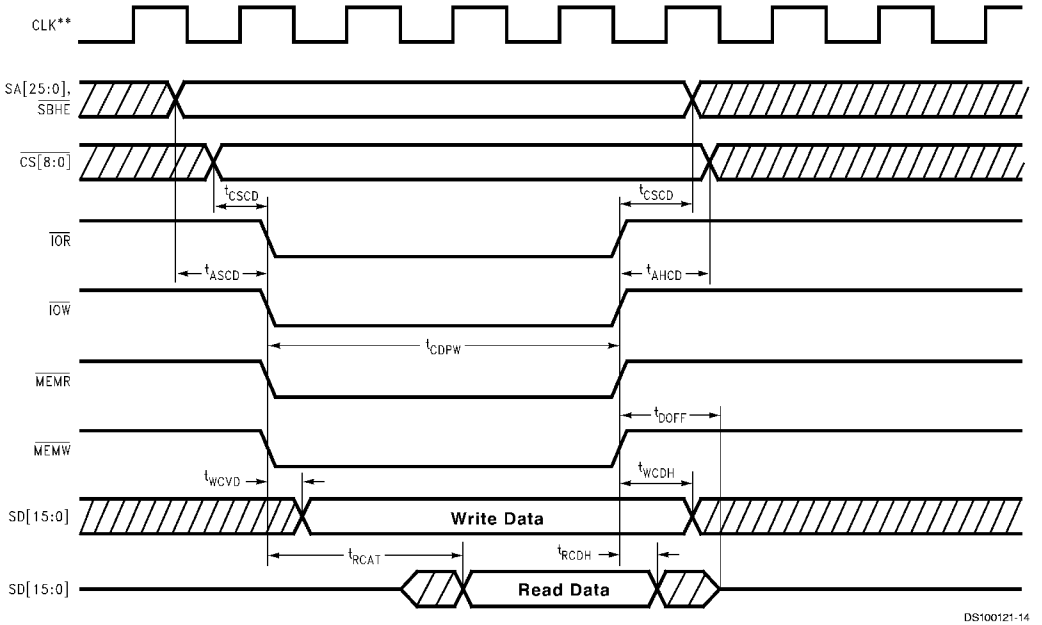
Symbol	Parameter	Formula	Min	Max
t_{ASC}	Column Address Setup Time	0.5T +	−20	
t_{ASR}	Row Address Setup time	0.5T +	−20	
t_{CAC}	Access Time from $\overline{CAS}$	0.5T +		−5
t_{CAH}	Column Address Hold Time	0.5T +	−5	
t_{CAS}	$\overline{CAS}$ Pulse Width	0.5T +	0	10
t_{CP}	Page Mode $\overline{CAS}$ Precharge	0.5T +	−10	
t_{DH}	Write Data Hold Time	0.5T +	−5	
t_{DS}	Write Data Setup Time	0.5T +	−20	

DRAM Interface Timing Specification (Continued)

TABLE 18. 3 Cycle Miss Preliminary Specifications (Continued)

Symbol	Parameter	Formula	Min	Max
t_{OFF}	Read Data Valid Hold Time		0	
t_{RAS}	$\overline{RAS}$ Pulse Width	2.0T +	–15	PROG
t_{RAH}	Row Address Hold Time	0.5T +	–10	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	1.0T +	–20	
t_{RCH}	Read Command Hold Time		0	
t_{RCS}	Read Command Setup Time	0.5T +	–20	
t_{RP}	$\overline{RAS}$ Precharge Time	1.0T +	0	
t_{WCH}	Write Command Hold Time	0.5T +	–5	
t_{WCS}	Write Command Setup Time	0.5T +	–20	

ISA-like Bus Cycles Timing Specification



**The CLK signal is only included as a reference; no specifications are guarantee to this signal.

FIGURE 9. ISA-like Bus Timing Diagram

TABLE 19. No Command Delay ISA-like Bus Specifications

Symbol	Parameter	Formula	Min	Max
t_{AHCD}	Address Hold Time from $\overline{CMD}$	1.0T +	–20	
t_{ASCD}	Address Setup Time to $\overline{CMD}$	1.0T +	–20	
t_{CDPW}	Command Pulse Width	1.0T + (Wait)T +	–10	
t_{CHCD}	Chip Select Hold Time from $\overline{CMD}$	1.0T +	–25	
t_{CSCD}	Chip Select Setup Time to $\overline{CMD}$	1.0T +	–40	
t_{DOFF}	Read Data TRI-STATE	1.0T +		–25
t_{RCAT}	Read $\overline{CMD}$ Data Access Time	1.0T + (Wait)T +		–30

ISA-like Bus Cycles Timing Specification (Continued)

TABLE 19. No Command Delay ISA-like Bus Specifications (Continued)

Symbol	Parameter	Formula	Min	Max
t_{RCDH}	Read $\overline{CMD}$ Data Hold Time		0	
t_{WCDH}	Write $\overline{CMD}$ Data Hold Time	1.0T +	−25	
t_{WCVD}	Write $\overline{CMD}$ to Valid Data			5
t_{WCS}	Write Command Setup Time	0.5T +	−20	

Note 12: The value of (Wait) in the above formulae, is the number of programmed wait states associated with that access cycle (default value is 7, but may be programmed to 0–7).

TABLE 20. One Programmed Command Delay ISA-like Bus Specifications

Symbol	Parameter	Formula	Min	Max
t_{AHCD}	Address Hold Time from $\overline{CMD}$	1.0T +	−20	
t_{ASCD}	Address Setup Time to $\overline{CMD}$	2.0T +	−20	
t_{CDPW}	Command Pulse Width	1.0T + (Wait)T +	−10	
t_{CHCD}	Chip Select Hold Time from $\overline{CMD}$	1.0T +	−25	
t_{CSCD}	Chip Select Setup Time to $\overline{CMD}$	2.0T +	−40	
t_{DOFF}	Read Data TRI-STATE	1.0T +		−25
t_{RCAT}	Read $\overline{CMD}$ Data Access Time	1.0T + (Wait)T +		−30
t_{RCDH}	Read $\overline{CMD}$ Data Hold Time		0	
t_{WCDH}	Write $\overline{CMD}$ Data Hold Time	1.0T +	−25	
t_{WCVD}	Write Valid Data to CMD (Note 14)	1.0T +	−5	
t_{WCS}	Write Command Setup Time	0.5T +	−20	

Note 13: The value of (Wait) in the above formulae, is the number of programmed wait states associated with that access cycle (default value is 7, but may be programmed to 0–7).

Note 14: For this case Valid Write Data Sets-up to the leading edge of the Command Strobe.

Ready Feedback Timing Specifications

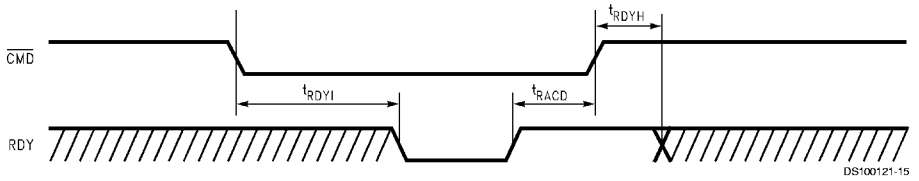


FIGURE 10. Ready Feedback Timing Diagram

TABLE 21. Ready Signal Timing Specifications

Symbol	Parameter	Formula	Min	Max
t_{RACD}	RDY Active to $\overline{CMD}$ Rising	(E_RDY)T +	0	
t_{RDYH}	RDY Hold Time from $\overline{CMD}$		0	
t_{RDYL}	$\overline{CMD}$ to RDY Inactive Feedback	1.0T + (Wait)T +		−30

Note 15: The value of (Wait) in the above formulae, is the number of programmed wait states associated with that access cycle (default value is 7, but may be programmed to 0–7). The value of (E_RDY) in the above formulae, is the number of programmed extended ready states associated with every access cycle (default number is 2, but may be programmed to 0–2).

OSCX1 AC Specification

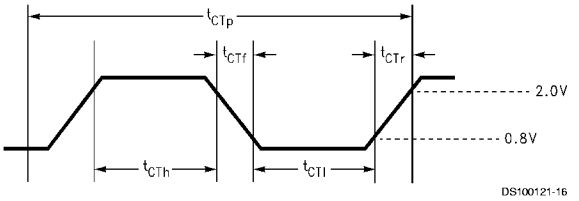


FIGURE 11. TTL Clock Input Timing Diagram

TABLE 22. TTL Clock Input Specification

Symbol	Parameter	Min	Max	Units
t_{CTp}	CTTL Clock Period	40	870	ns
t_{CTh}	CTTL High Time (Note 16)	(0.5 x t_{CTp}) - 4		ns
t_{CTl}	CTTL Low Time (Note 16)	(0.5 x t_{CTp}) - 4		ns
t_{CTr}	CTTL Rise Time		4	ns
t_{CTf}	CTTL Fall Time		4	ns

Note 16: Except for the cycle in which the core frequency is changed. In this cycle, t_{CTh} and t_{CTl} relate to different t_{CTp} cycles.

PIC AC Specs

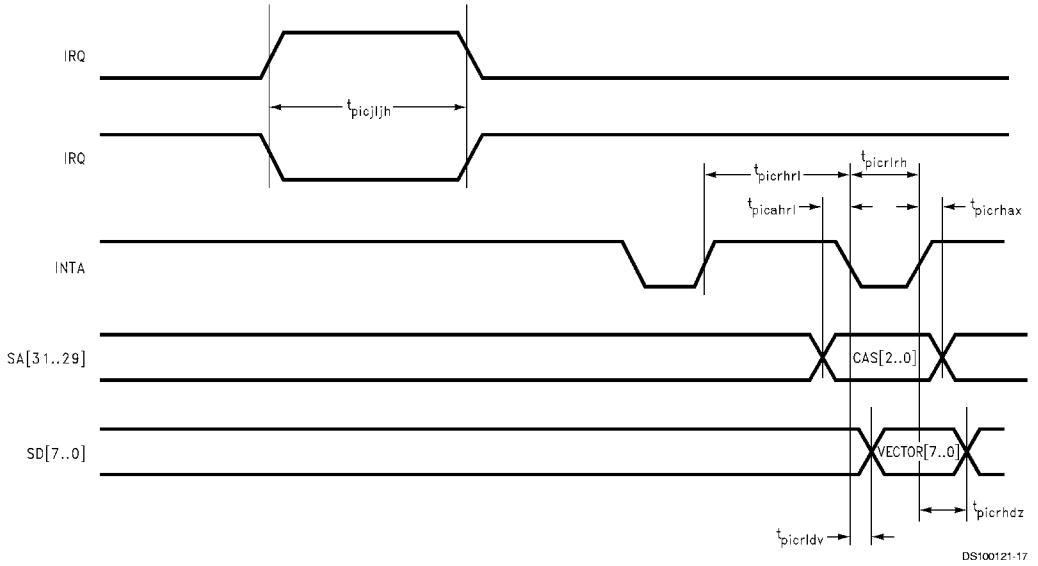


FIGURE 12. PIC Timing Diagram

TABLE 23. PIC Timing Specifications

Symbol	Parameter	Min	Typ	Max
$t_{picjljh}$		100		
$t_{picahrl}$		0		

PIC AC Specs (Continued)

TABLE 23. PIC Timing Specifications (Continued)

Symbol	Parameter	Min	Typ	Max
$t_{picrlrh}$		235		
$t_{picrhax}$		0		
$t_{picrldv}$				200
$t_{picrhdz}$		10		
$t_{picrhrl}$		100		

MICROWIRE (3-Wire) and Access.bus

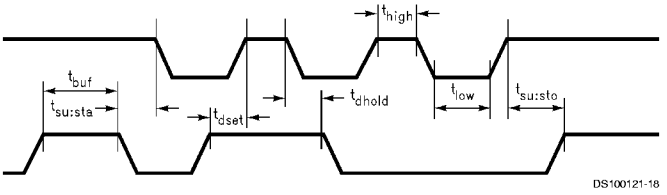


FIGURE 13. Access.bus Timing Diagram

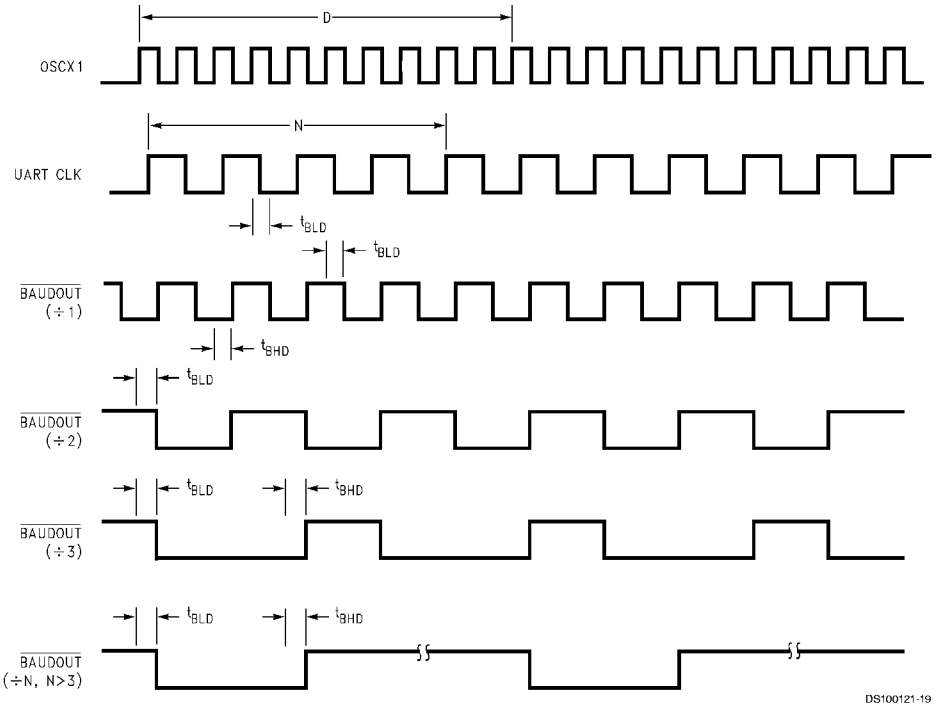
TABLE 24. Access.Bus Timing Specifications

Symbol	Parameter	Formula	Min	Max
t_{sclk}	SCLK Clock Frequency			100 kHz
t_{buf}	Bus Free Time between STOP and START Condition		4.7 µs	
t_{flow}	Low Period of the SCLK Clock		4.7 µs	
t_{high}	High Period of the SCLK Clock		4.0 µs	
t_{dhold}	Data Hold Time		250	
t_{dset}	Data Setup Time		250	
$t_{su:sto}$	Setup Time for STOP Condition		4.0 µs	
$t_{su:sta}$	Hold Time for START Condition		4.7 µs	

FIFO UART

Symbol	Parameter	Conditions	Min	Max	Units
D	OSC Clock Divider		1	63	CLKs
N	Baud Divisor		1	65535	CLKs
t_{BHD}	Baud Output Positive Edge Delay			56	ns
t_{BLD}	Baud Output Negative Edge Delay			56	ns

FIFO UART (Continued)



Symbol	Parameter	Conditions	Min	Max	Units
t_{IRTXW}	IRTX Pulse Width		1.6 µs	3/16	BAUD OUT Cycles
t_{IRRXW}	IRRX Pulse Width		1.6 µs	6/16	BAUD OUT Cycles

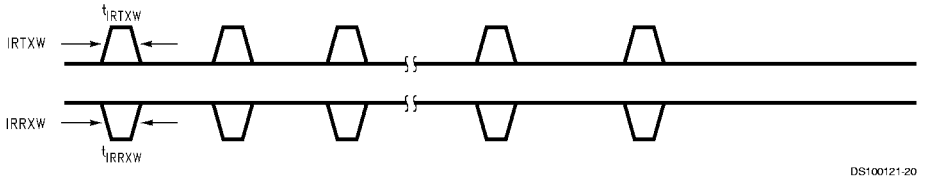


FIGURE 14. UART Baud Rate and Infrared Clocks

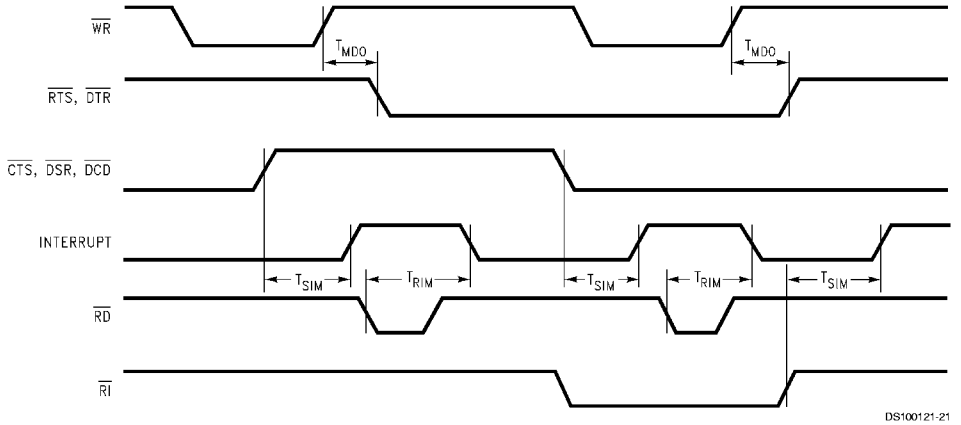
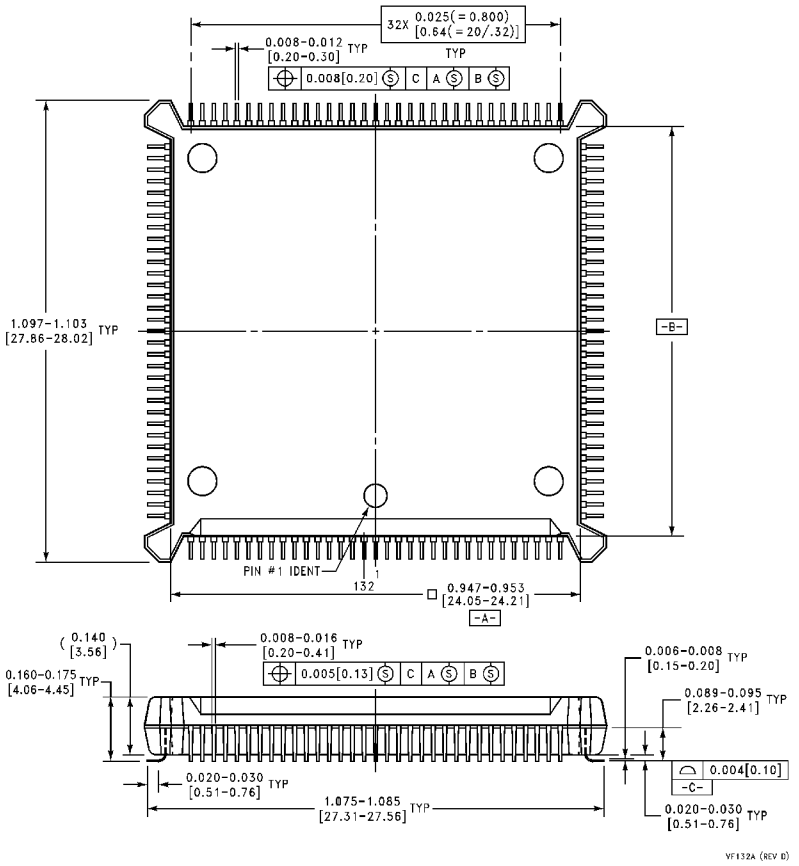


FIGURE 15. UART MODEM Control Timing

Physical Dimensions inches (millimeters) unless otherwise noted



132-Lead Plastic Quad Flatpak JEDEC (VUL)
Order Number NS486SXLVUL
NS Package Number VUL132A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179