SN74AVC8T245-Q1 8-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs

1 Features

- Qualified for Automotive Applications
- AEC Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to +125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Control Inputs V_{IH} and V_{IL} Levels Are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, All I/O Ports Are in the High-Impedance State
- I_{off} Supports Partial Power-Down-Mode Operation
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.4-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- Maximum Data Rates
  - 170 Mbps (V_{CCA} < 1.8 V or V_{CCB} < 1.8 V)
  - 320 Mbps (V_{CCA} ≥ 1.8 V and V_{CCB} ≥ 1.8 V)
- Latch-Up Performance Exceeds 100 mA per JESD 78, Class II

2 Applications

- Telematics
- Cluster
- Head Unit
- Navigation Systems

3 Description

The SN74AVC8T245-Q1 is an 8-bit noninverting bus transceiver that uses two separate configurable power-supply rails. The SN74AVC8T245-Q1 operation is optimimal with V_{CCA} and V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA} and V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC8T245 design enables asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. One can use the output-enable ($\overline{OE}$) input to disable the outputs so the buses are effectively isolated.

In the SN74AVC8T245 design, V_{CCA} supplies the control pins (DIR and $\overline{OE}$).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74AVC8T245-Q1	VQFN (24)	3.50 mm × 3.50 mm
	TSSOP (24)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

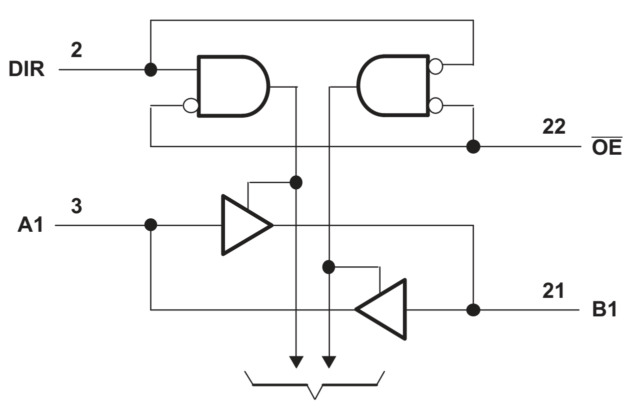


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (March 2016) to Revision D — **Page**

- Added Junction temperature, T_J in *Absolute Maximum Ratings* table ... 4
- Deleted 2DIR and 2$\overline{OE}$ from *Overview* ... 16
- Added *Documentation Support* and *Receiving Notification of Documentation Updates* ... 21

Changes from Revision B (December 2012) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table ... 1

Changes from Revision A (June 2011) to Revision B — **Page**

- Added bullets to the Features list ... 1
- Added *Pin Functions* table to the data sheet ... 3
- Deleted θ_{JA} row from *Absolute Maximum Ratings* table ... 4
- Changed ESD ratings ... 4
- Added Thermal Information table ... 6
- Added Figure 10 and Figure 11 to the *Typical Characteristics* section ... 13

5 Description (continued)

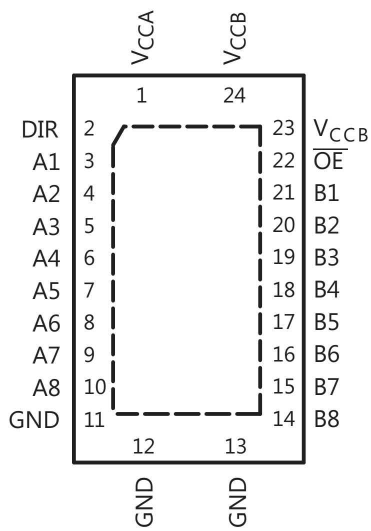
This device specification covers partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are in the high-impedance state.

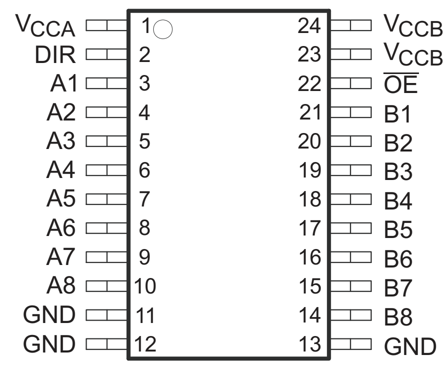
To ensure the high-impedance state during power up or power down, tie $\overline{OE}$ to V_{CC} through a pullup resistor; the current-sinking capability of the driver determines the minimum value of the resistor.

6 Pin Configuration and Functions

RHL Package
24-Pin VQFN
Top View



PW Package
24-Pin TSSOP
Top View



Pin Functions

PIN			TYPE	DESCRIPTION
NAME	VQFN	TSSOP		
A1	3	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	6	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	7	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	8	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	9	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	10	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	21	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	20	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	19	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	18	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	17	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	16	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	15	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	14	I/O	Input/output B8. Referenced to V_{CCB}.
DIR	2	—	I	Direction-control input for 1 ports
GND	12, 13	11, 12, 13	—	Ground

Pin Functions (continued)

PIN			TYPE	DESCRIPTION
NAME	VQFN	TSSOP		
$\overline{OE}$	22	22	I	3-state output-mode enable. Pull $\overline{OE}$ high to place '2' outputs in 3-state mode. Referenced to V_{CCA}.
Thermal pad	—	—	—	The exposed thermal pad must be connected as a secondary GND or be left electrically open.
V_{CCA}	1	1	—	A-port power supply voltage. 1.2 V ≤ V_{CCA} ≤ 3.6 V
V_{CCB}	23, 24	23, 24	—	B-port power supply voltage. 1.2 V ≤ V_{CCB} ≤ 3.6 V

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}, V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	V
		Control inputs	–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	V
V_O	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	(V_{CCA} + 0.5)	V
		B port	–0.5	(V_{CCB} + 0.5)	V
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The device withstands voltages in excess of input voltage and output negative-voltage ratings while operating within the input and output current ratings.
(3) The device withstands voltages in excess of the output positive-voltage rating up to 4.6 V maximum while operating within the output current rating.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 Classification Level H2(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 Classification Level C3B	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

See (1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t / \Delta v$	Input transition rise or fall rate					5	ns / V
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) Hold all unused data inputs of the device at V_{CCI} or GND to assure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

7.4 Thermal Information

THERMAL METRIC[1]		SN74AVC8T245-Q1 RHL (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)[1][2]

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to +125°C	V_{CCO} – 0.2			V
		I_{OH} = –3 mA		1.2 V	1.2 V	T_A = 25°C		0.95		
		I_{OH} = –6 mA		1.4 V	1.4 V	T_A = –40°C to +125°C	1			
		I_{OH} = –8 mA		1.65 V	1.65 V	T_A = –40°C to +125°C	1.2			
		I_{OH} = –9 mA		2.3 V	2.3 V	T_A = –40°C to +125°C	1.75			
		I_{OH} = –12 mA		3 V	3 V	T_A = –40°C to +125°C	2.3			
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to +125°C			0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V	T_A = 25°C		0.15		
		I_{OL} = 6 mA		1.4 V	1.4 V	T_A = –40°C to +125°C			0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V	T_A = –40°C to +125°C			0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V	T_A = –40°C to +125°C			0.55	
		I_{OL} = 12 mA		3 V	3 V	T_A = –40°C to +125°C			0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = 25°C		±0.025	±0.25	µA
						T_A = –40°C to +125°C			±1	
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V	T_A = 25°C		±0.1	±1	µA
						T_A = –40°C to +125°C			±5	
				0 V to 3.6 V	0 V	T_A = 25°C		±0.1	±1	
						T_A = –40°C to +125°C			±5	
I_{OZ} [3]	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V	T_A = 25°C		±0.5	±2.5	µA
						T_A = –40°C to +125°C			±5	

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

Electrical Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
I_{CCA}		$V_I = V_{CCI}$ or GND(4), $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to +125°C			15	µA
			0 V	3.6 V	T_A = –40°C to +125°C			–2	
			3.6 V	0 V	T_A = –40°C to +125°C			15	
I_{CCB}		$V_I = V_{CCI}$ or GND(4), $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to +125°C			15	µA
			0 V	3.6 V	T_A = –40°C to +125°C			15	
			3.6 V	0 V	T_A = –40°C to +125°C			–2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V	T_A = –40°C to +125°C			25	µA
C_i	Control inputs	V_I = 3.3 V or GND	3.3 V	3.3 V	T_A = 25°C		3.5		pF
C_{io}	A or B port	V_O = 3.3 V or GND	3.3 V	3.3 V	T_A = 25°C		6		pF

(4) Hold all unused data inputs of the device at V_{CCI} or GND to assure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

7.6 Switching Characteristics: V_{CCA} = 1.2 V

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	TYP	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V	3.1	ns
			V_{CCB} = 1.5 V	2.6	
			V_{CCB} = 1.8 V	2.5	
			V_{CCB} = 2.5 V	3	
			V_{CCB} = 3.3 V	3.5	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V	3.1	ns
			V_{CCB} = 1.5 V	2.7	
			V_{CCB} = 1.8 V	2.5	
			V_{CCB} = 2.5 V	2.4	
			V_{CCB} = 3.3 V	2.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V	5.3	ns
			V_{CCB} = 1.5 V		
			V_{CCB} = 1.8 V		
			V_{CCB} = 2.5 V		
			V_{CCB} = 3.3 V		
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V	5.1	ns
			V_{CCB} = 1.5 V	4	
			V_{CCB} = 1.8 V	3.5	
			V_{CCB} = 2.5 V	3.2	
			V_{CCB} = 3.3 V	3.1	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V	4.8	ns
			V_{CCB} = 1.5 V		
			V_{CCB} = 1.8 V		
			V_{CCB} = 2.5 V		
			V_{CCB} = 3.3 V		

Switching Characteristics: V_{CCA} = 1.2 V (continued)

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	TYP	UNIT
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V	4.7	ns
			V_{CCB} = 1.5 V	4	
			V_{CCB} = 1.8 V	4.1	
			V_{CCB} = 2.5 V	4.3	
			V_{CCB} = 3.3 V	5.1	

7.7 Switching Characteristics: V_{CCA} = 1.5 V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		3.1		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		14.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		13.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		13.9	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		17.2	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		3.1		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		14.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		14.2	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		13.5	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		13.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		5.3		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		20.5	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		20.5	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		20.5	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		20.5	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		5.1		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		18.6	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		17.7	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		15.1	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		14.4	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		4.8		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		20.3	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		20.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		20.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		20.3	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.7		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		20.0	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		18.6	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		17.9	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		18.9	

7.8 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		2.5		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		14.2	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		13.0	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		12.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		12.1	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		2.5		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		13.3	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		13.0	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		12.1	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		11.8	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		3		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		17.2	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		17.2	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		17.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		17.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.6		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		19.6	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		17.0	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		14.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		13.2	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		2.8		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		17.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		17.7	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		17.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		17.7	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.9		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		18.9	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		17.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		15.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		15.4	

7.9 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		2.4		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		13.5	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		12.1	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		10.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		10.2	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		3		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		13.9	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		12.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		10.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		10.4	

Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V (continued)

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		2.2		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		13.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		13.7	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		13.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		13.7	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.5		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		19.1	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		16.5	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		13.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		12.3	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		1.8		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		14.2	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		14.2	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		14.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		14.2	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.6		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		17.7	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		16.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		14.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		12.1	

7.10 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2 V		2.3		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		13.2	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		11.1	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		10.4	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		9.7	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2 V		3.5		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		17.2	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		12.1	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		10.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		9.7	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2 V		2		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		12.3	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		12.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		12.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		12.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2 V		4.5		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		18.9	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		16.1	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		13.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		12.3	

Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V (continued)

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 12)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2 V		1.7		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		12.3	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		12.3	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		12.3	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		12.3	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2 V		3.4		ns
			V_{CCB} = 1.5 V ± 0.1 V	0.5		17.4	
			V_{CCB} = 1.8 V ± 0.15 V	0.5		15.8	
			V_{CCB} = 2.5 V ± 0.2 V	0.5		13.7	
			V_{CCB} = 3.3 V ± 0.3 V	0.5		12.6	

7.11 Operating Characteristics

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA}	TYP	UNIT
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	pF
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} = V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		
		Outputs disabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} = V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		
	B to A	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	12	
				V_{CCA} = V_{CCB} = 1.5 V	12	
				V_{CCA} = V_{CCB} = 1.8 V	12	
				V_{CCA} = V_{CCB} = 2.5 V	13	
				V_{CCA} = V_{CCB} = 3.3 V	14	
		Outputs disabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} = V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		

(1) Power dissipation capacitance per transceiver

Operating Characteristics (continued)

T_A = 25°C

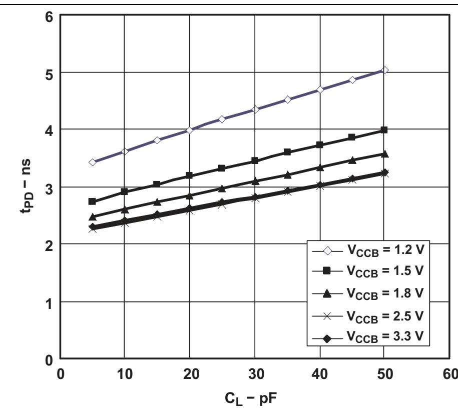
PARAMETER			TEST CONDITIONS	V_{CCA}	TYP	UNIT
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	12	pF
				V_{CCA} = V_{CCB} = 1.5 V	12	
				V_{CCA} = V_{CCB} = 1.8 V	12	
				V_{CCA} = V_{CCB} = 2.5 V	13	
				V_{CCA} = V_{CCB} = 3.3 V	14	
		Outputs disabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} = V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		
	B to A	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} = V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		
		Outputs disabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.2 V	1	
				V_{CCA} = V_{CCB} = 1.5 V		
				V_{CCA} = V_{CCB} = 1.8 V		
				V_{CCA} = V_{CCB} = 2.5 V		
				V_{CCA} = V_{CCB} = 3.3 V		

Table 1. Typical Total Static Current Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	μA
1.5 V	<0.5	<1	<1	<1	<1	1	μA
1.8 V	<0.5	<1	<1	<1	<1	<1	μA
2.5 V	<0.5	1	<1	<1	<1	<1	μA
3.3 V	<0.5	1	<1	<1	<1	<1	μA

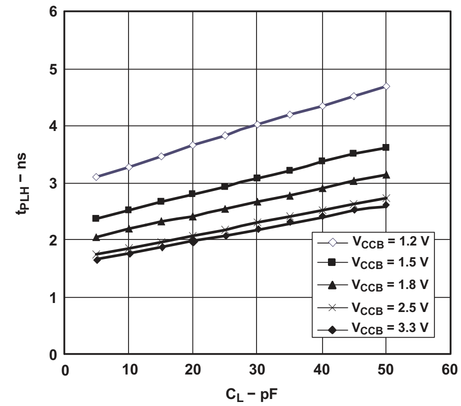
7.12 Typical Characteristics

T_A = 25°C



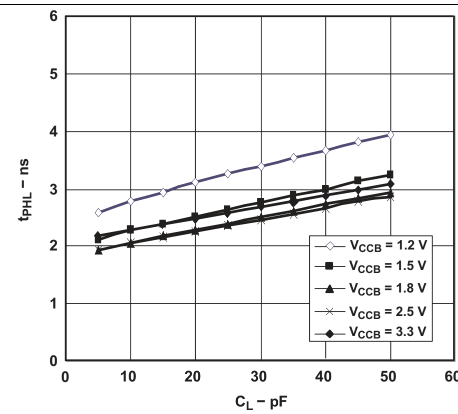
V_{CCA} = 1.2 V

Figure 1. Typical Propagation Delay (A to B) vs Load Capacitance



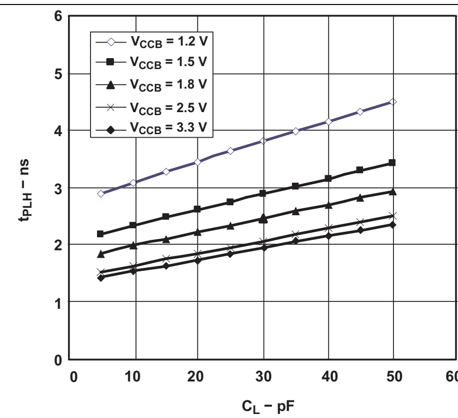
V_{CCA} = 1.5 V

Figure 2. Typical Propagation Delay (A to B) vs Load Capacitance



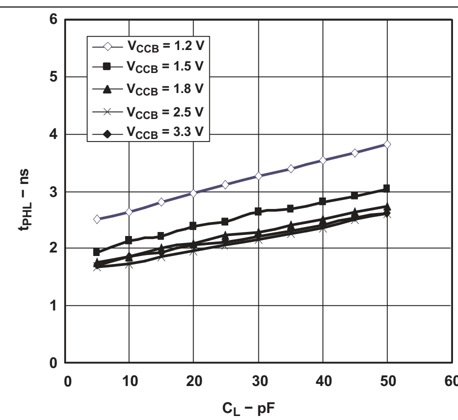
V_{CCA} = 1.5 V

Figure 3. Typical Propagation Delay (A to B) vs Load Capacitance



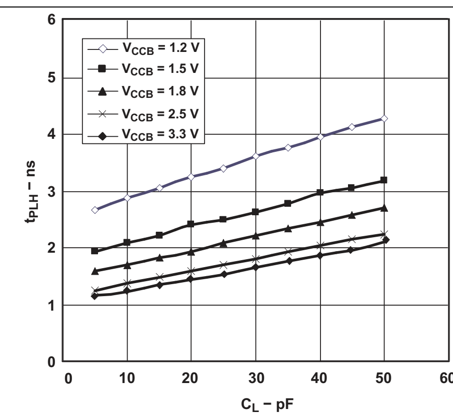
V_{CCA} = 1.8 V

Figure 4. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 1.8 V

Figure 5. Typical Propagation Delay (A to B) vs Load Capacitance

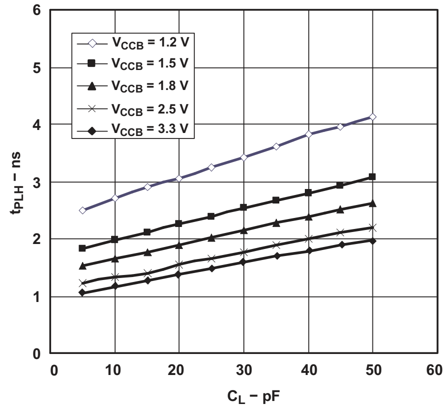


V_{CCA} = 2.5 V

Figure 6. Typical Propagation Delay (A to B) vs Load Capacitance

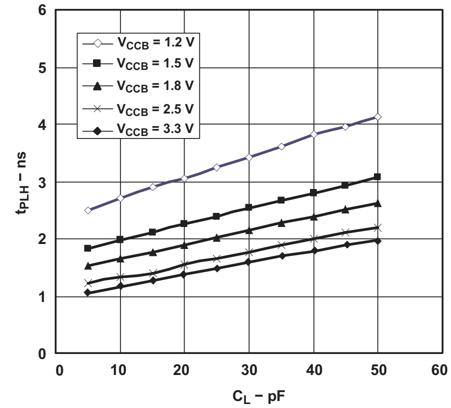
Typical Characteristics (continued)

T_A = 25°C



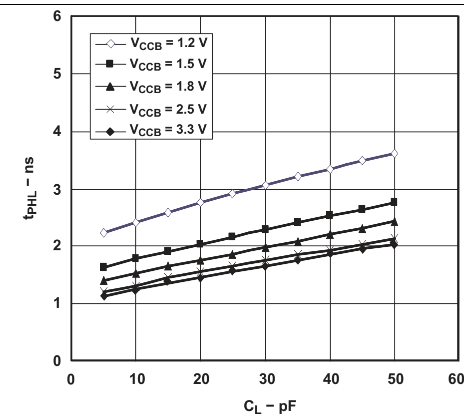
V_{CCA} = 2.5 V

Figure 7. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3 V

Figure 8. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3 V

Figure 9. Typical Propagation Delay (A to B) vs Load Capacitance

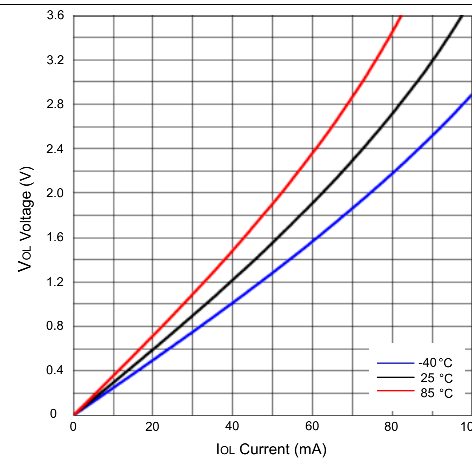


Figure 10. Low-Level Output Voltage (V_{OL}) vs Low-Level Current (I_{OL})

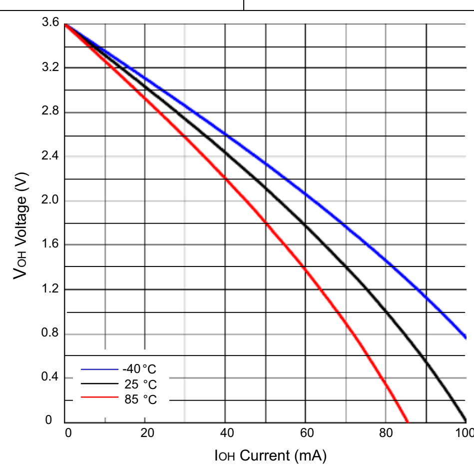
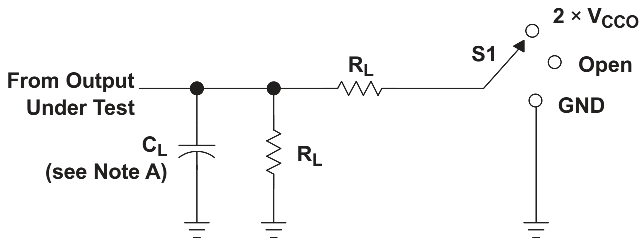


Figure 11. High-Level Output Voltage (V_{OH}) vs High-Level Current (I_{OH})

8 Parameter Measurement Information

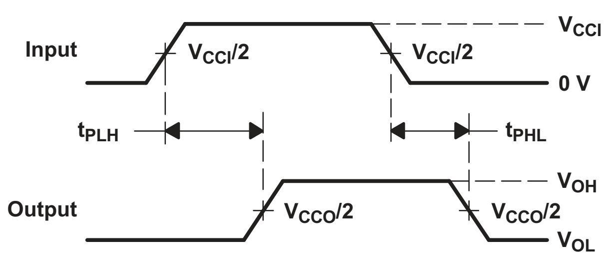


LOAD CIRCUIT

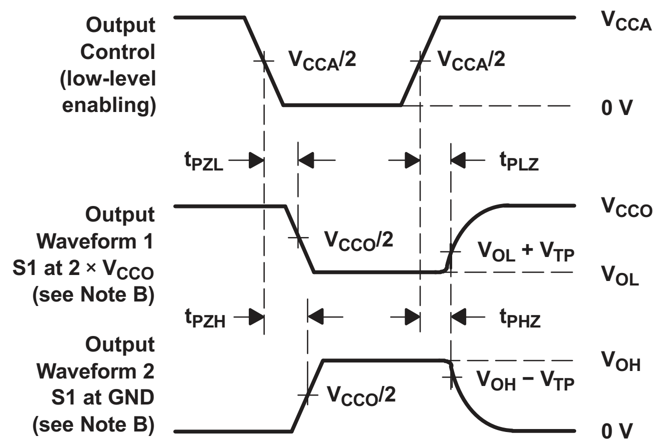
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

Figure 12. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SN74AVC8T245-Q1 is an 8-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (DIR and $\overline{OE}$) are supported by V_{CCA}, and Bx pins are supported by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.2 V to 3.6 V, while the B port can accept I/O voltages from 1.2 V to 3.6 V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state.

9.2 Functional Block Diagram

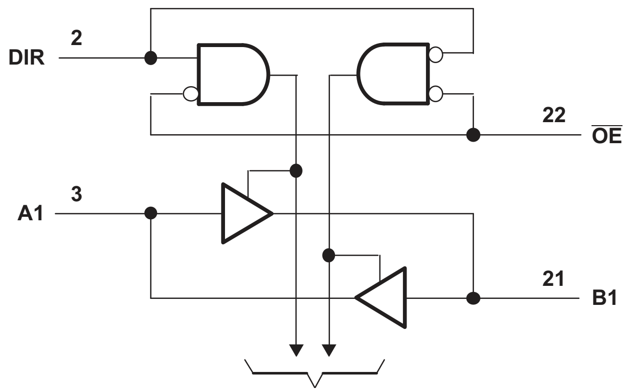


Figure 13. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.2 V and 3.6 V; thus, making the device suitable for translating between any of the low voltage nodes (1.2 V, 1.8 V, 2.5 V, and 3.3 V).

9.3.2 Supports High Speed Translation

The SN74AVC8T245-Q1 device can support high data rate applications. The translated signal data rate can be up to 380 Mbps when the signal is translated from 1.8 V to 3.3 V.

9.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when the device is in partial-power-down mode.

9.4 Device Functional Modes

Table 2 lists the functional modes of the device.

Table 2. FUNCTION TABLE (Each 8-Bit Section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	All outputs Hi-Z

10 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AVC8T245-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC8T245-Q1 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 320 Mbps when the device translates a signal from 1.8 V to 3.3 V.

10.2 Typical Application

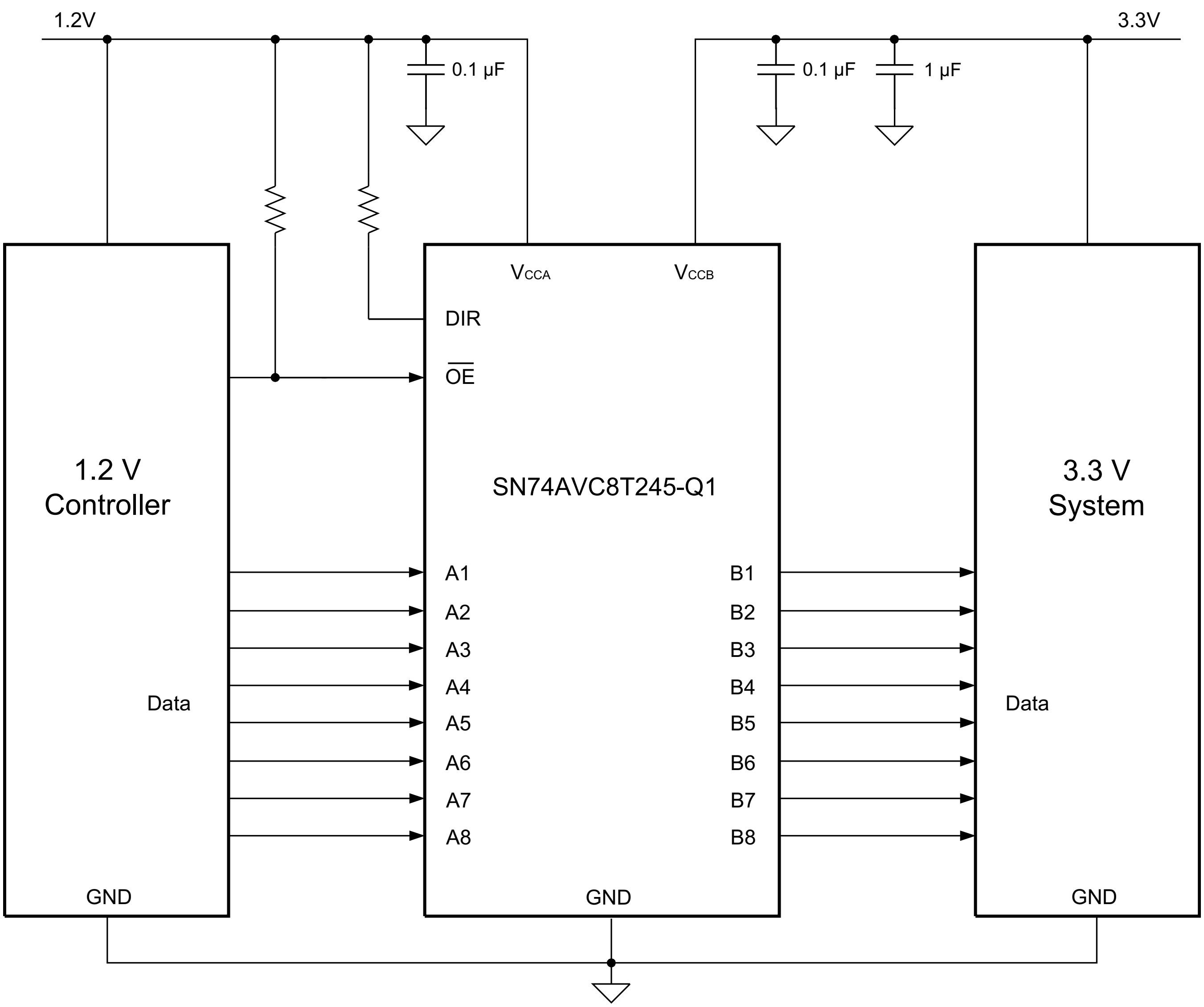


Figure 14. Typical Application Diagram

Typical Application (continued)

10.2.1 Design Requirements

Table 3 lists the parameters for this design example.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V
Output voltage range	3.3 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC8T245-Q1 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port. For this example, the input voltage is 1.2 V.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC8T245-Q1 device is driving to determine the output voltage range. For this example, the output voltage is 3.3 V.

10.2.3 Application Curve

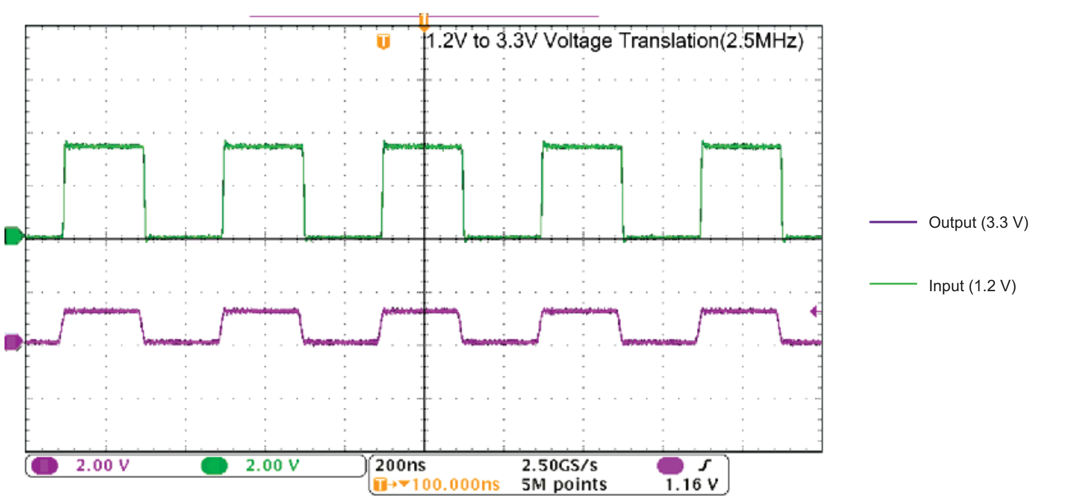


Figure 15. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

11 Power Supply Recommendations

The SN74AVC8T245-Q1 device uses two separate configurable power-supply rails: V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V, and V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively, allowing for low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The output-enable ($\overline{OE}$) input circuit is designed so that it is supplied by V_{CCA}; when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

12.2 Layout Example

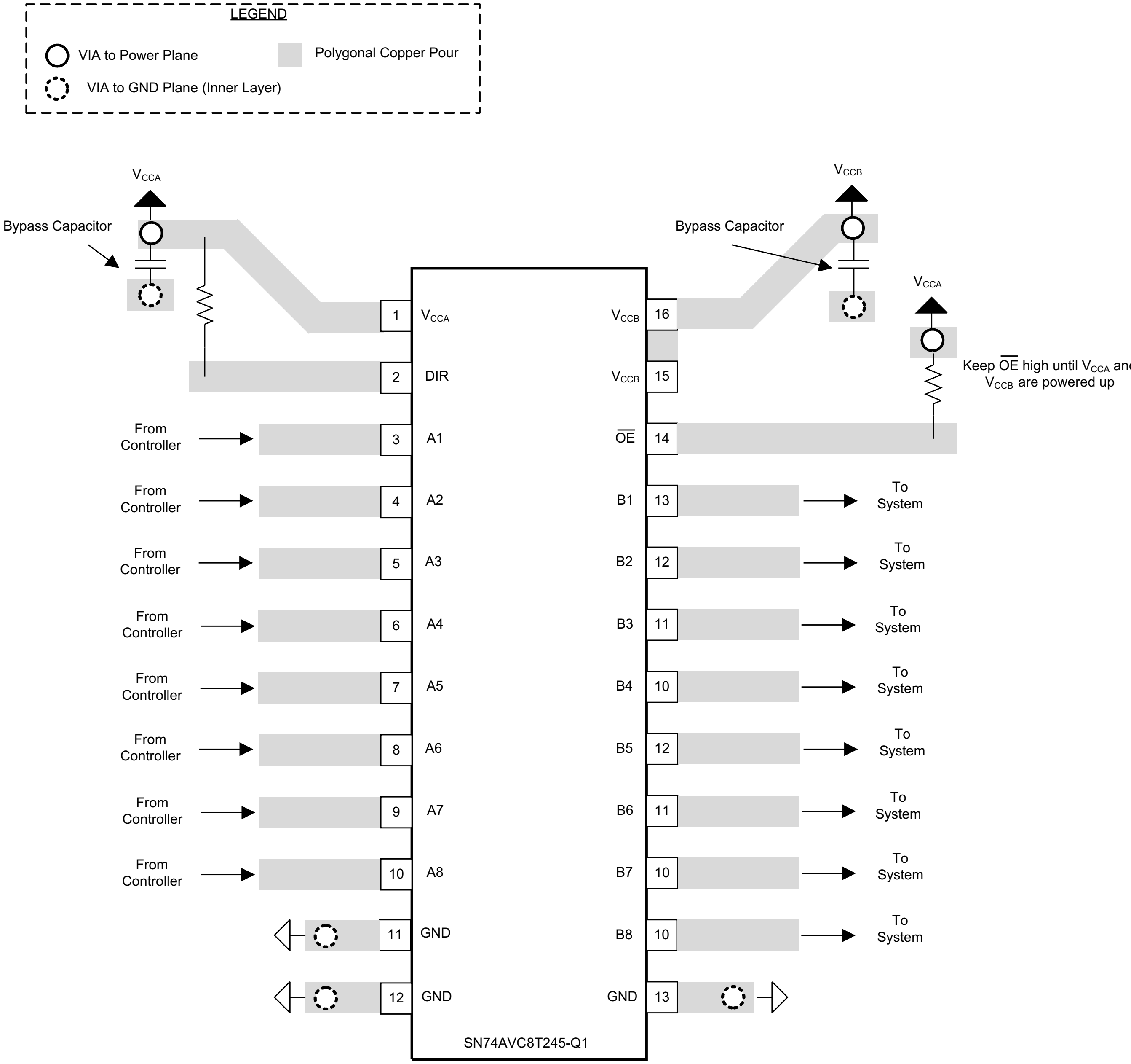


Figure 16. SN74AVC8T245-Q1 Layout Diagram

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* Application Note
- Texas Instruments, *Understanding and Interpreting Standard-Logic Data Sheets* Application Note
- Texas Instruments, *Introduction to Logic* Application Note
- Texas Instruments, *Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards* Application Note
- Texas Instruments, *AVC Advanced Very-Low-Voltage CMOS Logic Data Book* User's Guide

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CAVC8T245QRHLRQ1	ACTIVE	VQFN	RHL	24	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	WE245Q	Samples
SN74AVC8T245QPWRQ1	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	WE245Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AVC8T245-Q1 :

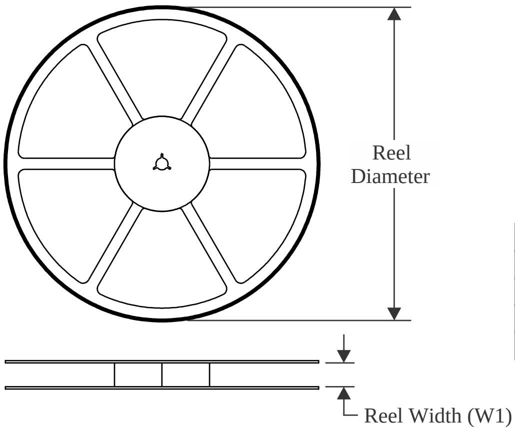
- Catalog: SN74AVC8T245

NOTE: Qualified Version Definitions:

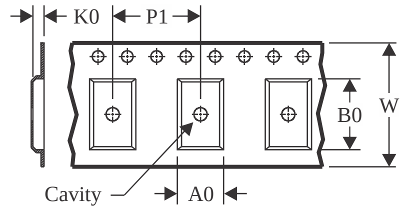
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

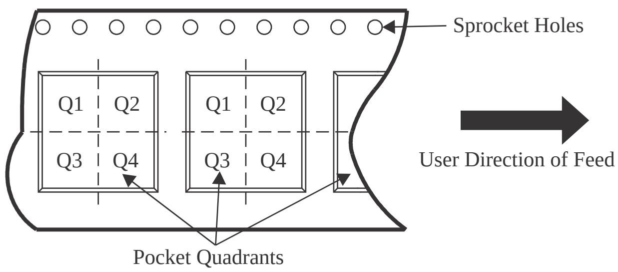


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

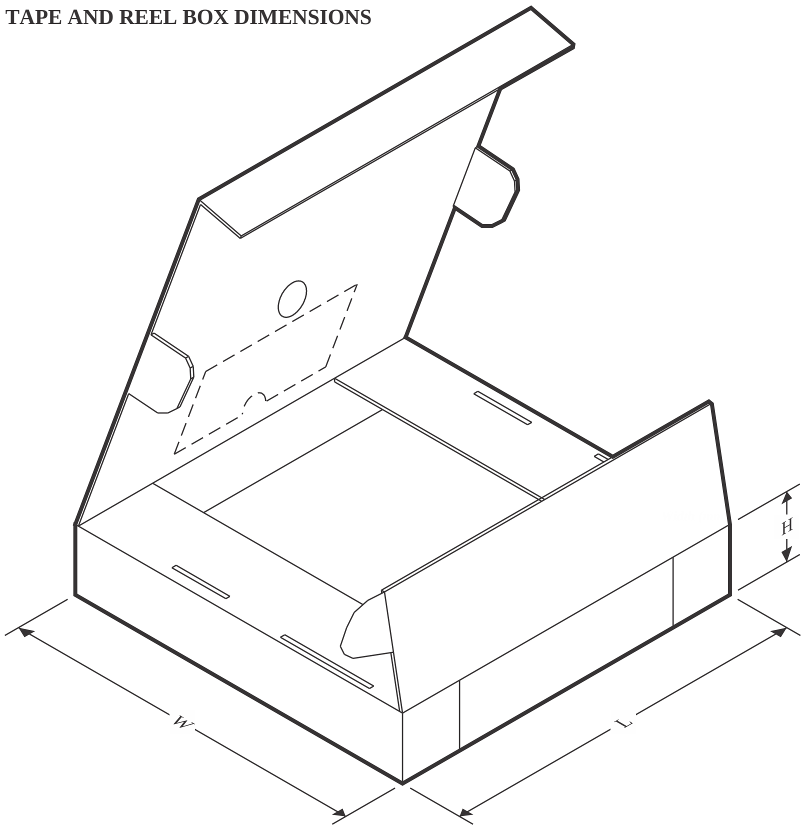
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

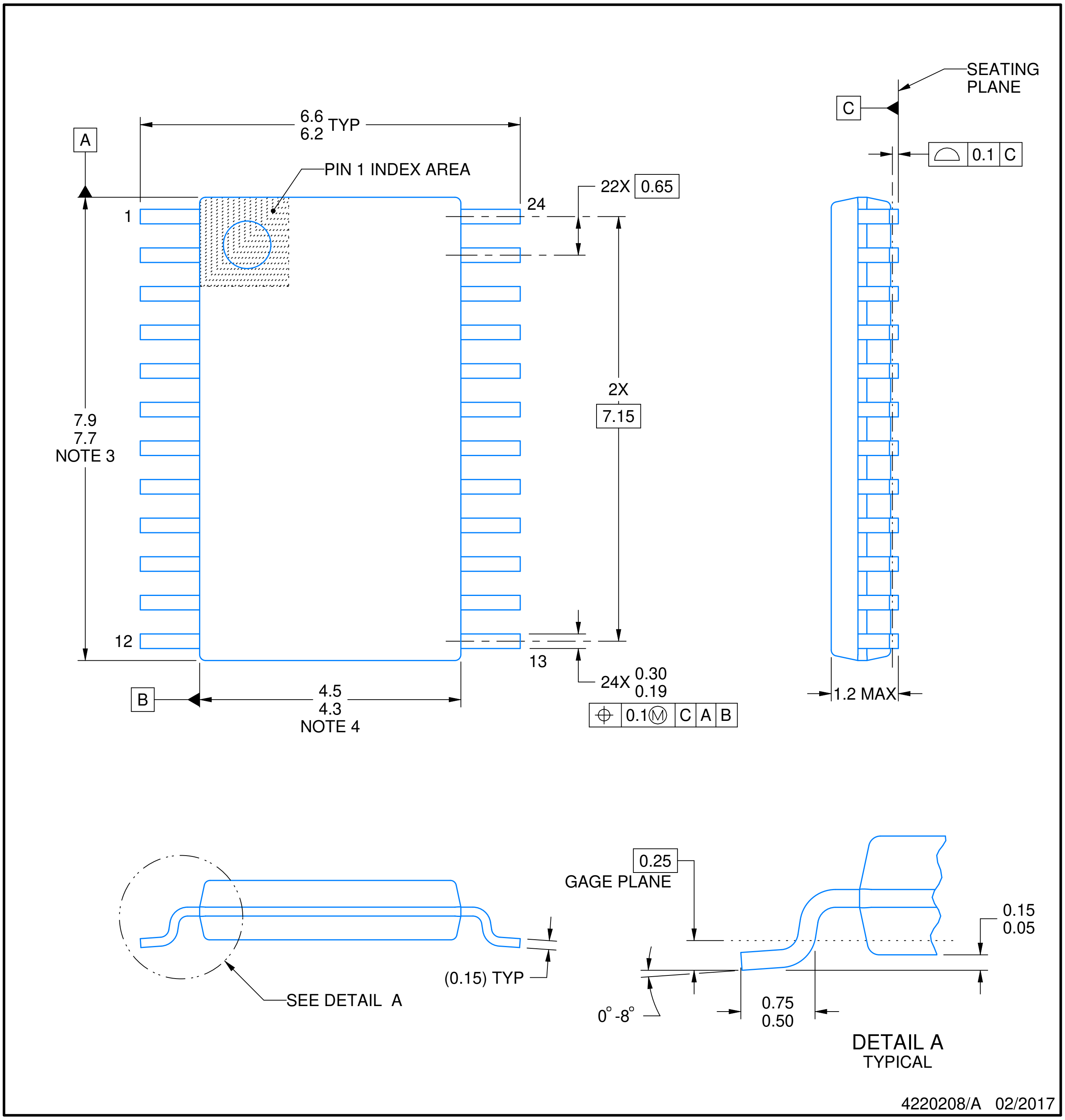
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAVC8T245QRHLRQ1	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1
SN74AVC8T245QPWRQ1	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



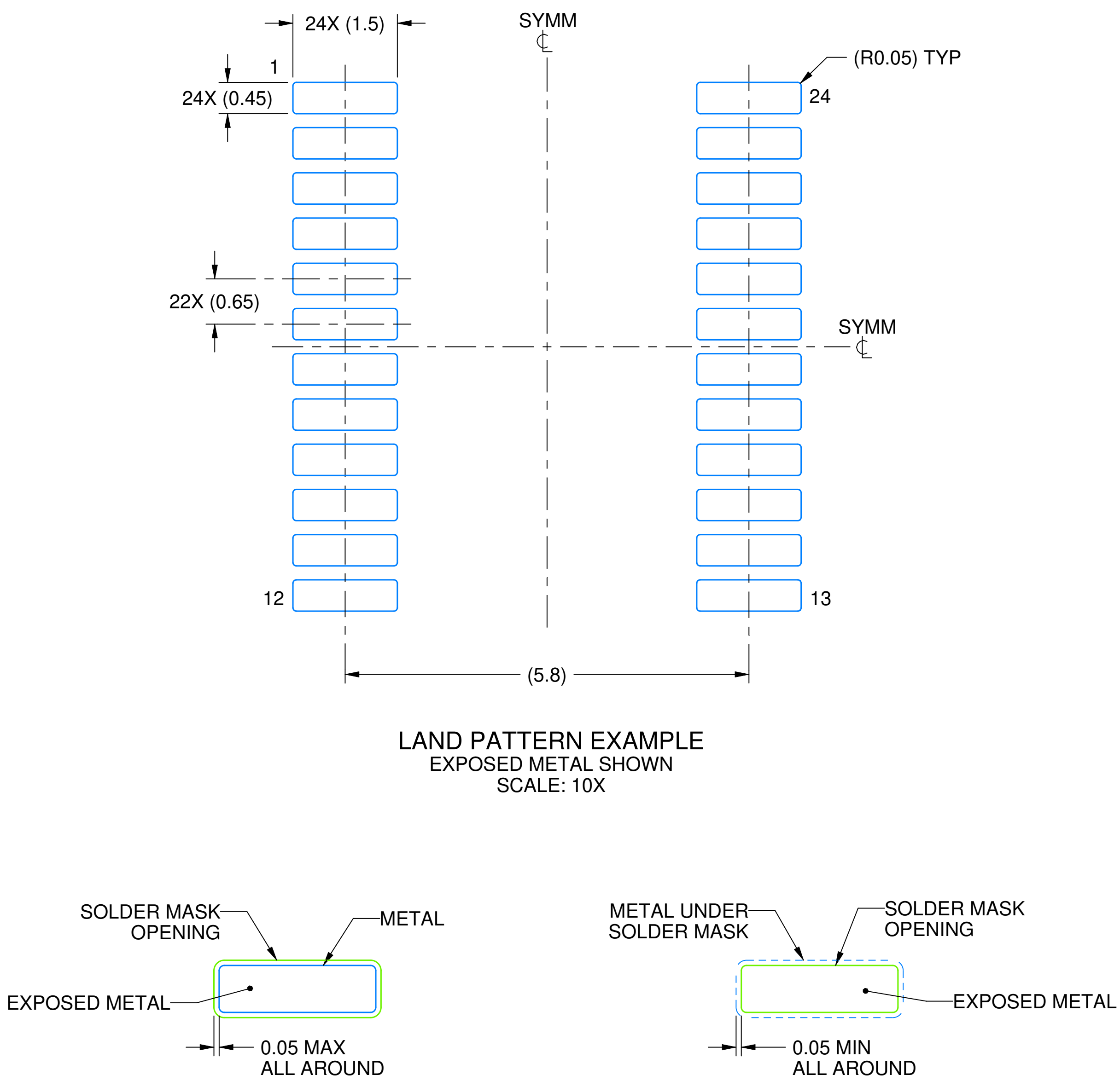
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAVC8T245QRHLRQ1	VQFN	RHL	24	1000	210.0	185.0	35.0
SN74AVC8T245QPWRQ1	TSSOP	PW	24	2000	356.0	356.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

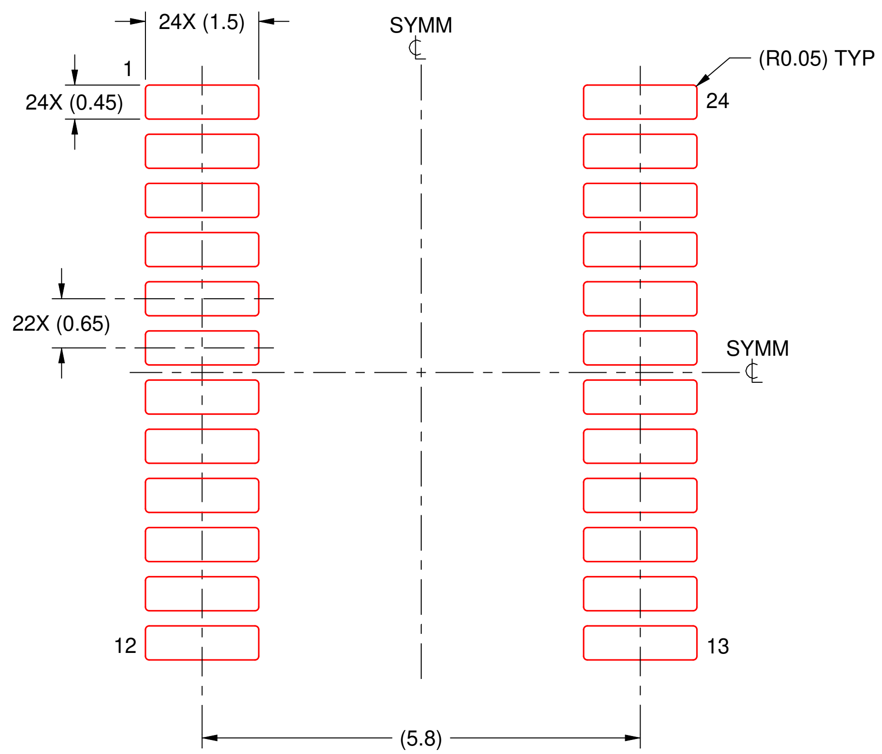
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

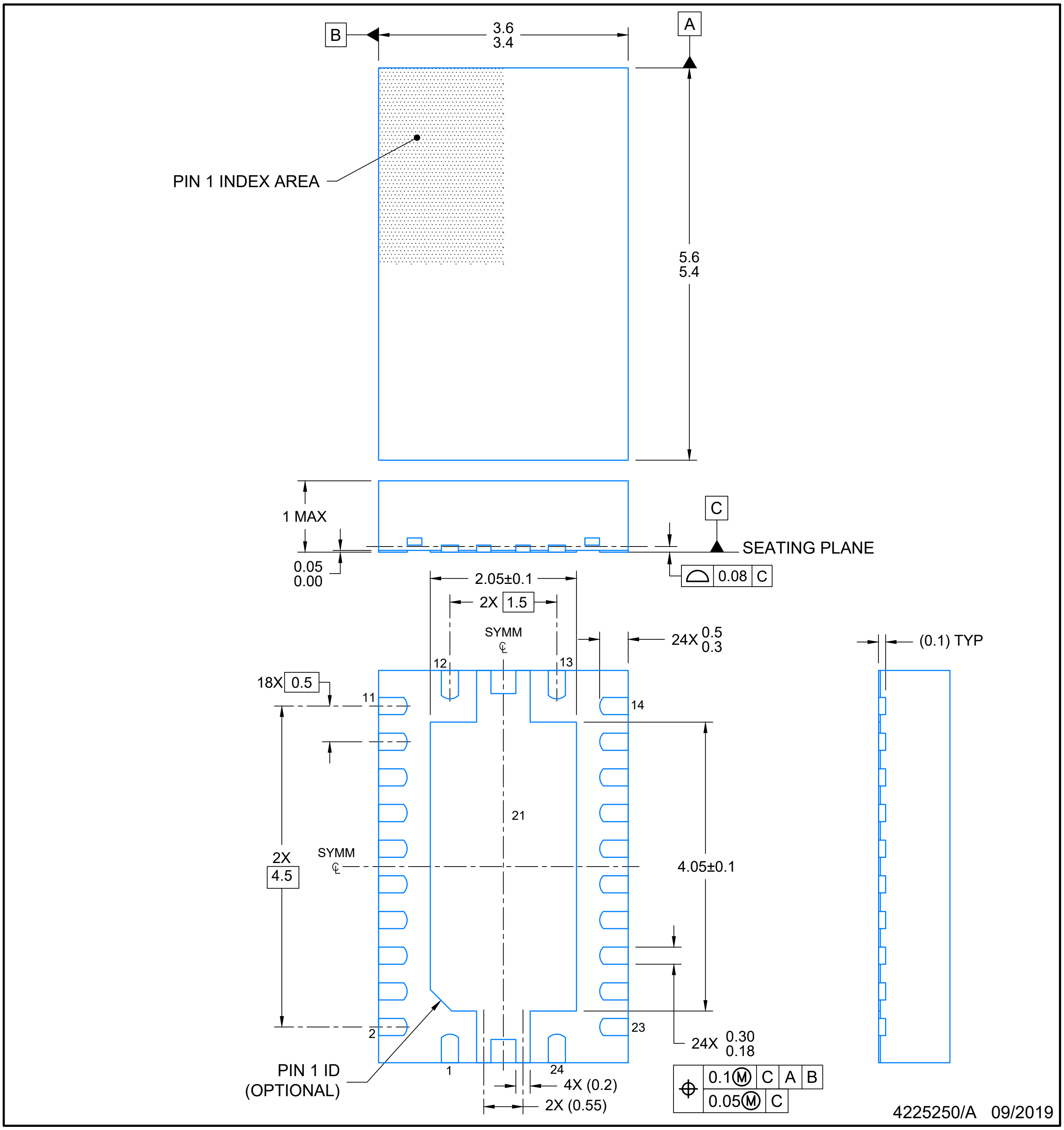


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

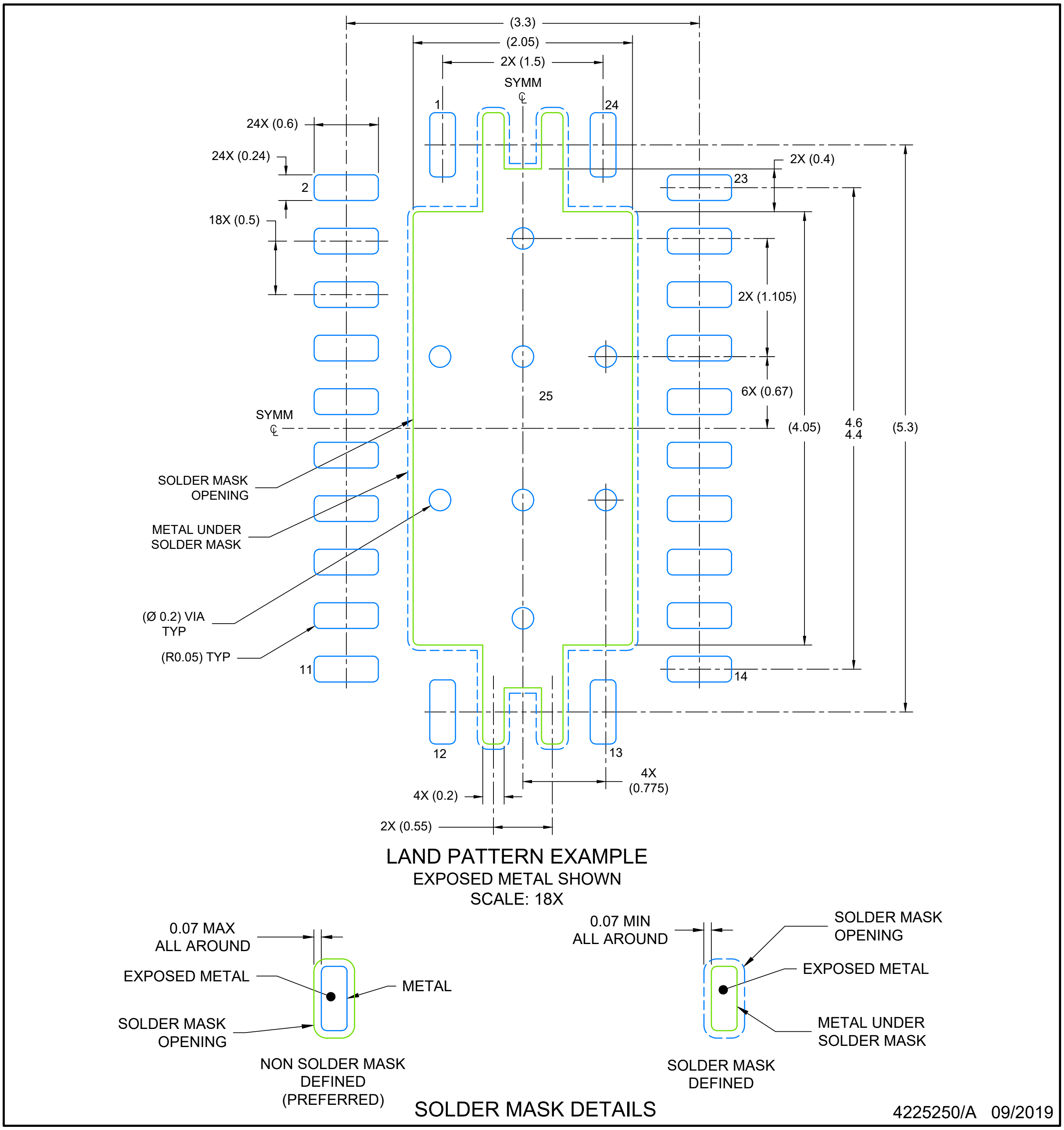
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



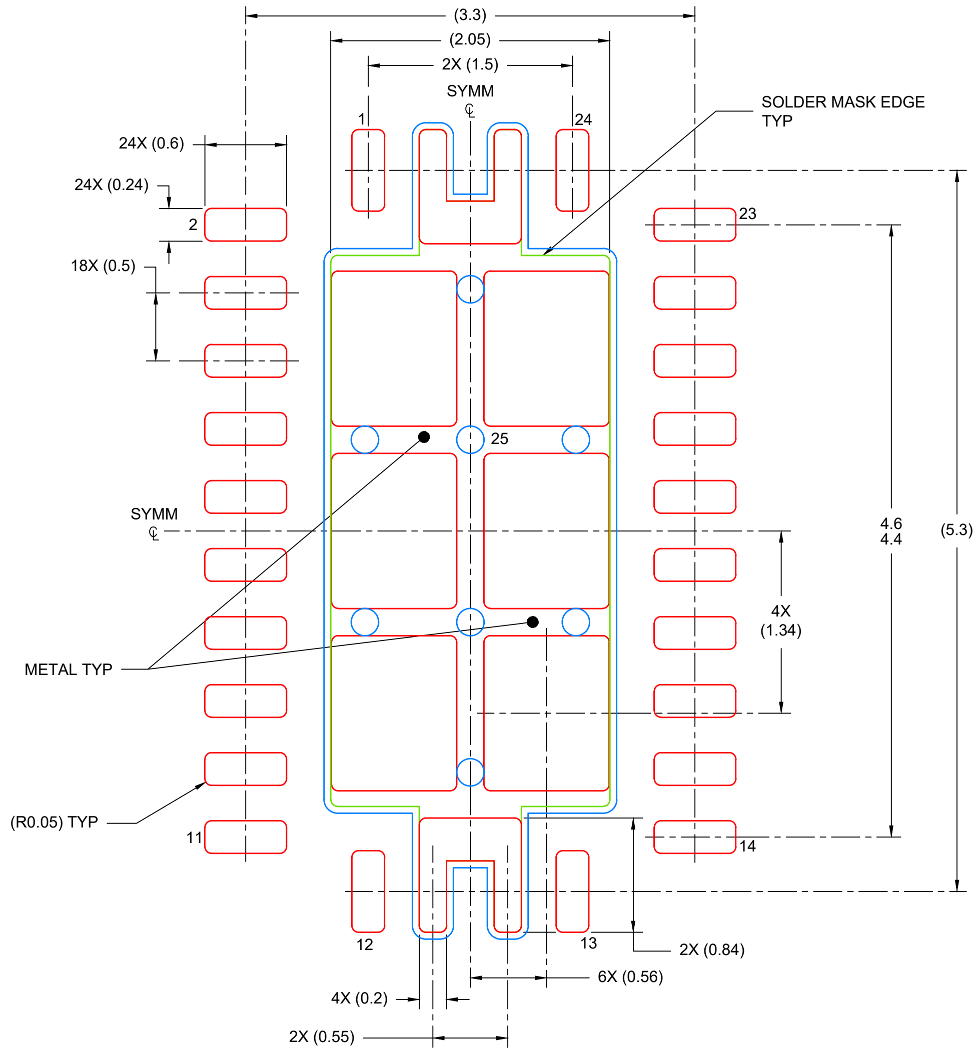
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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