4702B/4702BX

PROGRAMMABLE BIT-RATE GENERATOR

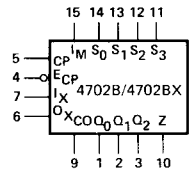
FAIRCHILD CMOS MACROLOGIC™

DESCRIPTION — The 4702B/4702BX Bit-Rate Generator provides the necessary clock signals for digital data transmission systems, such as Universal Asynchronous Receiver and Transmitter circuits (UARTs). It generates any of the 14 commonly used bit rates using an on-chip crystal oscillator, but its design also provides for easy and economical multi-channel operation, where any of the possible frequencies must be made available on any output channel.

One 4702B/4702BX can control up to eight output channels. When more than one bit-rate generator is required, they can still be operated from one crystal. The 4702B is specified to operate over a power supply voltage range of 5 V ± 10%. The 4702BX is a specially selected device specified to operate over a power supply voltage range of 4.5 V to 12.5 V.

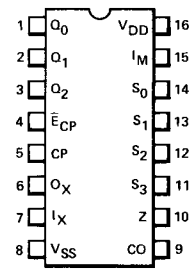
- **PROVIDES 14 COMMONLY USED BIT-RATES**
- **ONE 4702B/4702BX CONTROLS UP TO EIGHT TRANSMISSION CHANNELS**
- **USES 2.4576 MHz INPUT FOR STANDARD FREQUENCY OUTPUTS (16 TIMES BIT RATE)**
- **CONFORMS TO EIA RS-404**
- **ON-CHIP INPUT PULL UP CIRCUITS**
- **TTL COMPATIBLE-OUTPUTS WILL SINK 1.6 mA**
- **INITIALIZATION CIRCUIT FACILITIES DIAGNOSTIC FAULT ISOLATION**
- **LOW POWER DISSIPATION – 1.35 mA POWER DISSIPATION AT 5 V AND 2.4576 MHz**
- **16-PIN DUAL IN-LINE PACKAGE**

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	$\bar{E}_{CP}$	CP	OPERATION
⎍⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍⎺	Reset During First CP = HIGH Time

H = HIGH Level
L = LOW Level
X = Don't Care
⎺⎍⎺ = 1st HIGH Level Clock Pulse After $\bar{E}_{CP}$ Goes LOW
⎍⎍⎍ Clock Pulses

Note 1: Actual output frequency is 16 times the indicated output rate, assuming a clock frequency of 2.4576 MHz.

TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

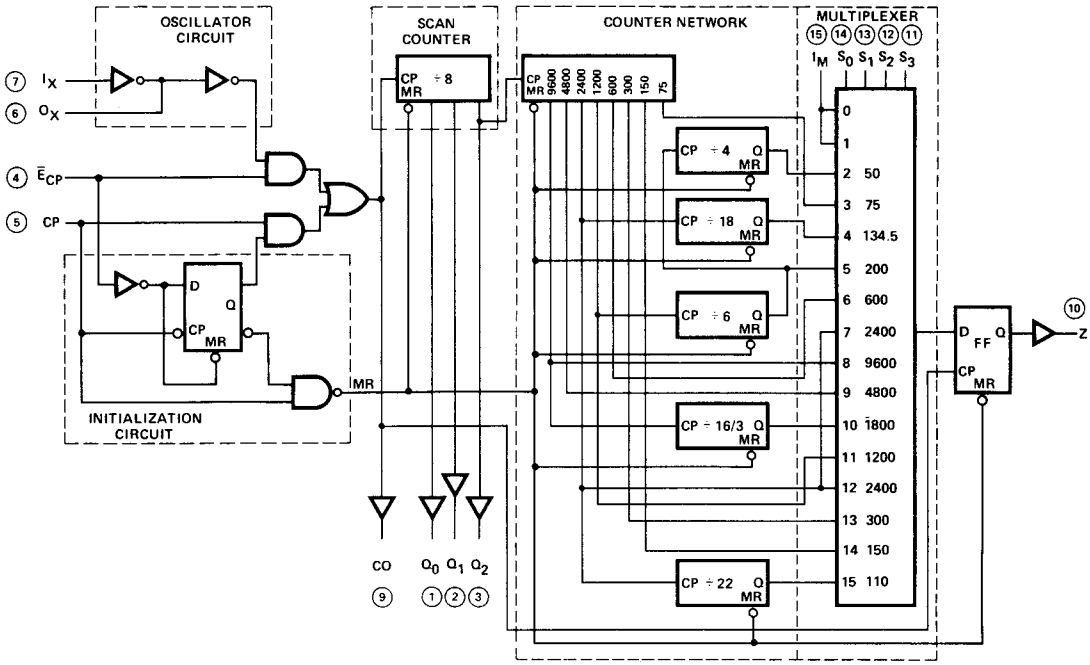
S_3	S_2	S_1	S_0	Output Rate (Z) Note 1
L	L	L	L	Multiplexed Input (I_M)
L	L	L	H	Multiplexed Input (I_M)
L	L	H	L	50 Baud
L	L	H	H	75 Baud
L	H	L	L	134.5 Baud
L	H	L	H	200 Baud
L	H	H	L	600 Baud
L	H	H	H	2400 Baud
H	L	L	L	9600 Baud
H	L	L	H	4800 Baud
H	L	H	L	1800 Baud
H	L	H	H	1200 Baud
H	H	L	L	2400 Baud
H	H	L	H	300 Baud
H	H	H	L	150 Baud
H	H	H	H	110 Baud

L = LOW Level
H = HIGH Level

PIN NAMES

CP	External Clock Input
$\bar{E}_{CP}$	External Clock Enable Input (Active LOW)
I_X	Crystal Input
I_M	Multiplexed Input
S_0-S_3	Rate Select Inputs
CO	Clock Output
O_X	Crystal Drive Output
Q_0-Q_2	Scan Counter Outputs
Z	Bit Rate Output

BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number

FUNCTIONAL DESCRIPTION – Digital data transmission systems employ a wide range of standardized bit rates, ranging from 50 baud interfacing with electromechanical devices, to 9600 baud for high speed modems. Modern electronic systems commonly use Universal Asynchronous Receiver and Transmitter circuits (UARTs) to convert parallel data inputs into a serial bit stream (transmitter) and to reconvert the serial bit stream into parallel outputs (receiver). In order to resynchronize the incoming serial data, the receiver requires a clock rate that is a multiple of the incoming bit rate. Popular MOS-LSI UART circuits use a clock that is 16 times the transmitted bit rate. The 4702B/4702BX can generate 14 standardized clock rates from one commonly high frequency input.

The 4702B/4702BX contains the following five functional subsystems which are discussed in detail below:

1. An Oscillator Circuit with associated gating.
2. A prescaler used as Scan Counter for multichannel operation (described in the applications section).
3. A Counter Network to generate the required standardized frequencies.
4. An output Multiplexer (frequency selector) with resynchronizing output flip-flop.
5. An Initialization (reset) Circuit.

Oscillator – For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576 MHz (i.e. 9600 baud x 16 x 16, since the scan counter and the first flip-flop of the counter chain act as an internal ÷ 16 prescaler). A lower input frequency will obviously result in a proportionally lower output frequency.

The 4702B/4702BX can be driven from two alternate clock sources: (1) When the E_{CP} (active LOW External Clock Enable) input is LOW, the CP input is the clock source. (2) When the E_{CP} input is HIGH, a crystal connected between I_X and O_X, or a signal applied to the I_X input, is the clock source.

Prescaler (Scan Counter) – The clock frequency is made available on the CO (Clock Output) pin and is applied to the ÷ 8 prescaler with buffered outputs Q_0, Q_1, and Q_2. This prescaler is of no particular advantage in single frequency applications, but it is essential for the simple economical multichannel scheme described in the Applications section of this data book.

Counter Network – The prescaler output Q_2 is a square wave of 1/8 the input frequency and is used to drive the frequency counter network generating 13 standardized frequencies. Note that the frequencies are labeled in the block diagram and described in terms of the transmission bit rate. In a conventional system using a 2.4576 MHz clock input, the actual output frequencies are 16 times higher.

The output from the first frequency divider flip-flop is thus labeled 9600, since it is used to transmit or receive 9600 baud (bits per second). The actual frequency at this node is 16 x 9.6 kHz = 153.6 kHz. Seven more cascaded binaries generate the appropriate frequencies for bit rates 4800, 2400, 1200, 600, 300, 150, and 75.

The other five bit rates are generated by individual counters:

bit rate 1200 is divided by 6 to generate bit rate 200,
bit rate 200 is divided by 4 to generate bit rate 50,
bit rate 2400 is divided by 18 to generate bit rate 134.5 with a frequency error of –0.87%,
bit rate 2400 is also divided by 22 to generate bit rate 110 with a frequency error of –0.83%, and
bit rate 9600 is divided by 16/3 to generate bit rate 1800.

The 16/3 division is accomplished by alternating the divide ratio between 5 (twice) and 6 (once). The result is an exact average output frequency with some frequency modulation. Taking advantage of the ÷ 16 feature of the UART, the resulting distortion is less than 0.78%, irrespective of the number of elements in a character, and therefore well within the timing accuracy specified for high speed communications equipment. All signals except 1800, have a 50% duty cycle.

Output Multiplexer – The outputs of the counter network are fed to a 16-input multiplexer, which is controlled by the Rate Select inputs (S_0-S_3). The multiplexer output is then resynchronized with the incoming clock in order to cancel all cumulative delays and to present an output signal at the buffered output (Z) that is synchronous with the prescaler outputs (Q_0-Q_2). *Table 2* lists the correspondence between select code and output bit rate. Two of the 16 codes do not select an internally generated frequency, but select an input into which the user can feed either a different, nonstandardized frequency, or a static level (HIGH or LOW) to generate "zero baud".

The bit rates most commonly used in modern data terminals (110, 150, 300, 1200, 2400 baud) require that no more than one input be grounded, easily achieved with a single pole, 5-position switch. 2400 baud is selected by two different codes, so that the whole spectrum of modern digital communication rates has a common HIGH on the S_3 input.

Initialization (Reset) – The initialization circuit generates a common master reset signal for all flip-flops in the 4702B/4702BX. This signal is derived from a digital differentiator that senses the first HIGH level on the CP input after the $\overline{E}_{CP}$ input goes LOW. When $\overline{E}_{CP}$ is HIGH, selecting the Crystal input, CP must be LOW. A HIGH level on CP would apply a continuous reset.

All inputs to the 4702B/4702BX, except I_X have on-chip pull-up circuits which improve TTL compatibility and eliminate the need to tie a permanently HIGH input to V_{DD}.

DC CHARACTERISTICS: V_{DD} = 5 V, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEMP	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		3.5			V	All	Guaranteed Input High Voltage
V_{IL}	Input LOW Voltage				1.5	V	All	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage		4.95			V	MIN, 25°C	$I_{OH} < 1\ \mu A$, Inputs at 0 or 5 V per the Logic Function or Truth Table
			4.95				MAX	
			4.5			V	All	$I_{OH} < 1\ \mu A$, Inputs at 1.5 or 3.5 V
V_{OL}	Output LOW Voltage				0.05	V	MIN, 25°C	$I_{OL} < 1\ \mu A$, Inputs at 0 or 5 V per the Logic Function or Truth Table
					0.05		MAX	
					0.5	V	All	$I_{OL} < 1\ \mu A$, Inputs at 1.5 or 3.5 V
I_L (See Note 1)	Input LOW Current for Input I_X	XC			0.3	μA	MIN, 25°C	Pin under Test at 0 V All other Inputs Simultaneously at 5 V
					1		MAX	
		XM			0.1	μA	MIN, 25°C	
					1		MAX	
	Input LOW Current for all Other Inputs	XC	−15	−30	−100	μA	25°C	
		XM	−15	−30	−100			
I_{IH}	Input HIGH Current for all Inputs	XC			0.3	μA	MIN, 25°C	Pin Under Test at 5 V All other Inputs Simultaneously at 0 V
					1		MAX	
		XM			0.1	μA	MIN, 25°C	
					1		MAX	
I_{OH}	Output HIGH Current for Output O_X		−0.3			mA	MIN, 25°C	V_{OUT} = 4.5 V Inputs at 0 or 5 V per Logic Function or Truth Table
			−0.1				MAX	
	Output HIGH Current for all other Outputs		−1.5			mA	MIN, 25°C	V_{OUT} = 2.5 V
			−1				MAX	
			−0.5			mA	MIN, 25°C	V_{OUT} = 4.5 V
			−0.3				MAX	
I_{OL}	Output LOW Current for Output O_X		0.2			mA	MIN, 25°C	V_{OUT} = 0.4 V
			0.1				MAX	
	Output LOW Current for all Other Outputs		3.2			mA	MIN, 25°C	
			1.6				MAX	
I_{DD}	Quiescent Power Supply Current	XC			100	μA	MIN, 25°C	$\overline{E}_{CP} = V_{DD}$, CP = 0 V, All other Inputs at 0 V or V_{DD} (Note 6)
					1000		MAX	
		XM			10	μA	MIN, 25°C	
					150		MAX	

See Notes on following page.

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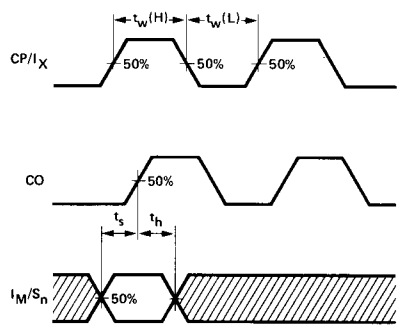
AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} = 5 V, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_{PLH} t_{PHL}	Propagation Delay I_X to CO		175 135	350 275	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns C_L ⩽ 7 pF on O_X
t_{PLH} t_{PHL}	Propagation Delay CP to CO		130 110	260 220	ns	
t_{PLH} t_{PHL}	Propagation Delay CO to $\bar{Q}_n$		53 45	Note 5	ns	
t_{PLH} t_{PHL}	Propagation Delay CO to Z		37 32	85 75	ns	
t_{TLH} t_{THL}	Output Transition Time (Except O_X)		80 35	160 75	ns	
t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	350	185 −182		ns	
t_s t_h	Set-Up Time, I_M to CO Hold Time, I_M to CO	350 0	190 −182		ns	
$t_wCP(L)$ $t_wCP(H)$	Minimum Clock Pulse Width LOW and HIGH	120 120	60 60		ns	
$t_wI_X(L)$ $t_wI_X(H)$	Minimum I_X Pulse Width LOW and HIGH	160 160	75 75		ns	

NOTES:
1. Propagation Delays and Output Transition Times are graphically described under 4000B Series CMOS Family Characteristics.
2. The first HIGH level Clock Pulse after $\overline{E}_{CP}$ goes LOW must be at least 350 ns long to guarantee reset of all Counters.
3. It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V, and the V_{DD} pin should be decoupled.
4. Input current and quiescent power supply current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
5. For multichannel operation, propagation delay, CO to Q_n, plus set-up time, select to CO, is guaranteed to ⩽ 367 ns.
6. I_{DD} is measured on Pin 8 and does not include Input Leakage Currents.

SWITCHING WAVEFORMS



MINIMUM CP AND I_X PULSE WIDTHS AND SET-UP AND HOLD TIMES, SELECT INPUT (S_n) TO CLOCK OUTPUT (CO) AND I_M INPUT TO CLOCK OUTPUT (CO)

NOTE: Set-up and Hold Times are shown as positive values but may be specified as negative values.

APPLICATIONS

Single Channel Bit Rate Generator – *Figure 1* shows the simplest application of the 4702B/4702BX. This circuit generates one of five possible bit rates as determined by the setting of a single pole, 5-position switch. The bit rate output (Z) drives one standard TTL load or four low power Schottky loads over the full temperature range. The possible output frequencies correspond to 110, 150, 300, 1200, and 2400 Baud. For many low cost terminals these five bit rates are adequate.

Simultaneous Generation of Several Bit Rates:
Fixed Programmed Multichannel Operation – Figure 2 shows a simple scheme that generates eight bit rates on eight output lines, using one 4702B/4702BX and one 93L34 8-Bit Addressable Latch. This and the following applications take advantage of the built-in scan counter (prescaler) outputs. As shown in the block diagram, these outputs (Q_0 to Q_2) go through a complete sequence of eight states for every half-period of the highest output frequency (9600 Baud). Feeding these Scan Counter outputs back to the Select inputs of the multiplexer causes the 4702B/4702BX to interrogate sequentially the state of eight different frequency signals. The 93L34 8-Bit Addressable Latch, addressed by the same Scan Counter outputs, reconverts the multiplexed single output (Z) of the 4702B/4702BX into eight parallel output frequency signals. In the simple scheme of *Figure 2*, input S_3 is left open (HIGH) and the following bit rates are generated:

Q_0:	110 Baud,	Q_1:	9600 Baud,	Q_2:	4800 Baud,	Q_3:	1800 Baud,
Q_4:	1200 Baud,	Q_5:	2400 Baud,	Q_6:	300 Baud,	Q_7:	150 Baud.

Other bit rate combinations can be generated by changing the Scan Counter to selector interconnection or by inserting logic gates into this path.

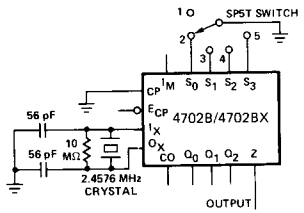
Fully Programmable Multichannel Operation – Figure 3 shows a fully programmable 8-channel bit rate generator system that, under computer control, generates arbitrarily assigned bit rates on all eight outputs simultaneously. The basic operation is similar to the previously described fixed programmed system, but two 9LS170 4 x 4 Register File MSI packages are connected as programmable look-up tables between the Scan Counter outputs (Q_0 to Q_2) and the multiplexer Select inputs (S_0 to S_3). The content of this 8-word by 4-bit memory determines which frequency appears at what output.

19200 Baud Operation – Though a 19200 Baud signal is not internally routed to the multiplexer, the 4702B/4702BX can be used to generate this bit rate by connecting the Q_2 output to the I_M input and applying select code 0 or 1. An additional 2-input NAND gate can be used to retain the "Zero Baud" feature on select code 0. Any multichannel operation that involves 19200 Baud must be limited to four outputs as shown in *Figure 4*. Only the two least significant Scan Counter outputs are used, so that the scan is completed within one half period of the 19200 output frequency.

Clock Expansion – One 4702B/4702BX can control up to eight output channels. For more than eight channels, additional bit rate generators are required. These bit rate generators can all be run from the same crystal or clock input. *Figure 5* shows one possible expansion scheme. One 4702B/4702BX is provided with a crystal. All other devices derive their clock from this master. *Figure 6* shows a different scheme where the master clock output feeds into the I_X input of all slaves and all E_{CP} inputs are normally held HIGH. This scheme retains the reset feature and the selection between two different clock sources of the basic 4702B/4702BX circuit.

During normal operation, the common E_{CP} line is HIGH and the common clock line (CP) is LOW. For diagnostic purposes the common E_{CP} is forced LOW. This deselects the crystal frequency and initiates the diagnostic mode. When CP goes HIGH for the first time, all 4702B/4702BXs are reset through their individual on-chip initialization circuitry. Subsequent LOW-to-HIGH clock transitions on the common CP line advance the scan counter, causing all 4702B/4702BXs to operate synchronously.

TYPICAL APPLICATIONS



SWITCH POSITION	BIT RATE
1	110 Baud
2	150 Baud
3	300 Baud
4	1200 Baud
5	2400 Baud

Fig. 1
SWITCH SELECTABLE BIT RATE GENERATOR CONFIGURATION PROVIDING FIVE BIT RATES

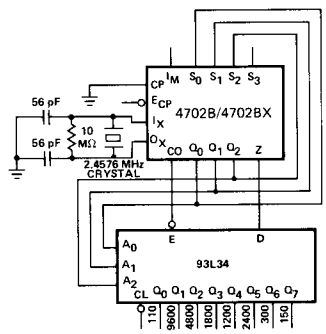


Fig. 2
BIT RATE GENERATOR CONFIGURATION WITH EIGHT SIMULTANEOUS FREQUENCIES

TYPICAL APPLICATIONS (Cont'd)

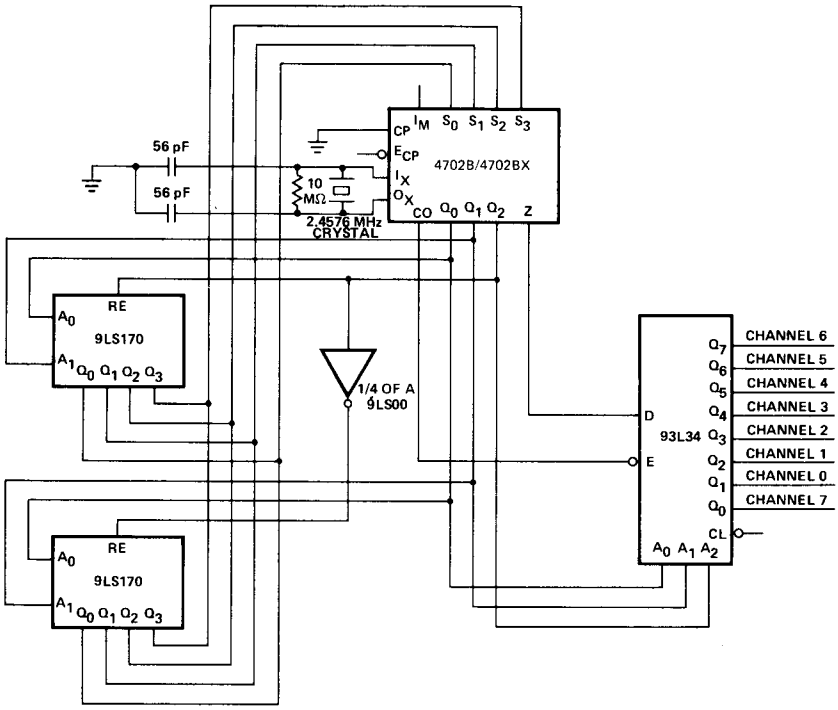


Fig. 3

FULLY PROGRAMMABLE 8-CHANNEL BIT RATE GENERATOR SYSTEM

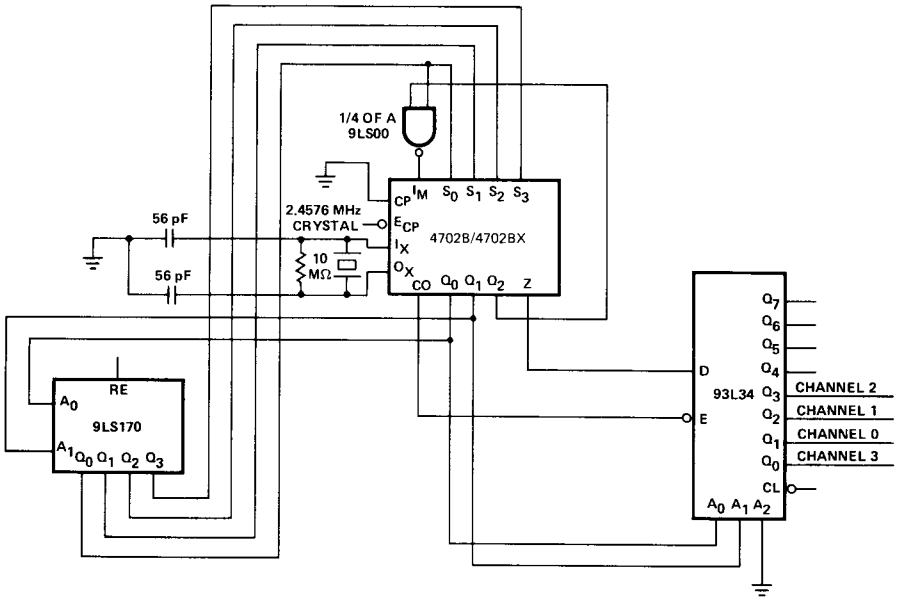


Fig. 4

FULLY PROGRAMMABLE 4-CHANNEL BIT RATE GENERATOR SYSTEM WITH THE 19.2k BAUD FEATURE

TYPICAL APPLICATIONS (Cont'd)

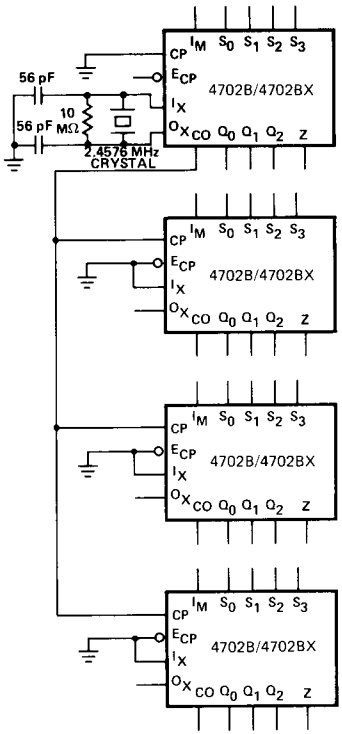


Fig. 5
CASCADE CLOCK EXPANSION SCHEME

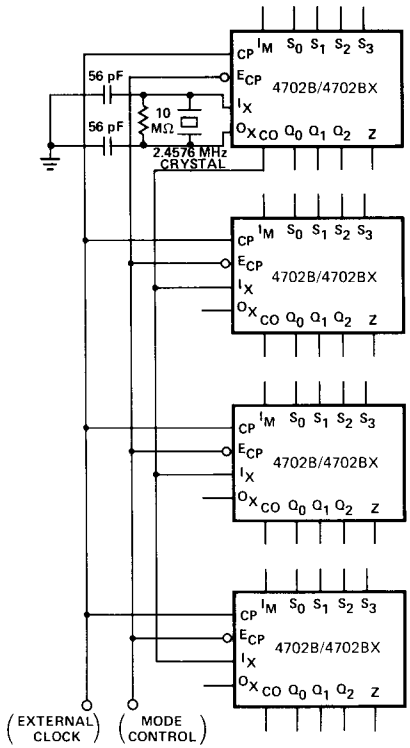


Fig. 6
TANDEM CLOCK EXPANSION SCHEME

CRYSTAL SPECIFICATION RECOMMENDATIONS – Table 3 is a convenient listing of recommended crystal specifications. Crystal manufacturers are also listed below.

TABLE 3 CRYSTAL SPECIFICATIONS

PARAMETERS	TYPICAL CRYSTAL SPEC
Frequency	2.4576 MHz "AT" Cut
Series Resistance (Max)	250 Ω
Unwanted Modes	−6 dB (Min)
Type of Operation	Parallel
Load Capacitance	32 pF ±0.5

CRYSTAL MANUFACTURERS

CTS Knights, Inc.
Sandwich, Ill. 60548
(815) 786-8411
Crystal #F1004

X - Tron Electronics
1869 National Ave.
Hayward, Calif.
(415) 783-2145

Erie Frequency Control
499 Lincoln St.
Carlisle, Pa. 17013
(717) 249-2232

International Crystal Mfg. Company
10 No. Lee
Oklahoma City, Okla. 73102
(405) 236-3741

Sentry Manufacturing Co.
Crystal Park
Chickasha, Oklahoma 73018
(405) 224-6780
Crystal # SGP 6-2.4576 or
Crystal # SGP-7-2.4576