

# n-Channel Power MOSFET

OptiMOS™  
BSF134N10NJ3 G

## Data Sheet

2.6, 2014-01-10  
Final

Industrial & Multimarket

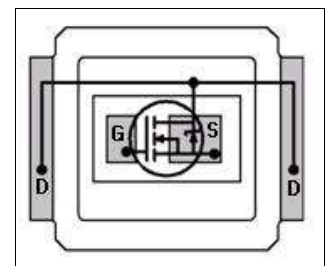
## 1 Description

OptiMOS™100V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 100V the best choice for the demanding requirements of voltage regulator solutions in Solar, Drives, Datacom and Telecom applications. Super fast switching Control FETs together with low EMI Sync FETs provide solutions that are easy to design in. OptiMOS™ products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space, efficiency and cost.



### Features

- Optimized for high switching frequency DC/DC converter
- Very low on-resistance  $R_{DS(on)}$
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Superior thermal resistance
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Double.sided cooling
- Compatible with DirectFET® package SJ footprint and outline
- Low profile (<0.7mm)
- Low parasitic inductance



### Applications

- Synchronous rectification
- Primary side switches
- Power managment for high performance computing
- High power density point of load converters



**Table 1 Key Performance Parameters**

Parameter	Value	Unit	Related Links
$V_{DS}$	100	V	<a href="#">IFX OptiMOS webpage</a> <a href="#">IFX OptiMOS product brief</a> <a href="#">IFX OptiMOS spice models</a> <a href="#">IFX Design tools</a>
$R_{DS(on),max}$	13.4	mΩ	
$I_D$	40	A	
$Q_{OSS}$	32	nC	
$Q_{g,typ}$	23		

Type	Package	Marking
BSF134N10NJ3 G	MG-WDSO-N-2	0210

1) J-STD20 and JESD22

## 2 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified.

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	40	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
				25		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
				9		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=45\text{ K/W}^1)$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	160		$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	70	mJ	$I_D=30\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	
Power dissipation	$P_{tot}$	-	-	43	W	$T_C=25\text{ °C}$
				2.2		$T_A=25\text{ °C}, R_{thJA}=58\text{ K/W}^1)$
Operating and storage temperature	$T_j, T_{stg}$	-40	-	150	°C	
IEC climatic category; DIN IEC 68-1		55/150/56				

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70µm thick) copper area for drain connection. PCB is vertical in still air

2) See figure 3 for more detailed information

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	2.9	K/W	top
		-	1	-		bottom
Device on PCB	$R_{thJA}$	-	-	58		6 cm <sup>2</sup> cooling area <sup>1)</sup>

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70µm thick) copper area for drain connection. PCB is vertical in still air

## 4 Electrical characteristics

Electrical characteristics, at  $T_J=25\text{ °C}$ , unless otherwise specified.

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	2.7	3.5		$V_{DS}=V_{GS}$ , $I_D=40\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1	10	$\mu\text{A}$	$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_J=25\text{ °C}$
		-	10	100		$V_{DS}=100\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_J=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	12.2	13.4	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$
		-	15.4	20		$V_{GS}=6\text{ V}$ , $I_D=15\text{ A}$
Gate resistance	$R_G$	-	0.5	-	$\Omega$	
Transconductance	$g_{fs}$	22	44		S	$ V_{DS}  > 2 I_D R_{DS(on)max}$ , $I_D=30\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1700	2300	$\text{pF}$	$V_{GS}=0\text{ V}$ , $V_{DS}=50\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	320	430		
Reverse transfer capacitance	$C_{riss}$	-	12	-		
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=50\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_G=1.6\text{ }\Omega$
Rise time	$t_r$	-	6	-		
Turn-off delay time	$t_{d(off)}$	-	15	-		
Fall time	$t_f$	-	5	-		

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	8	-	nC	$V_{DD}=50\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	4.1	-		
Switching charge	$Q_{sw}$	-	9	-		
Gate charge total	$Q_g$	-	23	30		
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	
Output charge	$Q_{oss}$		32	42		$V_{DD}=50\text{ V}$ , $V_{GS}=0\text{ V}$

1) See figure 16 for gate charge parameter definition

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_s$			36	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			160		
Diode forward voltage	$V_{SD}$	-	0.9	1.2	V	$V_{GS}=0\text{ V}$ , $I_F=I_s$ , $T_j=25\text{ °C}$
Reverse recovery charge	$t_{rr}$	-	59	-	nC	$V_R=50\text{ V}$ , $I_F=I_s$ , $di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery time	$Q_{rr}$	-	112	-	ns	

## 5 Electrical characteristics diagrams

Table 8

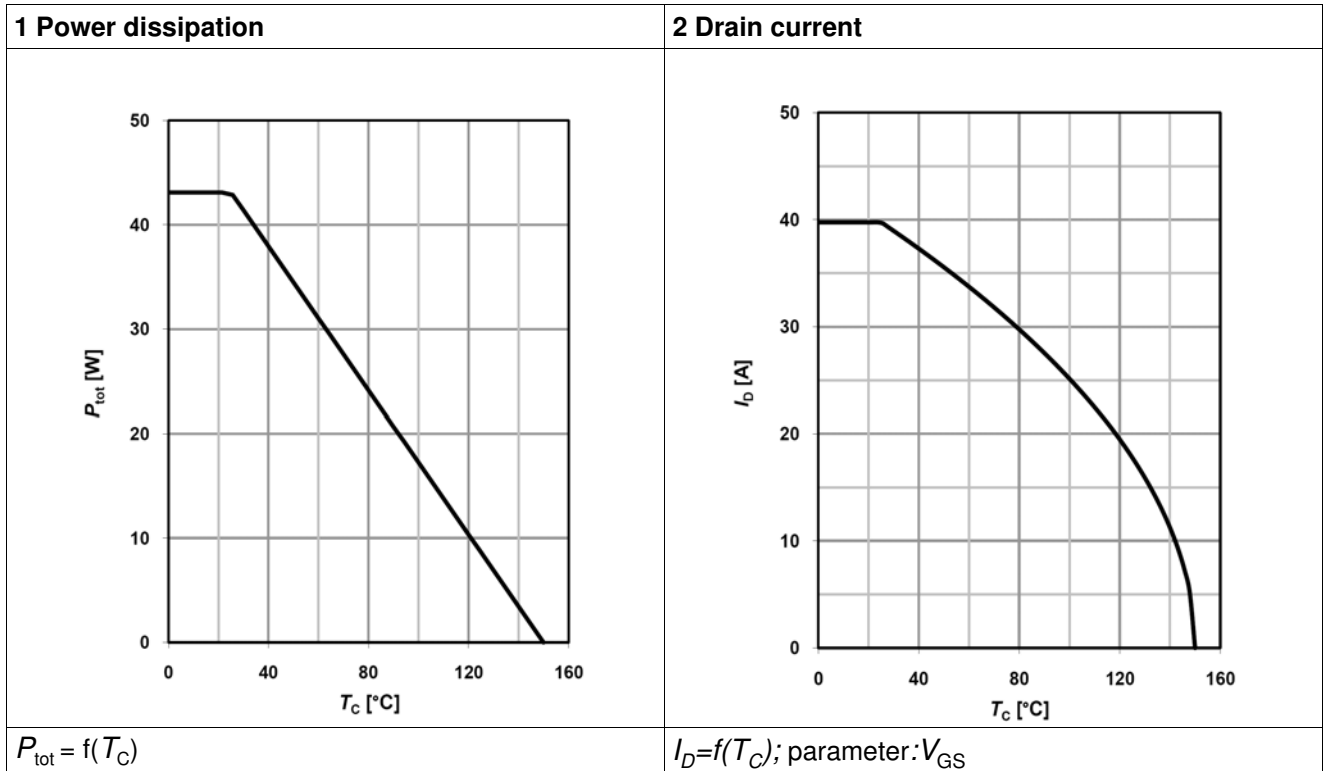


Table 9

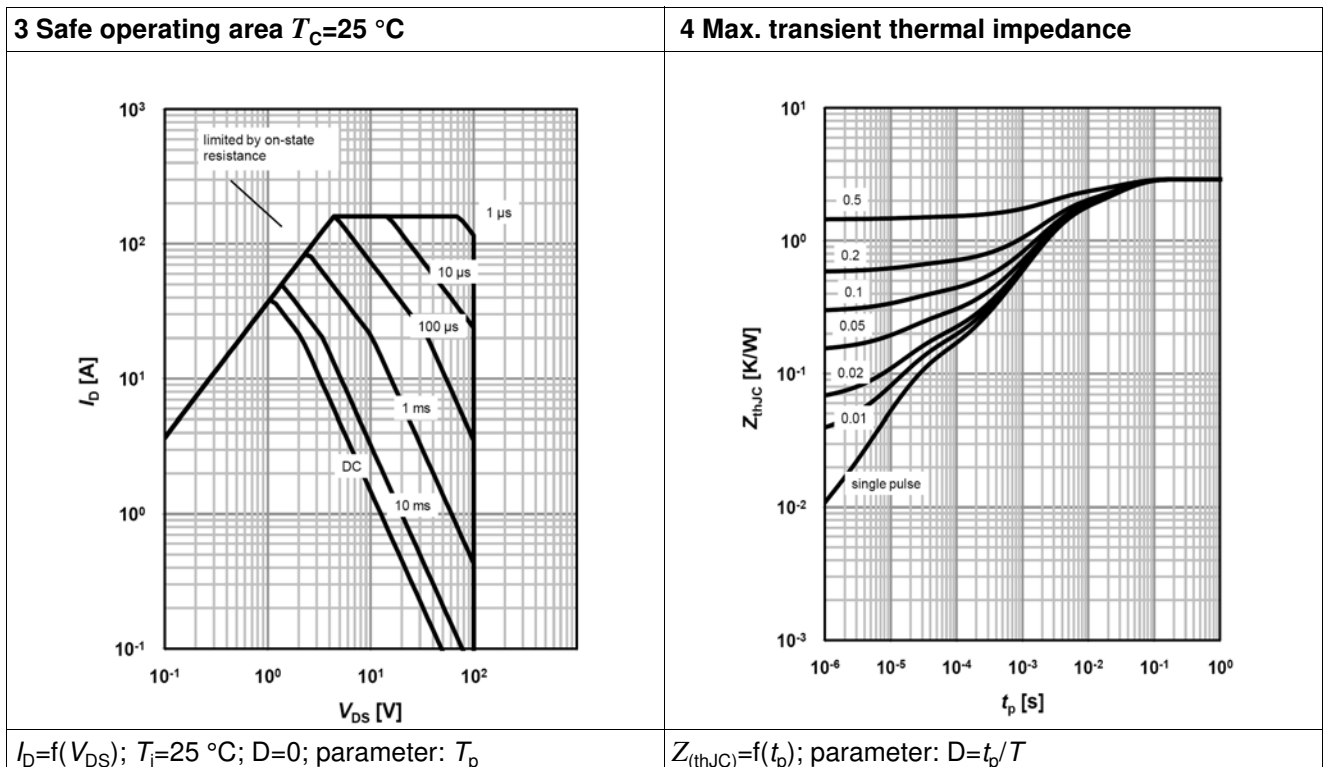


Table 10

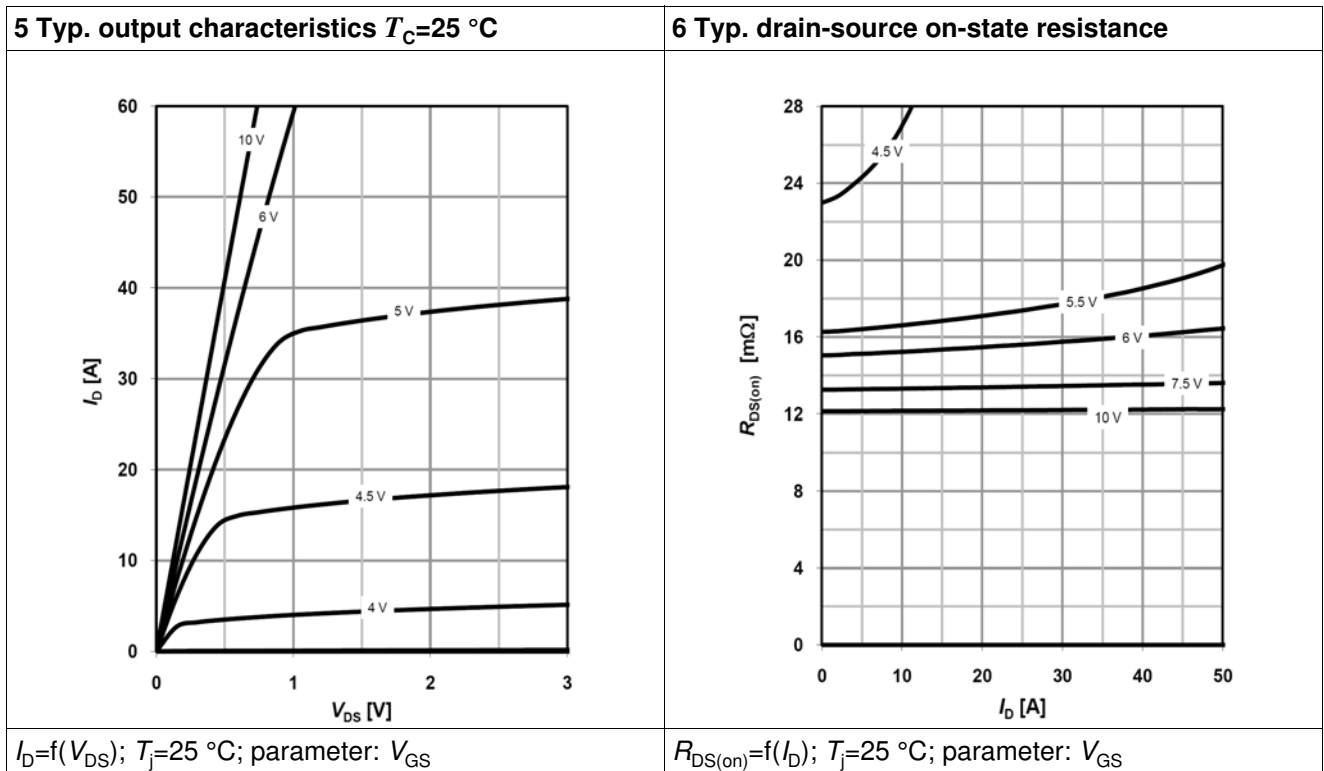


Table 11

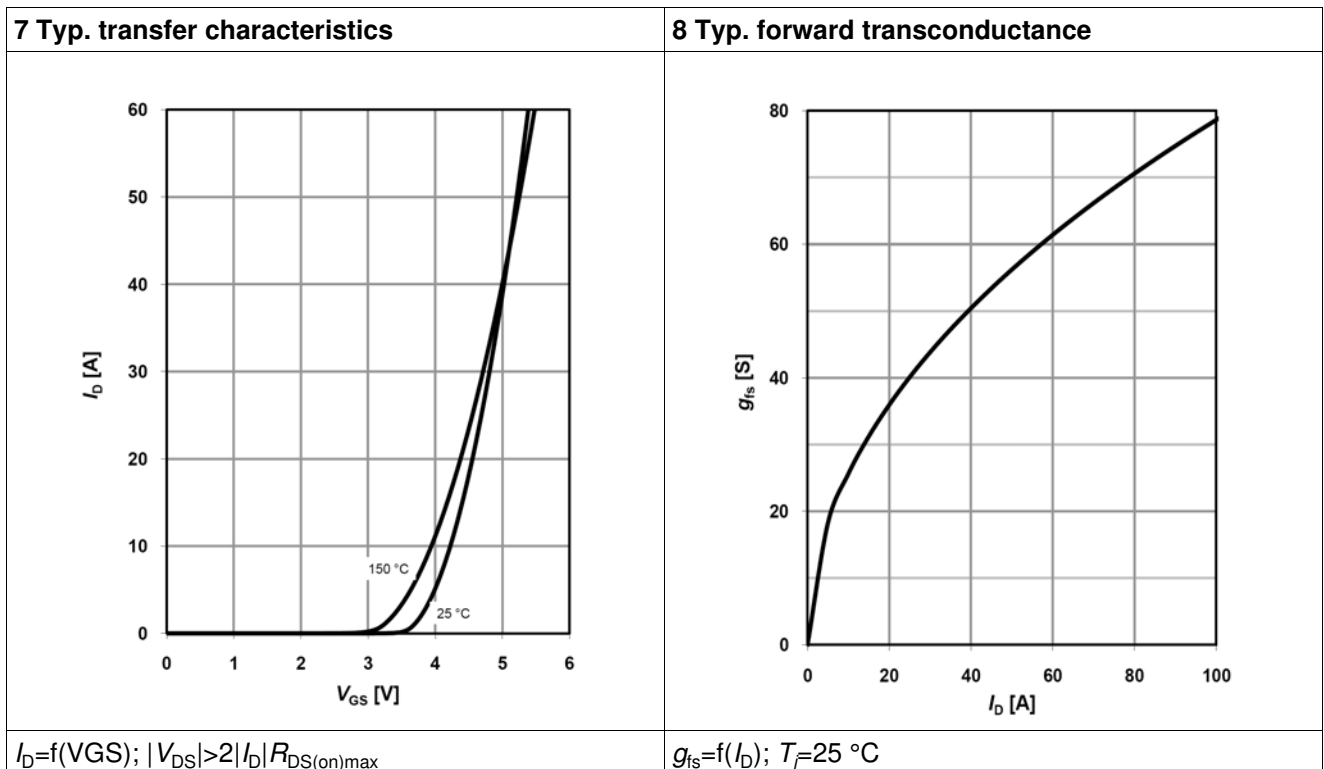


Table 12

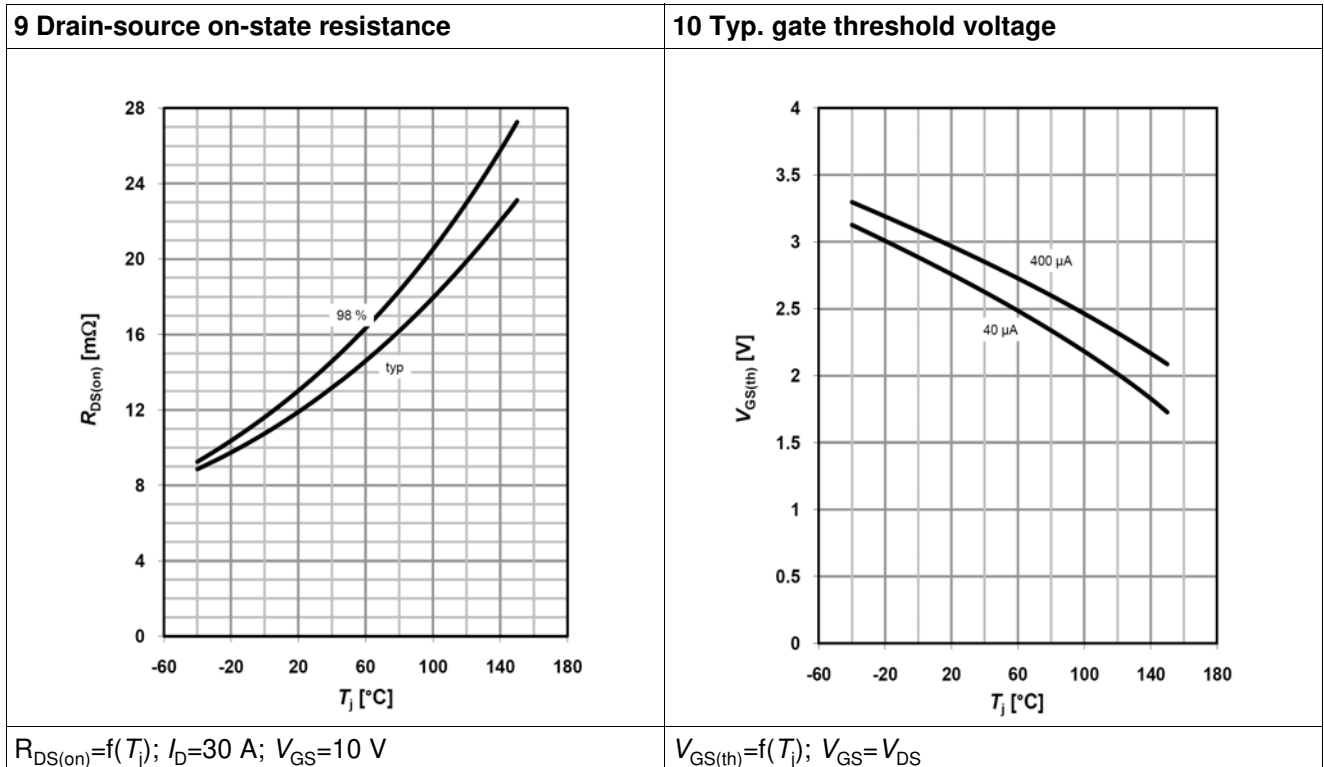


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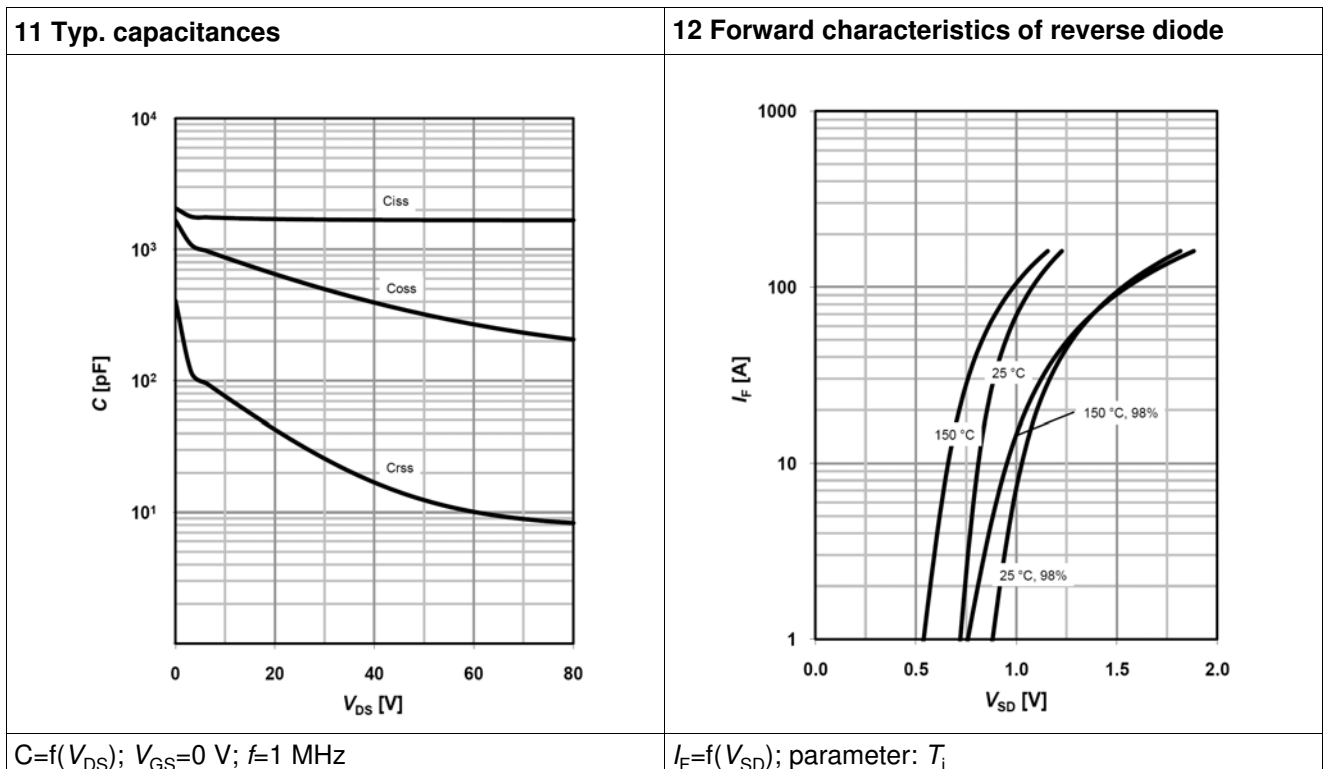




Table 14

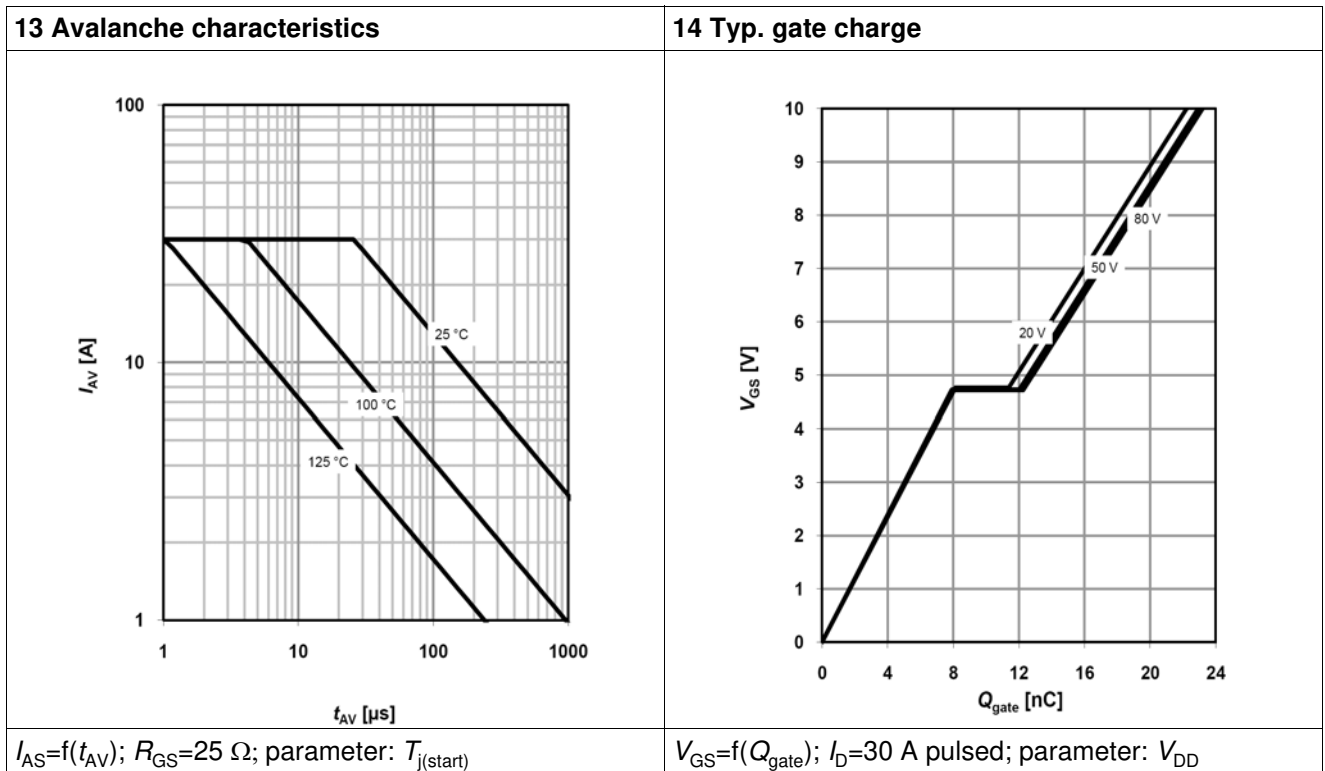
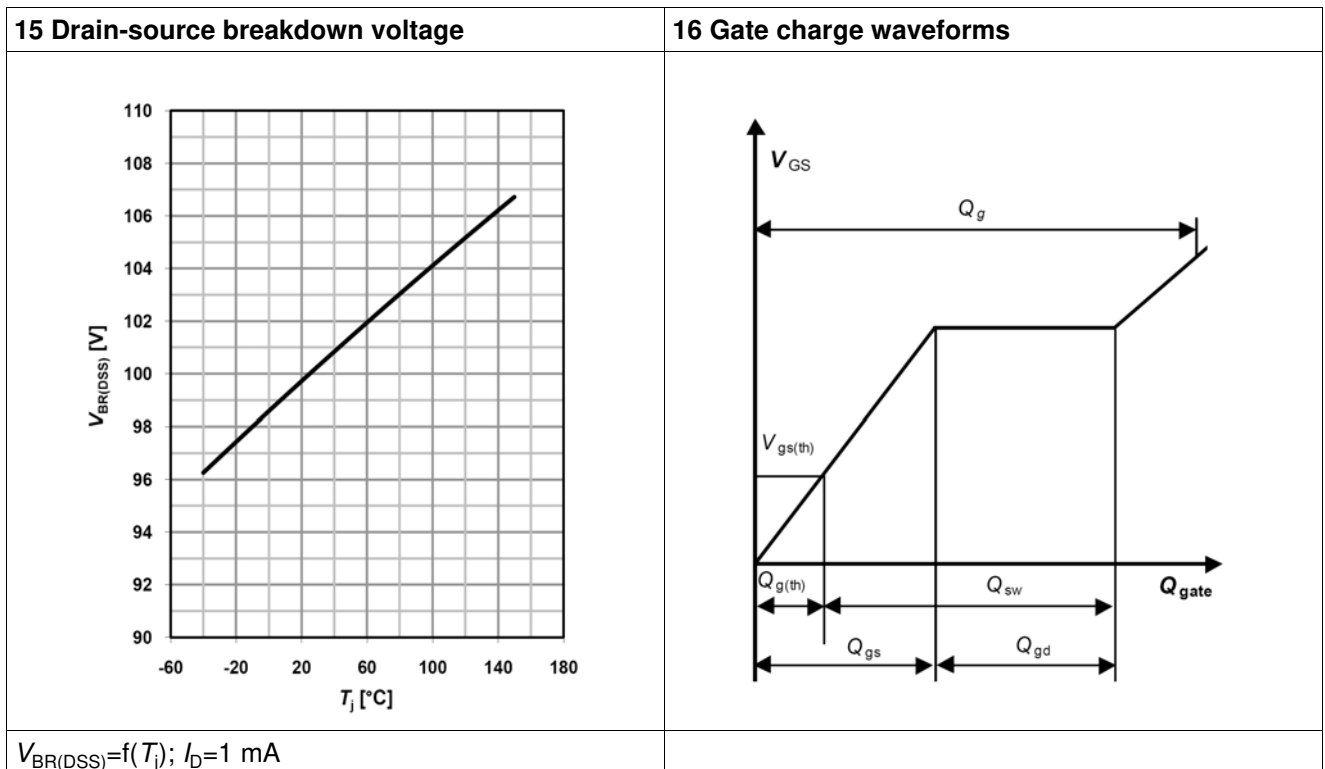


Table 15



## 6 Package outlines

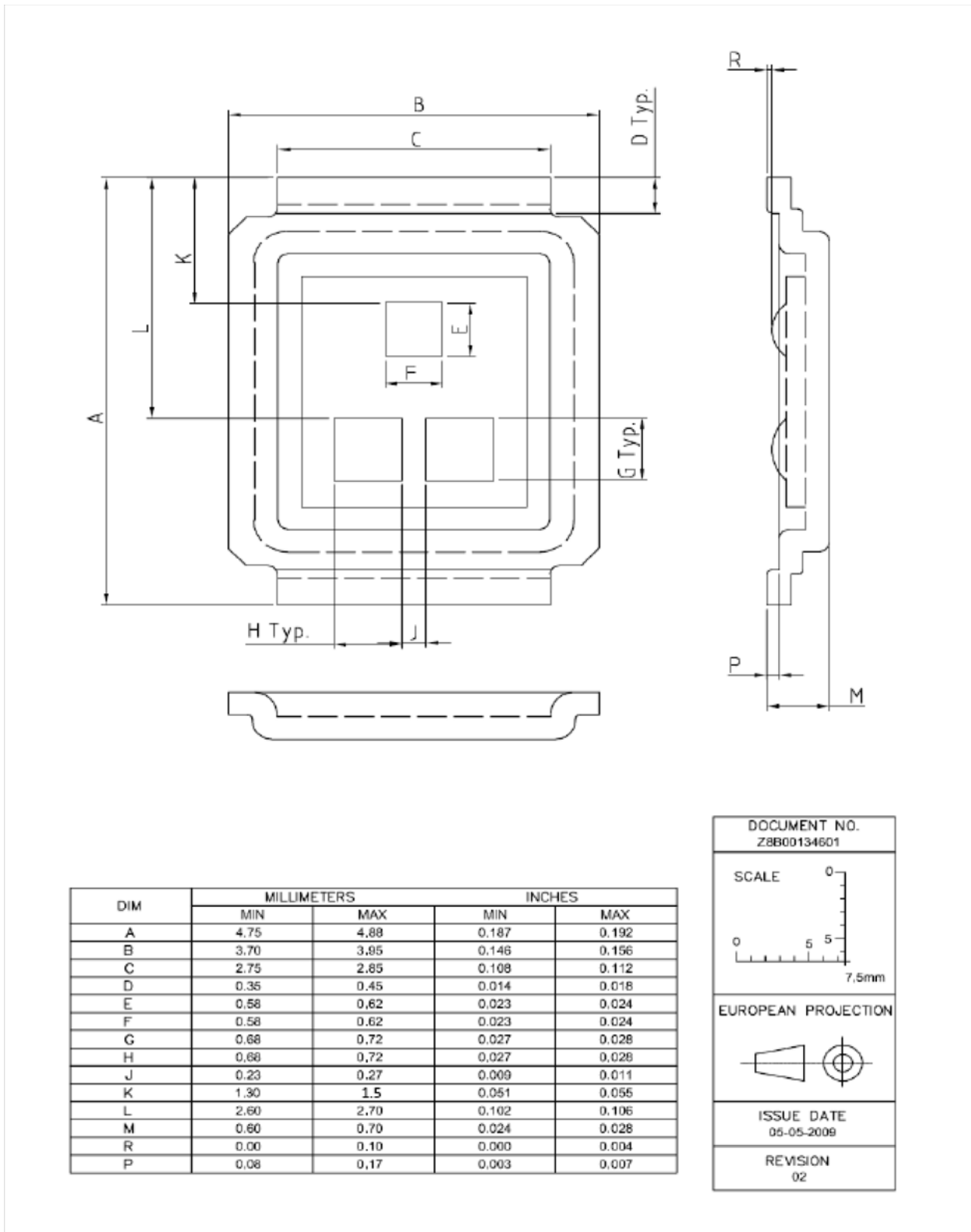


Figure 1 Outlines MG-WDSO-2, dimensions in mm/inches

7 Package outlines

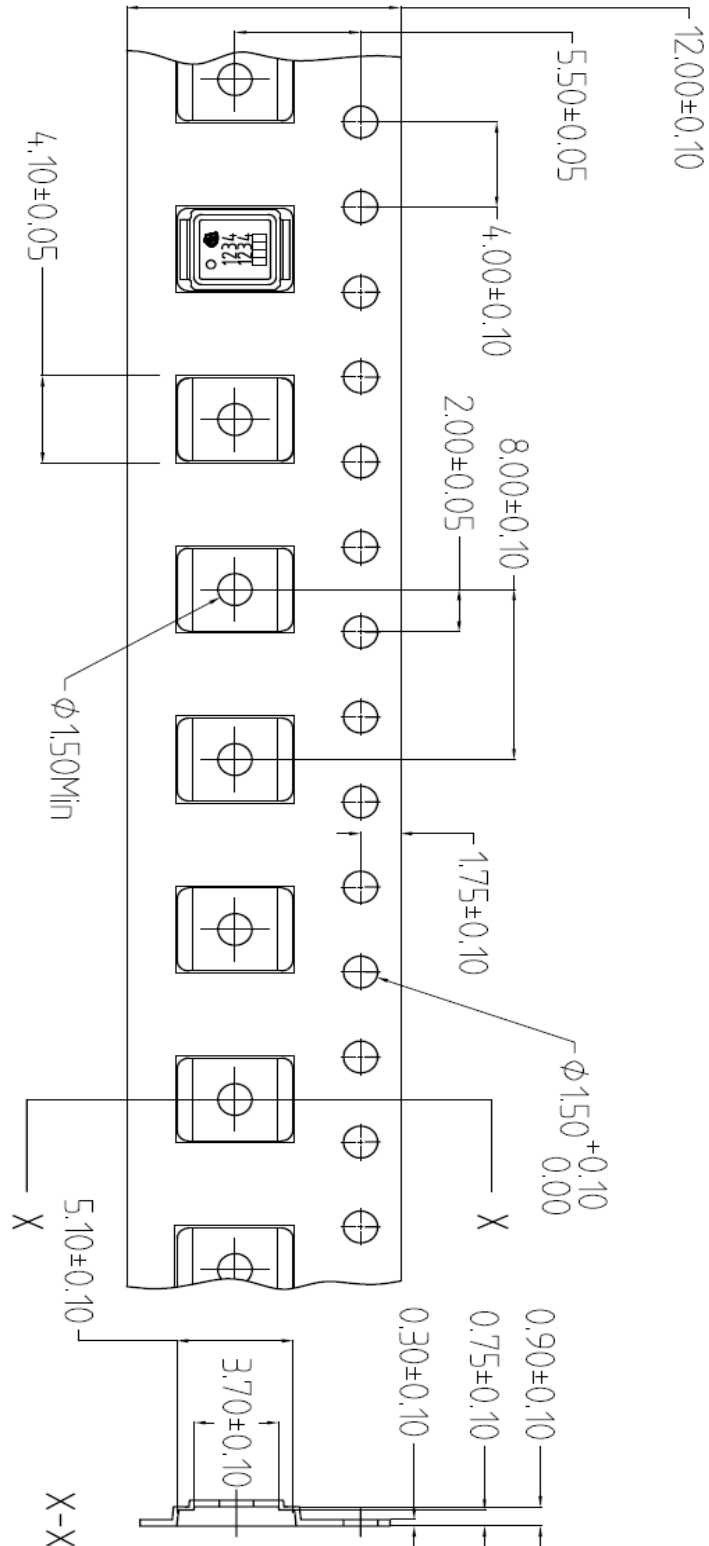
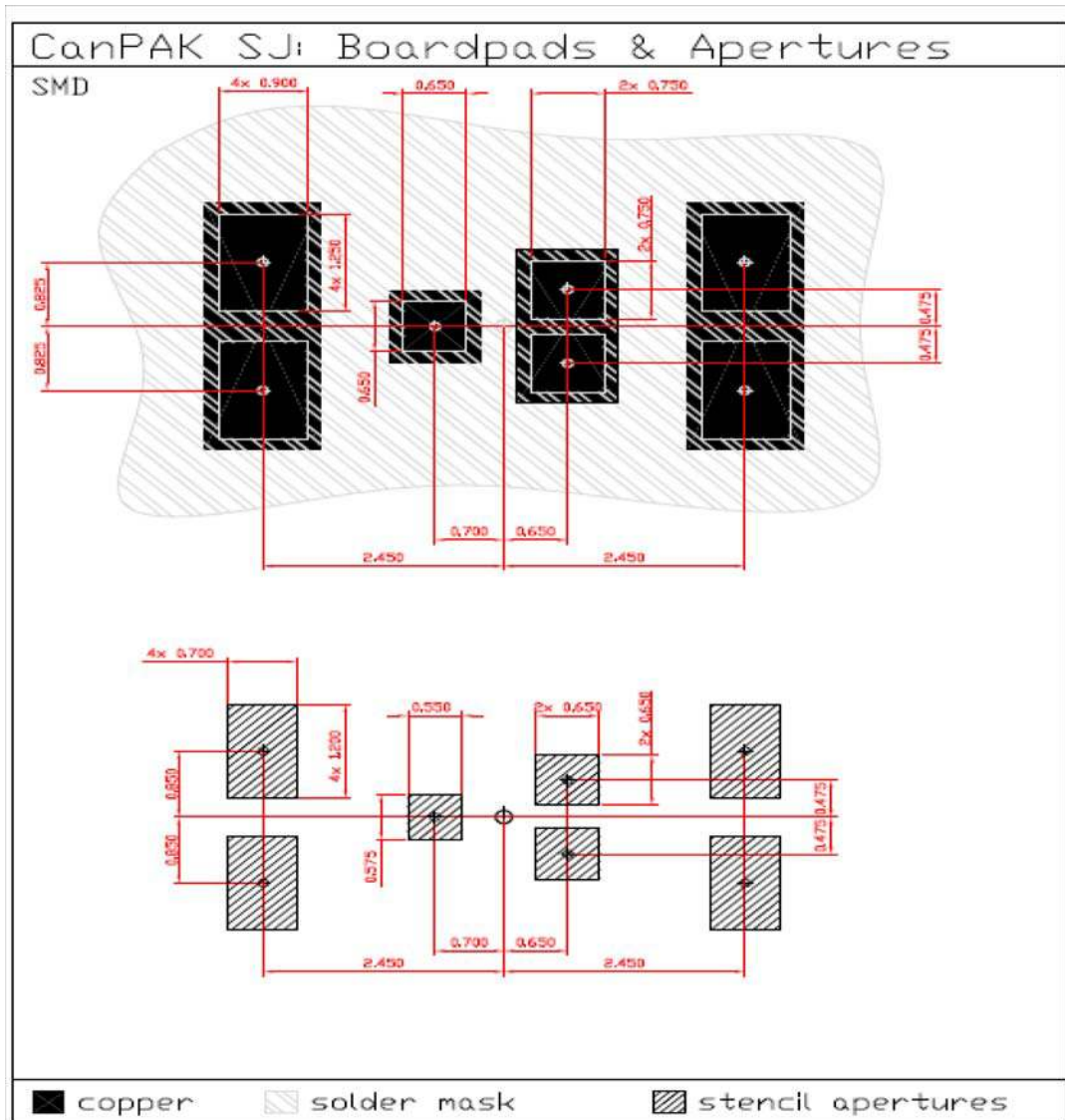
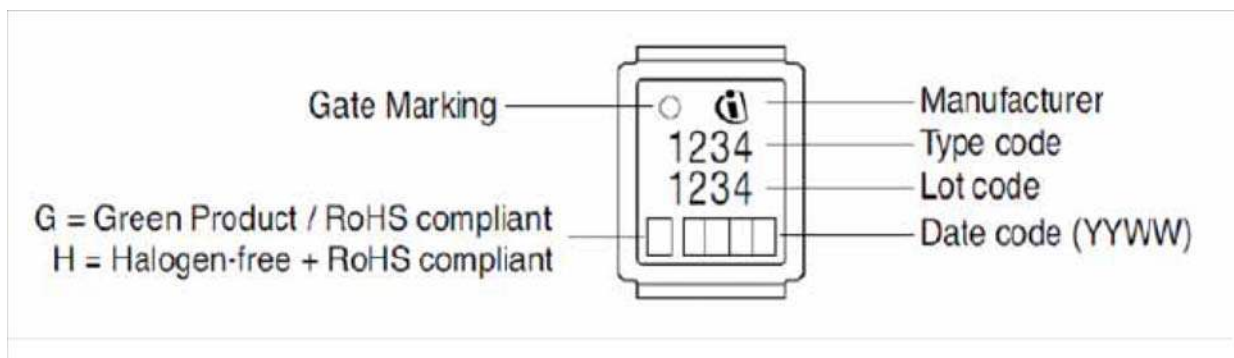


Figure 2 Outlines MG-WDSO-2, dimensions in mm/inches

## 8 Package outlines



## 9 Marking layout



## 9 Revision History

Revision History: 2011-05-31, 2.4

Previous Revision:

Revision	Subjects (major changes since last revision)
0.1	Release of target data sheet
1.0	Release Preliminary data sheet
2.2	Release Final data sheet
2.4	DirectFET Disclaimer expired

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