



Memory Module Data Sheet

Product Model Name : AD1U400A1G3

Product Specification : DDR-400(CL3) 184-Pin U-DIMM
1GB (128M x 64-bits)

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Version : 0

Item :

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Revision History

Version	Changes	Page	Date
0	- Initial release	-	2010/08/23

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AD1U400A1G3 DDR-400(CL3) 184-Pin U-DIMM 1GB (128M x 64-bits)

1. General Description :

The ADATA's module is a 128Mx64 bits 1024MB DDR-400(CL3)-3-3-8 SDRAM memory module. The SPD is programmed to JEDEC standard latency 400Mbps timing of 3-3-3-8 at 2.6V. The module is composed of six-teen 64Mx8 bits CMOS DDR SDRAMs in TSOP 66pin package and one 2Kbit EEPROM in 8pin SOIC package on a 184pin glass-epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 184-pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

2. Features :

- Power supply (Normal): VDD & VDDQ = 2.6V \pm 0.1V
- All inputs and outputs are compatible with SSTL_2 interface
- Programmable Read latency : DDR400(3 Clock)
- Programmable Burst Length (2, 4, 8) with both sequential and interleave mode
- Programmable Burst type (sequential & interleave)
- Differential clock input (CK, /CK)
- DLL aligns DQ and DQS transition with CK transition
- Double-data-rate architecture ; two data transfers per clock cycle
- Bidirectional data strobe [DQ] (x4,x8) & [L(U)DQS] (x16)
- Programmable Burst type (sequential & interleave)
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Lead-free products are RoHS Compliant

3. Pin Assignment :

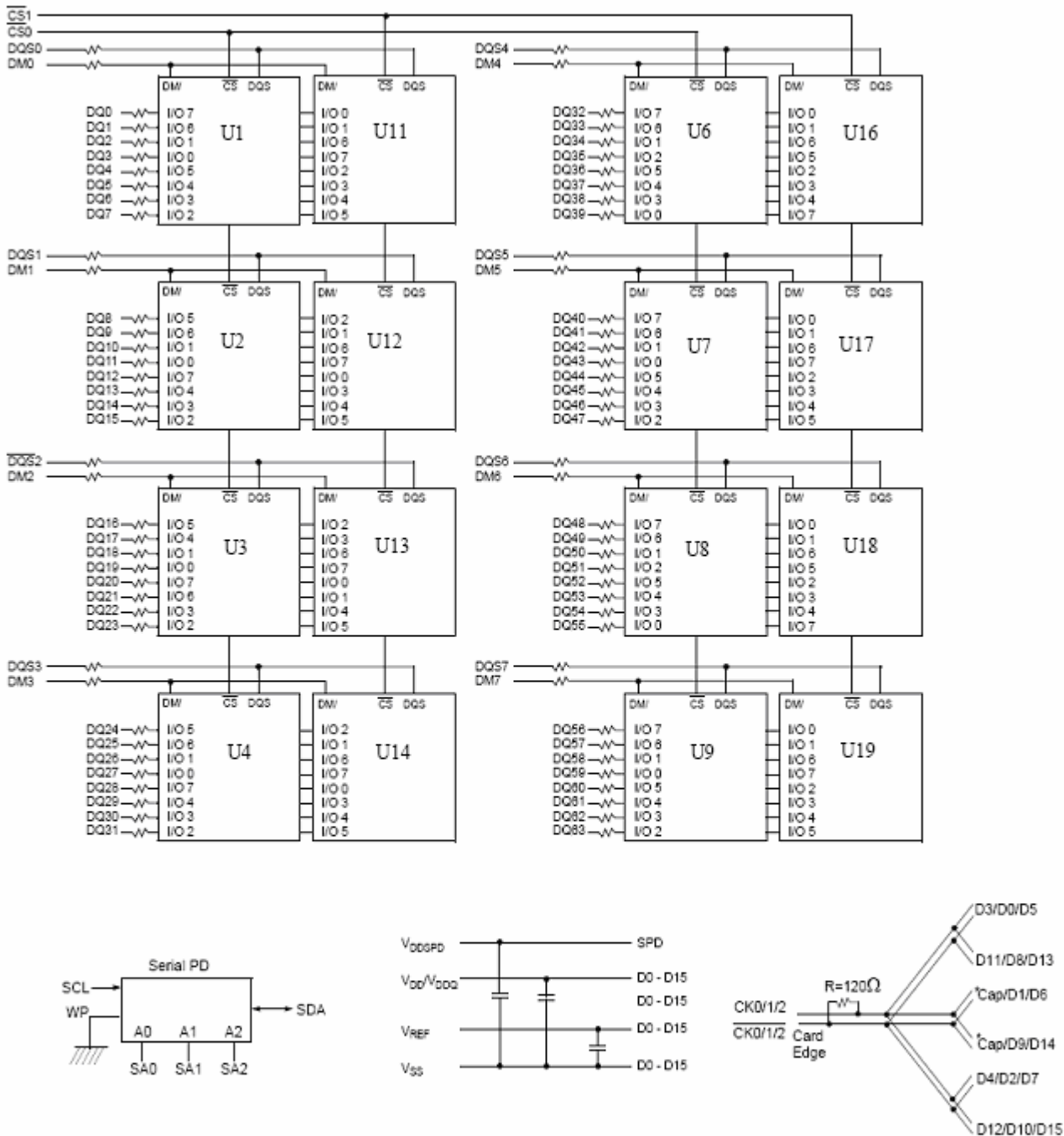
Front Side						Back Side					
PIN	Name	PIN	Name	PIN	Name	PIN	Name	PIN	Name	PIN	Name
1	VREF	32	A5	62	VDDQ	93	VSS	124	VSS	154	/RAS
2	DQ0	33	DQ24	63	/WE	94	DQ4	125	A6	155	DQ45
3	VSS	34	VSS	64	DQ41	95	DQ5	126	DQ28	156	VDDQ
4	DQ1	35	DQ25	65	/CAS	96	VDDQ	127	DQ29	157	/CS0
5	DQS0	36	DQS3	66	VSS	97	DM0	128	VDDQ	158	/CS1
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3	159	DM5
7	VDD	38	VDD	68	DQ42	99	DQ7	130	A3	160	VSS
8	DQ3	39	DQ26	69	DQ43	100	VSS	131	DQ30	161	DQ46
9	NC	40	DQ27	70	VDD	101	NC	132	VSS	162	DQ47
10	NC	41	A2	71	/CS2	102	NC	133	DQ31	163	/CS3
11	VSS	42	VSS	72	DQ48	103	NC	134	CB4	164	VDDQ
12	DQ8	43	A1	73	DQ49	104	VDDQ	135	CB5	165	DQ52
13	DQ9	44	CB0	74	VSS	105	DQ12	136	VDDQ	166	DQ53
14	DQS1	45	CB1	75	/CK2	106	DQ13	137	CK0	167	A13
15	VDDQ	46	VDD	76	CK2	107	DM1	138	/CK0	168	VDD
16	CK1	47	DQS8	77	VDDQ	108	VDD	139	VSS	169	DM6
17	/CK1	48	A0	78	DQS6	109	DQ14	140	DM8	170	DQ54
18	VSS	49	CB2	79	DQ50	110	DQ15	141	A10	171	DQ55
19	DQ10	50	VSS	80	DQ51	111	CKE1	142	CB6	172	VDDQ
20	DQ11	51	CB3	81	VSS	112	VDDQ	143	VDDQ	173	NC
21	CKE0	52	BA1	82	VDDID	113	BA2	144	CB7	174	DQ60
22	VDDQ			83	DQ56	114	DQ20			175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	VSS	176	VSS
24	DQ17	54	VDDQ	85	VDD	116	VSS	146	DQ36	177	DM7
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	DQ11	56	DQS4	87	DQ58	118	A11	148	VDD	179	DQ63
27	CKE0	57	DQ34	88	DQ59	119	DM2	149	DM4	180	VDDQ
28	VDDQ	58	VSS	89	VSS	120	VDD	150	DQ38	181	SA0
29	DQ16	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	DQ17	60	DQ35	91	SDA	122	A8	152	VSS	183	SA2
31	DQS2	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	VDDSPD

4. Pin Description :

PIN	NAME	FUNCTION
A0~A12	Address	Row / Column address are multiplexed on the same pins.
BA0~BA1	Banks Select	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
DQ0~DQ63	Data	Data inputs / outputs are multiplexed on the same pins.
DQS0~DQS8	Data Strobe	Bi-directional Data Strobe
CK0~CK2	System Clock	Clock Inputs.
/CK0 ~ /CK2	System Clock	Differential clock inputs
CKE0,CKE1(for 2 rank)	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby
/CS0,/CS1(for 2 rank)	Chip Select	Disables or Enables device operation by masking or enabling all input except CK, CKE and L(U)DQM
/RAS	Row Address Strobe	Latches row addresses on the positive edge of the CK with /RAS low
/CAS	Column Address Strobe	Latches Column addresses on the positive edge of the CK with /CAS low
/WE	Write Enable	Enables write operation and row recharge.
DM0~DM7,8(for ECC)	Data Mask	Mask input data when DM is high.
VDD/ VDDQ	Power Supply	Power for the input buffers and the core logic.
VSS	Power Supply	Ground for the input buffers and the core logic.
VREF	Power Supply reference	Power Supply for reference
VDDSPD	SPD Power Supply	Serial EEPROM power Supply
SDA	Serial data I/O	EEPROM serial data I/O
SCL	Serial clock	EEPROM clock input
SA0~2	Address in EEPROM	EEPROM address input
VDDID	VDD identification	VDD identification flag
NC	No Connection	This pin is recommended to be left No Connection on the device.

5. Block Diagram :

(Populated as 2 Rank of x8 DDR SDRAM Module)



BA0 - BA1 → BA0-BA1 : All DDR SDRAMs
A0 - A12 → A0-A12: All DDR SDRAMs
 $\overline{\text{RAS}}$ → $\overline{\text{RAS}}$: All DDR SDRAMs
 $\overline{\text{CAS}}$ → $\overline{\text{CAS}}$: All DDR SDRAMs
CKE 0/1 → CKE : All DDR SDRAMs
 $\overline{\text{WE}}$ → $\overline{\text{WE}}$: All DDR SDRAMs

* Clock Wiring	
Clock Input	DDR SDRAMs
*CK0/CK0	4 DDR SDRAMs
*CK1/CK1	6 DDR SDRAMs
*CK2/CK2	6 DDR SDRAMs

*Clock Net Wiring

Note :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DM/CKE/ $\overline{\text{CS}}$ relationships must be maintained as shown.
3. DQ, DQS, DM/DQS resistors: 22 Ohms \pm 5%.

6. Absolute Maximum Ratings :

Parameter	Symbol	Value	Unit
Operating Temperature (Ambient)	TA	0 ~ 70	°C
Voltage on VDD supply relative to Vss	VDD	-1.0 ~ 3.6	V
Voltage on VDDQ supply relative to Vss	VDDQ	-1.0 ~ 3.6	V
Voltage on any pin relative to Vss	VIN, Vout	-0.5 ~ 3.6	V
Storage temperature	TSTG	-55 ~ 100	°C
Short circuit current	IOS	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

7. DC Operating Condition :

Recommended operating conditions(Voltage referenced to Vss=0V, TA=0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Note
Supply voltage	VDD, VDDQ	2.5	2.7	V	1
Reference voltage	VREF	VDDQ*0.49	VDDQ*0.51	V	2
Termination voltage	VTT	VREF-0.04	VREF+0.04	V	
Input logic high voltage	VIH	VREF+0.15	VDDQ+0.3	V	
Input logic low voltage	VIL	-0.3	VREF-0.15	V	3
Input voltage Level	VIN	-0.3	VDDQ+0.3	V	
Input Differential Voltage	VID	0.36	VDDQ+0.6	V	4
V-I Matching: Pullup to Pulldown current ratio	VI (ratio)	0.71	1.4	V	
Input leakage current	IL	-2	+2	uA	5
Output leakage current	IOZ	-5	5	uA	6
Output logic high voltage	VOH	VTT+0.76	-	V	IOH=-15.2mA
Output logic low voltage	VOL	-	VTT-0.76	V	IOL=15.2mA

Note : 1. VDDQ must not exceed the level of VDD.

2. The value of VREF is approximately equal to 0.5*VDDQ

3. VIL(min) is acceptable -1.5V AC pulse width with ≤ 5 ns of duration.

4. VID is the magnitude of the difference between the input level on CK and the input level on /CK.

5. VIN=0 to 3.6 V, All other pins are not tested under VIN=0V

6. DQ is disabled, Vout = 0 to 2.7V

8. AC Operating Condition :

Parameter	Symbol	Min	Max	Unit	Note
Input High (Logic 1) Voltage, DQ, DQS and DM signals	VIH	VREF +0.31	-	V	
Input Low (Logic 0) Voltage, DQ, DQS and DM signals	VIL	-	VREF-0.31	V	
Input Differential Voltage, CK and /CK inputs	VID	0.7	VDDQ+0.6	V	1
Input Crossing Point Voltage, CK and /CK inputs	VIX	0.5*VDDQ-0.2	0.5*VDDQ+0.2	V	2

Note: 1. VID is the magnitude of the difference between the input level on CK and the input level on /CK.

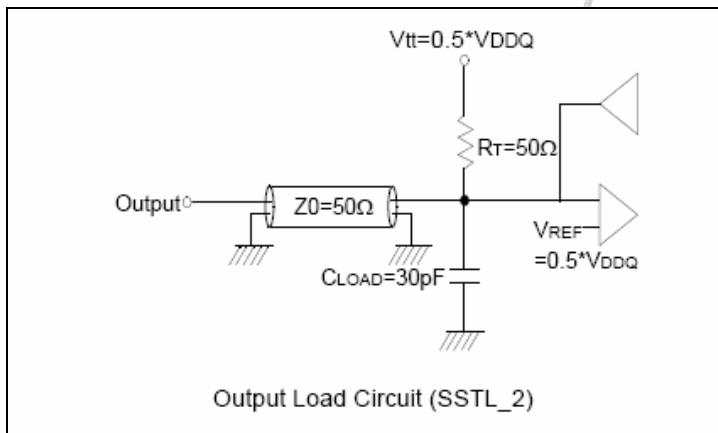
2. VIX is expected to be equal to 0.5*VDDQ of the transmitting device and must track variations in the dc level of the same.

9. AC Operation Test Condition :

(Voltage referenced to $V_{SS} = 0V$, $T_A=0$ to $70^{\circ}C$)

Parameter	Value	Unit
Reference Voltage	$V_{DDQ} \cdot 0.5$	V
Termination Voltage	$V_{DDQ} \cdot 0.5$	V
AC Input High Level Voltage (V_{IH} , min)	$V_{REF} + 0.31$	V
AC Input Low Level Voltage (V_{IL} , max)	$V_{REF} - 0.31$	V
Input Timing Measurement Reference Level Voltage	V_{REF}	V
Output Timing Measurement Reference Level Voltage	V_{TT}	V
Input Signal Maximum peak swing	1.5	V
Input signal Minimum Slew Rate	1	V/ns
Termination Resistor (R_T)	50	Ohm
Series Resistor (R_S)	25	Ohm
Output Load Capacitance For Access Time Measurement	30	pF

Output load circuit



10. IDD Specification and Conditions :

(TA=0 to 70°C, Voltage referenced to Vss = 0V)

Symbol	Condition	Typical	Unit
IDD0	One bank Active-Precharge	1,440	mA
IDD1	One bank Active-Read-Precharge	1,680	mA
IDD2P	Precharge power-down standby current	80	mA
IDD2F	Precharge floating standby current	480	mA
IDD3P	Active power-down standby current	720	mA
IDD3N	Active standby current	960	mA
IDD4R	Operating current-burst read	1,720	mA
IDD4W	Operating current-burst write	1,880	mA
IDD5	Auto refresh current	2,240	mA
IDD6	Self refresh current	80	mA
IDD7	Operating current-Four bank operation	3,560	mA

Note :: Module IDD was calculated on the basis of component IDD. Only for reference.

11. AC Characteristics :

Parameter	Symbol	Min	Max	Unit
Row cycle time	tRC	55	-	ns
Refresh row cycle time	tRFC	70	-	ns
Row active time	tRAS	40	70K	ns
/RAS to /CAS delay	tRCD	15	-	ns
/RAS to /RAS bank active delay	tRRD	10	-	ns
/RAS precharge time	tRP	15	-	ns
Write recovery time	tWR	15	-	ns
Write to Read command Delay	tWTR	2	-	tCK
Auto Precharge Write Recovery + Precharge	tDAL	(tWR/ tCK) + (tRP/ tCK)	-	tCK
System clock Cycle time	/CAS Latency =3 tCK	5	10	ns
Clock High Level Width	tCH	0.45	0.55	tCK
Clock Low Level Width	tCL	0.45	0.55	tCK
Access time form clock	tAC	-0.65	+0.65	ns
DQS out access time from CK /CK	tDQSCK	-0.55	+0.55	ns
Data strobe edge to output data edge	tDQSQ	-	+0.4	ns
Data-Out hold time from DQS	tQH	tHP - tQHS	-	ns
Clock Half Period	tHP	Min(tCH, tCL)	-	ns

Data Hold Skew Factor	tQHS	-	+0.5	ns
Data-out high-impedance window from CK, /CK	tHZ	-0.65	+0.65	ns
Data-out low-impedance window from CK, /CK	tLZ	-0.65	+0.65	ns
Address/Control input setup time (fast slew rate)	tIS	0.6	-	ns
Address/Control input hold time (fast slew rate)	tIH	0.6	-	ns
Address/Control input setup time (slow slew rate)	tIS	0.7	-	ns
Address/Control input hold time (slow slew rate)	tIH	0.7	-	ns
Input Pulse Width	tIPW	2.2	-	ns
DQS in high level width	tDQSH	0.35	-	tCK
DQS in low level width	tDQSL	0.35	-	tCK
CK to valid DQS-in	tDQSS	0.72	1.28	tCK
DQS falling edge to CK setup time	tDSS	0.2	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	-	tCK
DQ & DM input setup time	tDS	0.4	-	ns
DQ & DM input hold time	tDH	0.4	-	ns
DQ & DM Input Pulse Width	tDIPW	1.75	-	ns
Read DQS Preamble Time	tRPRE	0.9	1.1	tCK
Read DQS Postamble Time	tRPST	0.4	0.6	tCK
DQS-in setup time	tWPRES	0	-	tCK
DQS-in hold time	tWPREH	0.25	-	tCK
DQS write postamble Time	tWPST	0.4	0.6	tCK
MRS to new command	tMRD	10	-	ns
Exit Self Refresh to non-Read command	tXSNR	75	-	ns
Exit Self Refresh to Read command	tXSRD	200	-	tCK
Average Periodic Refresh Interval	tREFI	-	7.8	us

12. System Characteristics Conditions :

(The following tables are described specification parameters that required in systems using DDR devices to ensure proper performance. These characteristics are for system simulation purposes and are guaranteed by design.)

Inputs Slew Rate for DQ,DQS, and DM

Parameter	Symbol	Min	Max	Unit
DQ/DQM/DQS input slew rate measured between VIH(DC), VIL(DC) and VIL(DC), VIH(DC)	DCSLEW	0.5	4	V/ns

Inputs Setup & Hold Time Derating for Slew Rate

Input Slew Rate	Delta tIS	Delta tIH	Unit
0.5 V/ns	0	0	ps
0.4 V/ns	+50	0	ps
0.3 V/ns	+100	0	ps

Inputs/ Outputs Setup & Hold Time Derating for Slew Rate

Input Slew Rate	Delta tDS	Delta tDH	Unit
0.5 V/ns	0	0	ps
0.4 V/ns	+75	+75	ps
0.3 V/ns	+150	+150	ps

Inputs/ Outputs Setup & Hold Time Derating for Rise/Fall Delta Slew Rate

Input Slew Rate	Delta tDS	Delta tDH	Unit
+/-0.0 V/ns	0	0	ps
+/-0.25 V/ns	+50	+50	ps
+/-0.5 V/ns	+100	+100	ps

Output Slew Rate Characteristics(x4,x8 device only)

Slew Rate Characteristic	Typical Range	Min	Max	Unit
Pullup Slew Rate	1.2 ~ 2.5	1.0	4.5	V/ns
Pulldown Slew Rate	1.2 ~ 2.5	1.0	4.5	V/ns

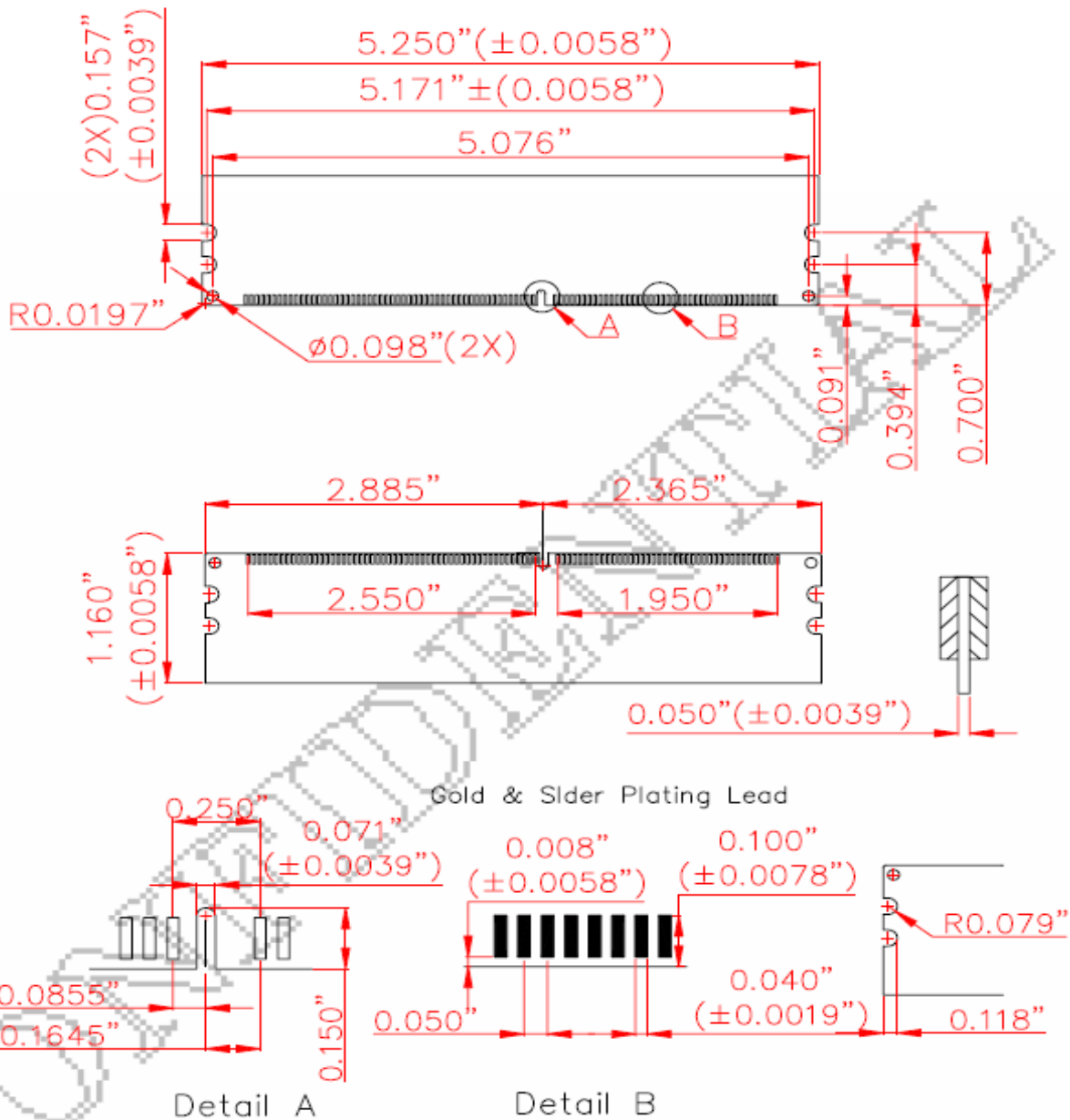
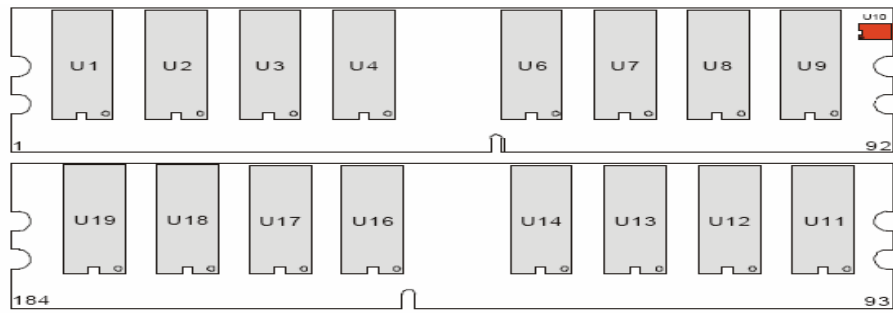
Output Slew Rate Characteristics(x16 device)

Slew Rate Characteristic	Typical Range	Min	Max	Unit
Pullup Slew Rate	1.2 ~ 2.5	0.7	5.0	V/ns
Pulldown Slew Rate	1.2 ~ 2.5	0.7	5.0	V/ns

13. Command Truth-Table :

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	ADDR	A10/AP	BA
Mode Register Set		H	X	L	L	L	L	OP code		
No Operation		H	X	L	H	H	H	X		
Bank Active		H	X	L	L	H	H	RA		V
Read	Read with Auto Precharge	H	X	L	H	L	H	CA	L	V
									H	
Write	Write with Auto Precharge	H	X	L	H	L	L	CA	L	V
									H	
Precharge All Bank		H	X	L	L	H	L	X	H	X
Precharge select Bank									L	V
Burst Stop		H	X	L	H	H	L	X		
Auto Refresh		H	H	L	L	L	H	X		
Self Refresh	Entry	H	L	L	L	L	H	X		
	Exit	L	H	L	H	H	H			
H				X	X	X				
Precharge	Entry	H	L	H	X	X	X	X		
				L	H	H	H			
Power down	Exit	L	H	H	X	X	X			
				L	V	V	V			
Active Power Down	Entry	H	L	H	X	X	X	X		
				L	V	V	V			
	Exit	L	H	X	X	X	X			

14. Package Dimensions :



Note :

All dimensions are in millimeters (inches) and should be kept within a tolerance of $\pm 0.127 (\pm 0.005'')$ unless otherwise specified.