20V, 2.5A Synchronous Monolithic Step-Down Regulator with Current and Temperature Monitoring

FEATURES

- **3.6V to 20V Input Voltage Range**
- **Wide Output Voltage Range of 0.6V to 97% V_{IN} Optimized for 0.6V to 6V**
- **Low $R_{DS(ON)}$ Integrated Switches Provide Up to 95% Efficiency**
- **Up to 2.5A of Output Current**
- **Average Input and Output Current Monitoring**
- **Programmable Average Input/Output Current Limit**
- **Die Temperature Monitor and Programmable Limit**
- **Adjustable Switching Frequency: 500kHz to 3MHz**
- **External Frequency Synchronization**
- **Current Mode Operation for Excellent Line and Load Transient Response**
- **0.6V Reference with 1% Accuracy Over Temperature**
- User Selectable Burst Mode® Operation or Forced Continuous Operation
- Short-Circuit Protected
- Output Voltage Tracking Capability
- Power Good Status Output
- Available in Small, Thermally Enhanced, 20-Lead (3mm × 4mm) QFN Package

APPLICATIONS

- Distributed Power Systems
- Battery-Powered Instruments
- Point-of-Load Power Supply

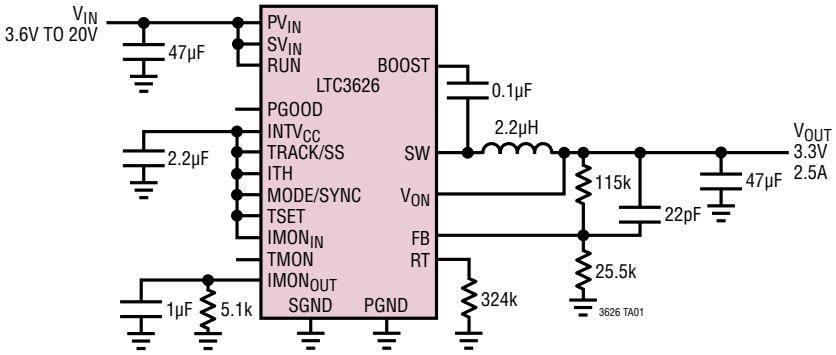
DESCRIPTION

The LTC®3626 is a high efficiency, monolithic synchronous buck regulator using a phase-lockable controlled on-time, current mode architecture capable of supplying up to 2.5A of output current. The operating supply voltage range is 3.6V to 20V, making it suitable for a wide range of power supply applications.

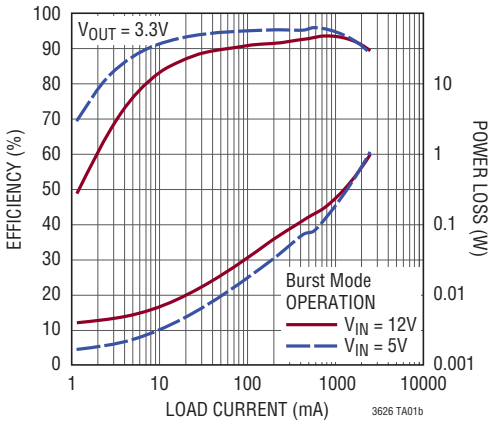
The operating frequency is programmable from 500kHz to 3MHz with an external resistor allowing the use of small surface mount inductors. For applications sensitive to switching noise, the LTC3626 can be externally synchronized over the same frequency range. An internal phase-locked loop aligns the on-time of the top power MOSFET to the internal or external clock. This unique controlled on-time architecture is ideal for high step-down ratio applications that demand high switching frequencies and fast transient response. An internal phase lock loop servos the on-time of the internal one-shot timer to match the frequency of the internal clock or an applied external clock.

The LTC3626 offers two operational modes: Burst Mode and forced continuous mode to allow the user to optimize output voltage ripple, noise and light load efficiency for a given application.

TYPICAL APPLICATION



Efficiency vs Load Current

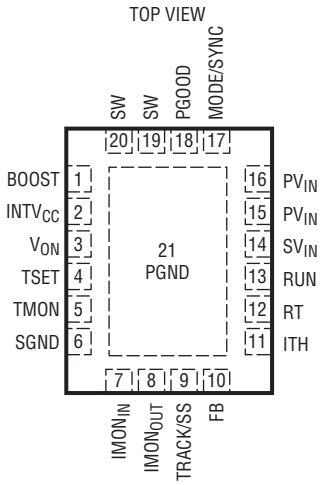


ABSOLUTE MAXIMUM RATINGS

(Note 1)

PV_{IN} ..... –0.3V to 22V
SV_{IN} ..... –0.3V to 22V
BOOST ..... –0.3V to 25.6V
BOOST-SW..... –0.3V to 3.6V
$INTV_{CC}$ ..... –0.3V to 3.6V
ITH, RT, FB.....–0.3V to $INTV_{CC}$ + 0.3V
MODE/SYNC .....–0.3V to $INTV_{CC}$ + 0.3V
TRACK/SS, $IMON_{IN}$, $IMON_{OUT}$...–0.3V to $INTV_{CC}$ + 0.3V
TSET, TMON .....–0.3V to $INTV_{CC}$ + 0.3V
SW, RUN ..... –0.3V to V_{IN} + 0.3V
PGOOD..... –0.3V to 22V
V_{ON} ..... –0.3V to 18V
SW Source Current (DC, Note 2).....2.5A
Operating Junction Temperature Range
(Notes 3, 4) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 47°C/W
EXPOSED PAD (PIN 21) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3626EUDC#PBF	LTC3626EUDC#TRPBF	LGCC	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3626IUDC#PBF	LTC3626IUDC#TRPBF	LGCC	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). PV_{IN} = SV_{IN} = 12V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PV_{IN}	Input Supply Range		●	3.0		20	V
SV_{IN}	Input Supply Range		●	3.6		20	V
V_{VOUT}	Output Voltage Range (Note 5)	V_{ON} = V_{OUT}		0.6		6	V
I_Q	Input DC Supply Current Forced Continuous Operation PV_{IN} SV_{IN}	MODE = 0, R_{RT} = 158k, $IMON_{IN}$, $IMON_{OUT}$, TMON, TSET = $INTV_{CC}$			 30 900	 39 1200	 µA µA
	Sleep Current PV_{IN} SV_{IN}	V_{FB} > 0.6V, $IMON_{IN}$, $IMON_{OUT}$, TMON, TSET, MODE = $INTV_{CC}$			 30 270	 39 350	 µA µA
	Shutdown PV_{IN} SV_{IN}	I_{LOAD} = 0A, V_{RUN} = 0V			 0.01 13	 2 17	 µA µA
V_{FB}	Feedback Reference Voltage		●	0.594	0.600	0.606	V
$\Delta V_{LINE(REG)}$	V_{FB} Line Regulation	PV_{IN} = SV_{VIN} = 3.6V to 20V			0.01		%/V
$\Delta V_{LOAD(REG)}$	V_{FB} Load Regulation	ITH = 0.6V to 1.5V			0.1		%
	Feedback Pin Input Current	V_{FB} = 0.6V				±30	nA
	Error Amplifier Transconductance	ITH = 1.2V			1.5		mS
$t_{ON(MIN)}$	Minimum On-Time	V_{VON} =1V, PV_{IN} = SV_{VIN} = 3.6V			20		ns
$t_{OFF(MIN)}$	Minimum Off-Time	PV_{IN} = SV_{IN} = 6V			40	60	ns
	Valley Switch Current Limit			2.4	2.9	3.6	A
	Negative Valley Switch Current Limit				–1		A
f_{OSC}	Oscillator Frequency	V_{RT} = $INTV_{CC}$ R_{RT} = 158k R_{RT} = 105k		1.4 1.7 2.5	2 2 3	2.6 2.3 3.5	MHz MHz MHz
$R_{DS(ON)}$	Top Switch On-Resistance Bottom Switch On-Resistance				115 70		mΩ mΩ
	$IMON_{OUT}$ Current (Note 6)	I_{SW} = 2.5A I_{SW} = 1.5A I_{SW} = 0.5A		148.5 89.1 29.7	156.25 93.75 31.25	164.0 98.4 33.5	µA µA µA
	I_{OUT} Limit Regulation Voltage		●	1.15	1.22	1.28	V
	$IMON_{IN}$ Current (Note 6)	I_{SW} = 2.5A, 20% Duty Cycle I_{SW} = 1.5A, 20% Duty Cycle I_{SW} = 0.5A, 20% Duty Cycle		29.7 17.8 5.9	31.25 18.75 6.25	32.8 19.7 6.7	µA µA µA
	I_{IN} Limit Regulation Voltage		●	1.15	1.22	1.28	V
	Internal Temperature Monitor	T_A = 25°C			1.5		V
	Internal Temperature Monitor Slope (Note 7)				200		°C/V
	Temperature Limit Hysteresis				50		mV
	PV_{IN} Overvoltage Lockout Threshold	PV_{IN} Rising PV_{IN} Falling		 20	21.5 20.5		V V
V_{INTVCC}	$INTV_{CC}$ Voltage	3.6V < PV_{IN} = SV_{VIN} < 20V		3.1	3.3	3.5	V
	$INTV_{CC}$ Load Regulation (Note 8)	I_{INTVCC} = 0mA to 20mA			0.6		%
V_{RUN}	RUN Threshold	RUN Rising RUN Falling	● ●	1.19 0.97	1.23 1.0	1.27 1.03	V V
	RUN Leakage Current	PV_{VIN} = SV_{VIN} = 20V			0	±1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 3). PV_{IN} = SV_{IN} = 12V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	PGOOD Good-to-Bad Threshold	FB Rising FB Falling			8 –8	10 –10	% %
	PGOOD Bad-to-Good Threshold	FB Rising FB Falling		–3 3	–5 5		% %
	Power Good Filter Time			20	40		µs
R_{PGOOD}	PGOOD Pull-Down Resistance	10mA Load			20		Ω
	Switch Leakage Current	V_{RUN} = 0V			0.01	1	µA
t_{SS}	Internal Soft-Start Time	V_{FB} from 10% to 90% Full Scale			400	700	µs
$I_{TRACK/SS}$	TRACK/SS Pull-Up Current				1.4		µA
	MODE Threshold Voltage	MODE V_{IH} MODE V_{IL}	● ●	1.0		 0.4	V V
	SYNC Threshold Voltage	SYNC V_{IH}	●	1.4			V
	MODE Input Current	MODE = 0V MODE = $INTV_{CC}$			–1.5 1.5		µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by long term current density limitations.

Note 3: The LTC3626 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3626E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization, and correlation with statistical process controls. The LTC3626I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance, and other environmental factors.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 5: Output voltages above 6V are not optimized for controlled on-time operation. Refer to the Applications Information section for further discussions related to the output voltage range. Verified at test by comparison of measured on-time to V_{ON} voltage.

Note 6: Tested in a proprietary test mode, where I_{SW} flows through the synchronous switch only.

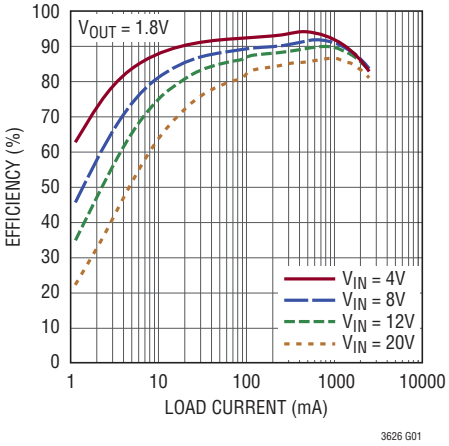
Note 7: Guaranteed by design.

Note 8: Maximum allowed current draw when used as a regulated output is 5mA. This supply is only intended to supply additional DC load currents as needed and not intended to regulate large transient or AC behavior as these waveforms may impact LTC3626 operation.

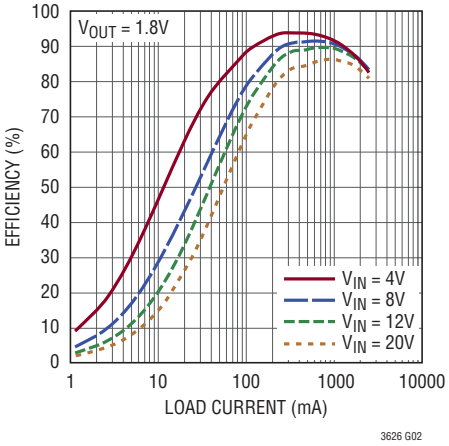
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, PV_{IN} = SV_{IN} = 12V, f = 1MHz unless otherwise noted.

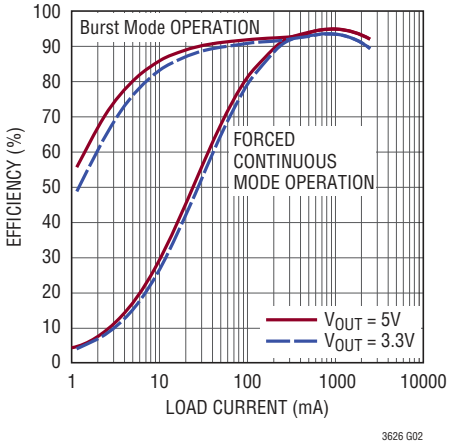
Efficiency vs Load Current (Burst Mode Operation)



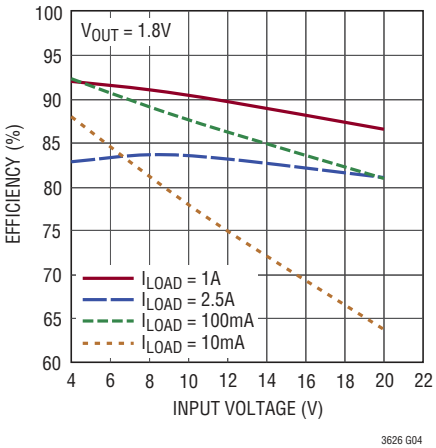
Efficiency vs Load Current (Forced Continuous Mode Operation)



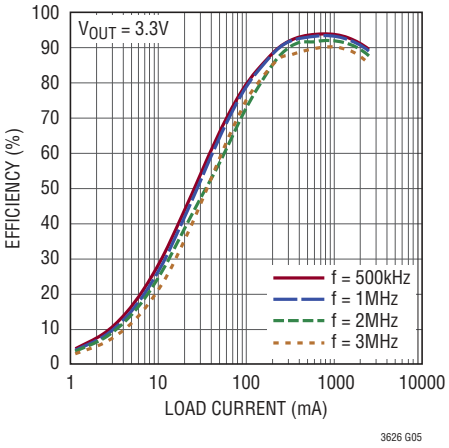
Efficiency vs Load Current (Burst and Forced Continuous)



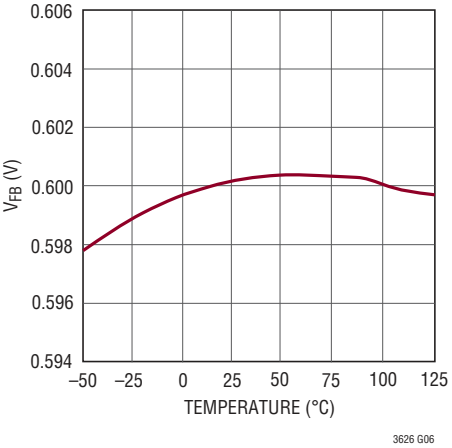
Efficiency vs Input Voltage (Burst Mode Operation)



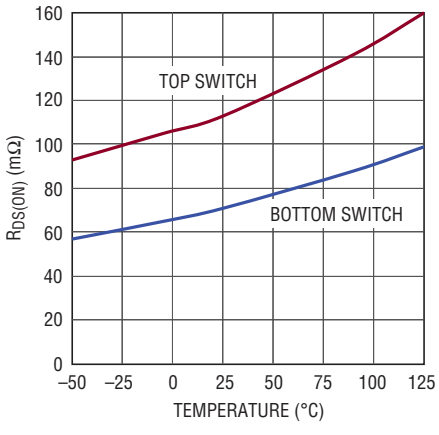
Efficiency vs Frequency (Forced Continuous Mode Operation)



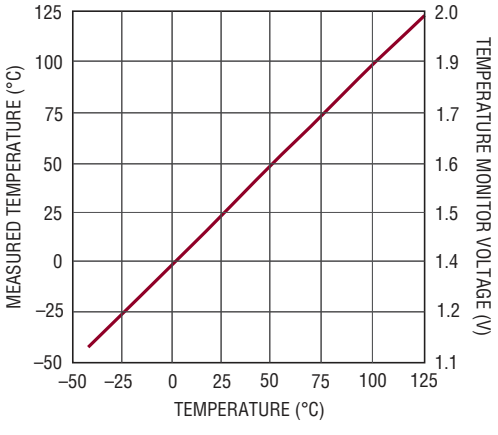
Reference Voltage vs Temperature



Internal MOSFET $R_{DS(ON)}$ vs Temperature



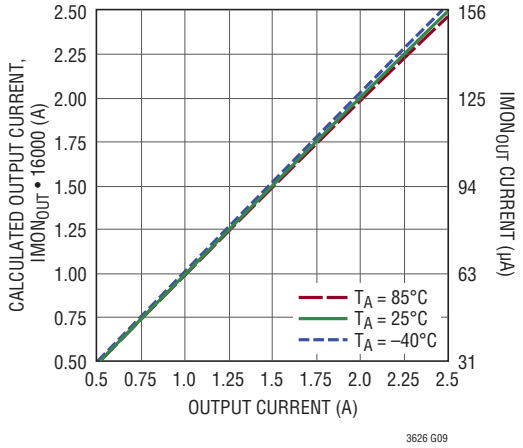
Temperature Monitor vs Temperature



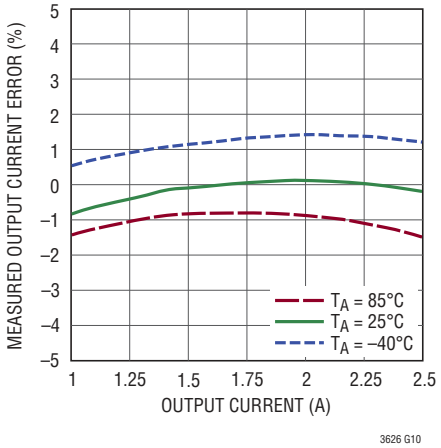
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, PV_{IN} = SV_{IN} = 12V, f = 1MHz unless otherwise noted.

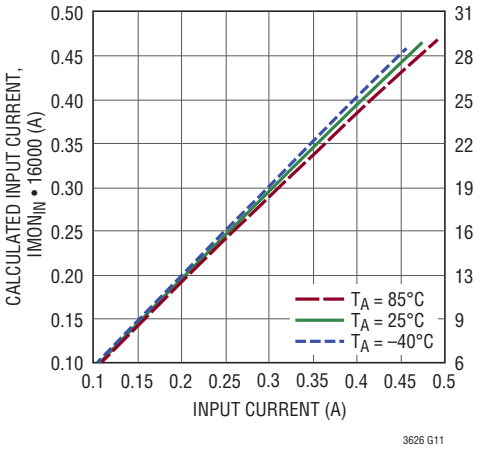
Output Current Monitor vs Output Current



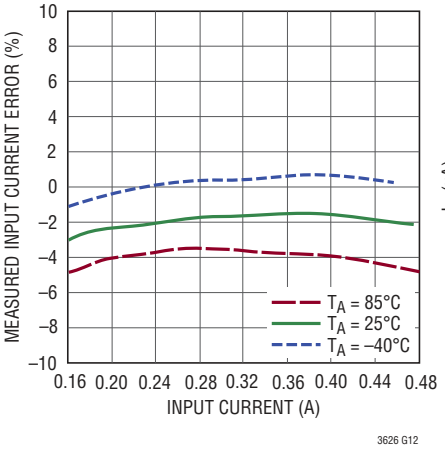
Output Current Monitor Error vs Output Current



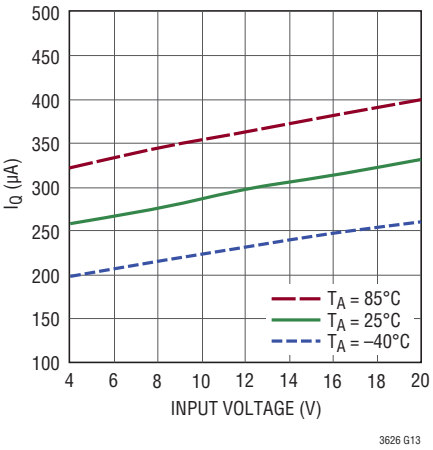
Input Current Monitor vs Input Current



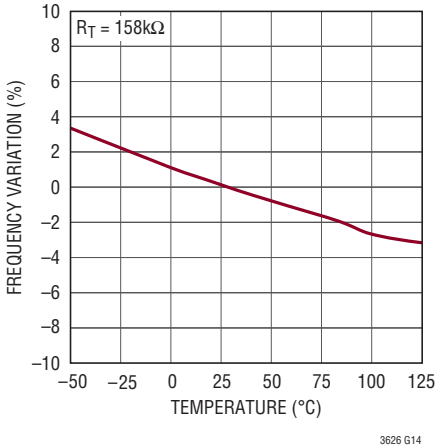
Input Current Monitor Error vs Input Current



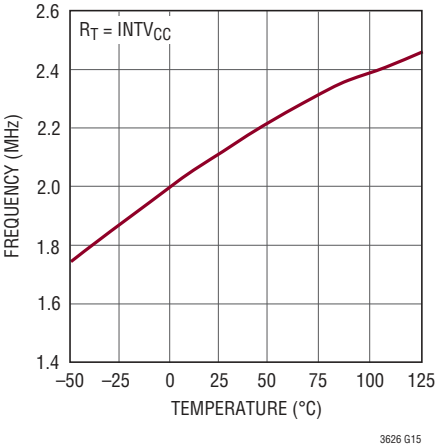
Quiescent Current vs V_{IN} (Burst Mode Operation)



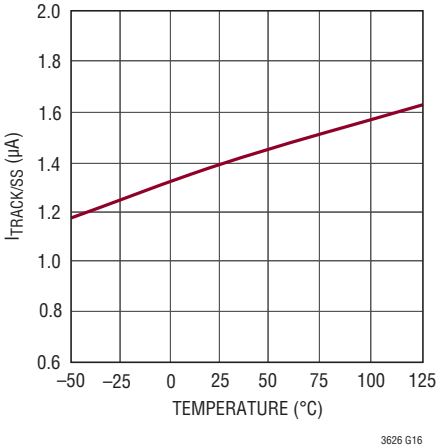
Oscillator Frequency vs Temperature



Oscillator Internal Set Frequency vs Temperature



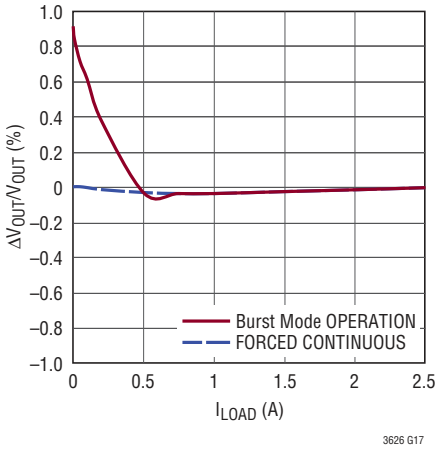
TRACK/SS Pull-Up Current vs Temperature



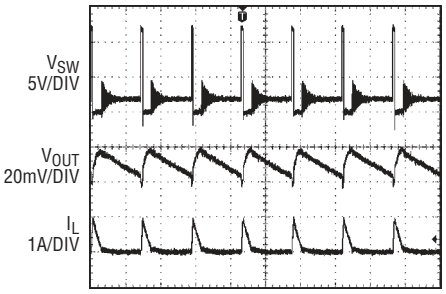
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, PV_{IN} = SV_{IN} = 12V, f = 1MHz unless otherwise noted.

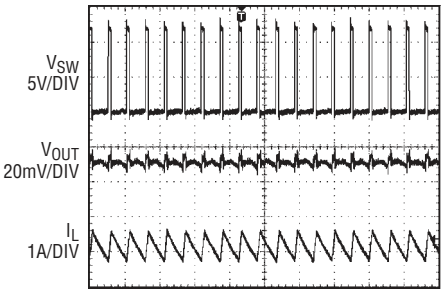
Load Regulation



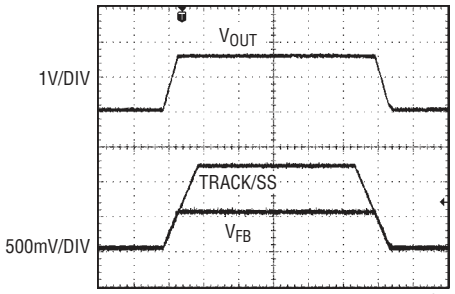
Output Voltage vs Time (Burst Mode Operation)



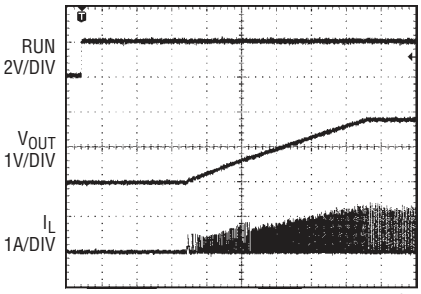
Output Voltage vs Time (Forced Continuous Mode Operation)



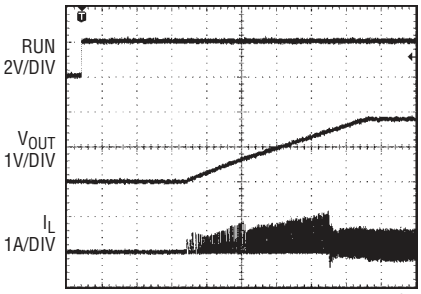
Output Tracking



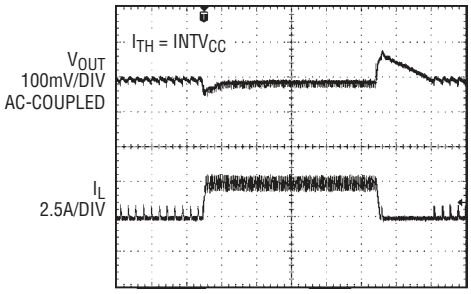
Start-Up from Shutdown (Burst Mode Operation)



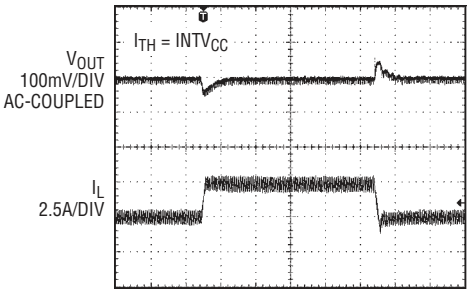
Start-Up from Shutdown (Forced Continuous Mode Operation)



Load Step (Burst Mode Operation)



Load Step (Forced Continuous Mode Operation)



PIN FUNCTIONS

BOOST (Pin 1): Boosted Floating Driver Supply Pin. The (+) terminal of the external bootstrap capacitor connects to this pin while the (–) terminal connects to the SW pin. The normal operation voltage swing of this pin ranges from $INTV_{CC}$ to PV_{IN} + $INTV_{CC}$.

$INTV_{CC}$ (Pin 2): Internal 3.3V Regulator Output Pin. This pin should be decoupled to PGND with a low ESR ceramic capacitor of value 1µF or greater. The 3.3V regulator is disabled when the RUN pin is low.

V_{ON} (Pin 3): On-Time Voltage Input. This pin sets the voltage trip point for the on-time comparator. Tying this pin to the output voltage makes the on-time proportional to V_{OUT} when V_{OUT} < 6V. When V_{OUT} > 6V, the switching frequency may become higher than the set frequency. The impedance of this pin is nominally 160kΩ.

TSET (Pin 4): Temperature Limit Set Pin. The voltage at this pin determines the threshold for internal temperature shutdown. When the voltage at TMON reaches the voltage at TSET, the LTC3626 will trigger an overtemperature fault. An overtemperature fault will initiate part shutdown, reset soft-start and an attempt to restart once the internal temperature falls 10°C (typical) from the threshold given at TSET. The voltage at TSET has no impact on a secondary overtemperature shutdown threshold within the LTC3626 as described in Note 4 of the Electrical Characteristics section.

TMON (Pin 5): Temperature Monitor Output. A voltage proportional to the measured on-die temperature will appear at this pin. The voltage-to-temperature scaling factor is 200°K/V. See the Applications Information section for detailed information on the TMON function. Tie this pin to $INTV_{CC}$ to disable the temperature monitor circuit.

SGND (Pin 6): Signal Ground Pin. This pin should have a low noise connection to reference ground. The feedback resistor network, external compensation network, current monitor components, and R_T resistor should be connected to this ground.

$IMON_{IN}$ (Pin 7): Average Input Current Monitor. A current proportional to the average input current flows out of this pin. Pull this pin to $INTV_{CC}$ to defeat the input current monitor function. An error amplifier compares the voltage on this pin to 1.2V (typical) and throttles the average current as required based on the external resistor value from this pin to SGND. Selecting the external resistor value allows the user to control the maximum average input current. See the Applications Information section for more details.

$IMON_{OUT}$ (Pin 8): Average Output Current Monitor Pin. A current proportional to the average output current flows out of this pin. Pull this pin to $INTV_{CC}$ to defeat the output current monitor function. An error amplifier compares the voltage on this pin to 1.2V (typical) and throttles the average current as required based on the external resistor value from this pin to SGND. Selecting the external resistor value allows the user to control the maximum average output current. See the Applications Information section for more details.

TRACK/SS (Pin 9): Output Voltage Tracking and Soft-Start Input. Forcing a voltage below 0.6V on this pin overrides the internal reference input to the error amplifier. The LTC3626 will servo the FB pin to the TRACK/SS voltage under this condition. Above 0.6V, the tracking function stops and the internal reference resumes control of the error amplifier. An internal 1.4µA (typical) pull-up current from $INTV_{CC}$ allows a soft-start function to be implemented by connecting an external capacitor between this pin and ground. See the Applications Information section for more details.

FB (Pin 10): Output Voltage Feedback. This pin is the input to the error amplifier that compares the feedback voltage to the internal 0.6V reference voltage. Connect this pin to the appropriate resistor divider network to program the desired output voltage.

PIN FUNCTIONS

ITH (Pin 11): Error Amplifier Output and Switching Regulator Compensation Point. Connect this pin to appropriate external components to compensate the regulator loop frequency response. Connect this pin to $INTV_{CC}$ to use the default internal compensation.

RT (Pin 12): Oscillator Frequency Program Pin. Connect an external resistor, between 640k to 105k, from this pin to SGND to program the LTC3626 switching frequency from 500kHz to 3MHz. When RT is tied to $INTV_{CC}$, the switching frequency will default to 2MHz (typical).

RUN (Pin 13): Regulator Enable Pin. Enables chip operation by applying a voltage above 1.25V. A voltage below 1.0V on this pin places the part into shutdown. Do not float this pin.

SV_{IN} (Pin 14): Signal Power Supply Input. This pin supplies current to the internal 3.3V regulator.

PV_{IN} (Pins 15, 16): Main Power Supply Input. These pins should be closely decoupled to PGND with a low ESR capacitor of value 10µF or more.

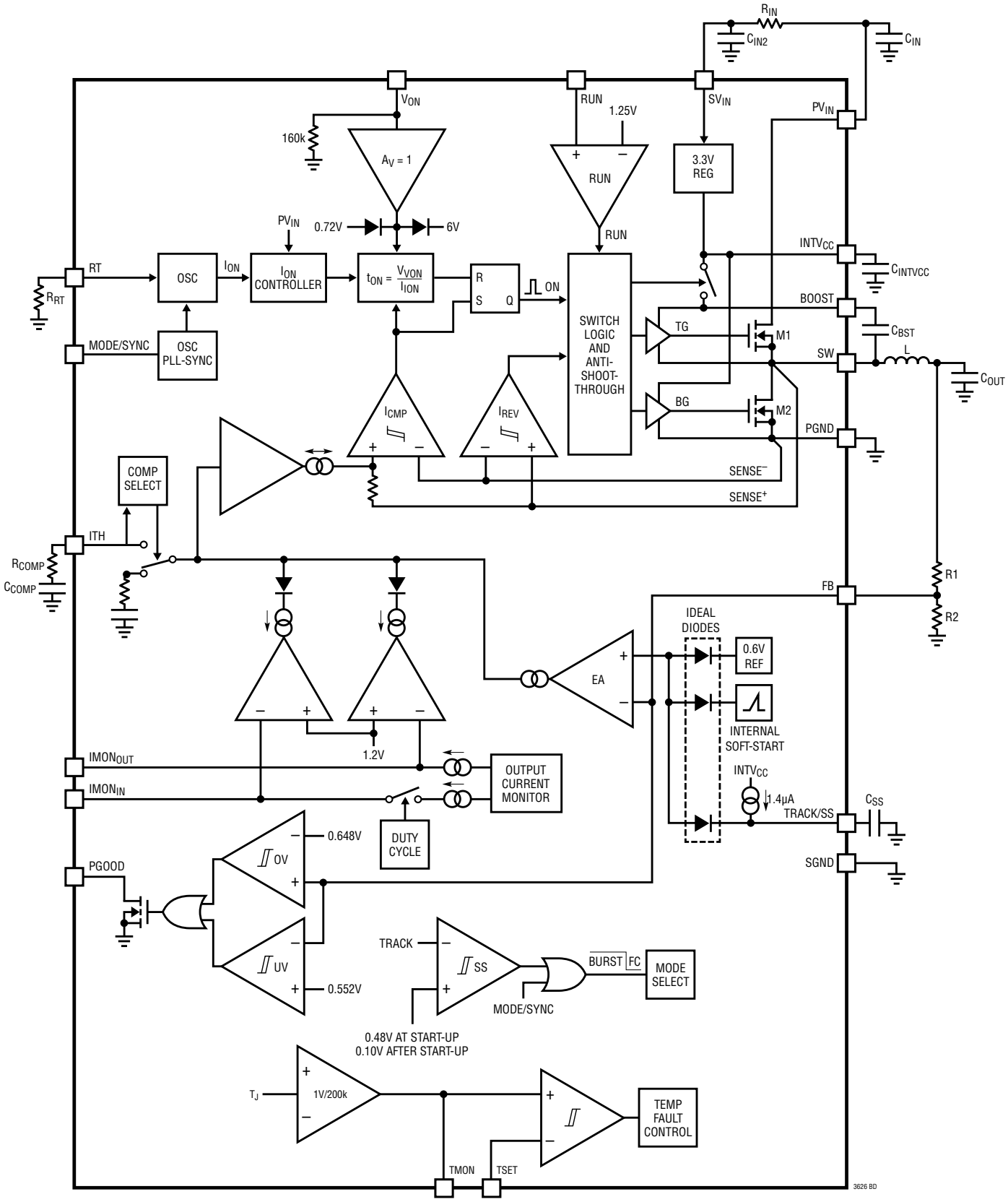
MODE/SYNC (Pin 17): Mode Selection and External Synchronization Input. This pin places the LTC3626 into forced continuous operation when tied to ground. High efficiency Burst Mode operation is enabled by either floating this pin or tying this pin to $INTV_{CC}$. When driven with an external clock, an internal phase-locked loop will synchronize the phase and frequency of the internal oscillator to that of incoming clock signal. During external clock synchronization, the LTC3626 will default to forced continuous operation.

PGOOD (Pin 18): Open-Drain Power Good Output Pin. PGOOD is pulled to ground when the voltage at the FB pin is not within ±8% (typical) of the internal 0.6V reference. PGOOD becomes high impedance once the voltage at the FB pin returns to within ±5% (typical) of the internal reference.

SW (Pins 19, 20): Switch Node Connection to Inductor. Connect this pin to the SW side of the external inductor. The normal operation voltage swing of this pin ranges from ground to PV_{IN}.

PGND (Exposed Pad Pin 21): Power Ground Pin. The (–) terminal of the input bypass capacitor, C_{IN}, and the (–) of the output capacitor, C_{OUT}, should be tied to this pin with a low impedance connection. This pin must be soldered to the PCB to provide low impedance electrical contact to ground and good thermal contact to the PCB.

FUNCTIONAL DIAGRAM



OPERATION

The LTC3626 is a current mode, monolithic, step-down regulator capable of providing up to 2.5A of output current from an input supply as high as 20V. Its unique controlled on-time architecture allows extremely low step-down ratios while maintaining a constant switching frequency. The part is enabled by raising the RUN pin above 1.25V (typical).

Main Control Loop

In normal operation the internal top power MOSFET is turned on for a fixed interval determined by an internal one-shot timer ("ON" signal in the Functional Diagram). When the top power MOSFET turns off, the bottom power MOSFET turns on until the current comparator, I_{CMP}, trips, thus restarting the one-shot timer and initiating the next cycle. The inductor current is monitored by sensing the voltage drop across the bottom power MOSFET. The voltage at the ITH node sets the I_{CMP} comparator threshold corresponding to the inductor valley current. The error amplifier, EA, adjusts the ITH voltage by comparing an internal 0.6V reference voltage to the feedback signal, V_{FB}, derived from the output voltage. If, for example, the load current increases, the output voltage will decrease relative to the 0.6V reference. The ITH voltage then rises until the average inductor current matches that of the load current.

At light load currents the inductor current can drop to zero or become negative. If the LTC3626 is configured for Burst Mode operation, this inductor current condition is detected by the current reversal comparator, I_{REV}, which in turn shuts off the bottom power MOSFET and places the part into a low quiescent current sleep state resulting in discontinuous operation and increased efficiency at low load currents. Both power MOSFETs remain off with the part in sleep and the output capacitor supplying the load current until the ITH voltage rises sufficiently to initiate another cycle. Discontinuous operation is disabled by tying the MODE/SYNC pin to ground, placing the LTC3626 into forced continuous mode. In forced continuous mode, continuous synchronous operation occurs regardless of the output load current.

The operating frequency is determined by the value of the R_T resistor, which programs the current for the internal oscillator. An internal phase-locked loop adjusts the switching regulator on-time to track the internal oscillator edge and force a constant switching frequency, subject to t_{ON} and t_{OFF} time constraints as shown in the Electrical Characteristics table. Alternatively, the RT pin can be connected to the $INTV_{CC}$ pin which causes the internal oscillator to run at the default frequency of 2MHz. Finally, a clock signal can be applied to the MODE/SYNC pin to synchronize the switching frequency to an external source. The regulator defaults to forced continuous operation when an external clock signal is applied.

Output/Input Current Monitor and Limit

The LTC3626 provides a scaled replica of the average output current and a scaled replica of the average input current at the $IMON_{OUT}$ and $IMON_{IN}$ pins respectively. The average current at each of these pins will be 1/16,000th of the measured average current. Further, the voltage at each pin is continuously fed to independent current limit amplifiers that have a voltage reference at 1.2V. Thus, a programmable average current limit for the output current and/or input current may be obtained by placing a resistor of suitable value at the pin of interest so as to produce 1.2V at the desired current limit. When the current limit feature is used, a compensation capacitor (1µF typical) should be placed in parallel with the chosen resistor. The output or input current monitor and limit circuits may be individually disabled by pulling $IMON_{OUT}$ or $IMON_{IN}$ to $INTV_{CC}$ as appropriate.

OPERATION

Temperature Monitor and Limit

The LTC3626 produces a voltage at the TMON pin proportional to the measured on-die temperature. The on-die temperature-to-voltage scaling factor is 200°K/V. Thus, to obtain the on-die temperature in degrees Kelvin, simply multiply the voltage provided at the TMON pin by the scaling factor. To obtain the on-die temperature in degrees Celsius, subtract 273 from the value obtained in degrees Kelvin.

The voltage produced at TMON is continuously fed to a limit comparator that has the voltage at the TSET pin as its reference input. When triggered, this comparator generates an overtemperature fault that will initiate part shutdown and reset of soft-start. Thus, a maximum junction temperature limit may be set by providing a voltage at the TSET pin that corresponds to the temperature limit of interest. The voltage at the TSET pin may be derived from a resistor divider from $INTV_{CC}$, subject to the current constraints listed in the Electrical Characteristics section, or may be driven externally. The LTC3626 will clear the overtemperature fault and restart once the internal temperature falls 10°C (typical) from the threshold given at TSET. The voltage at the TSET pin has no impact on the secondary overtemperature shutdown threshold within the LTC3626 as described in Note 4 of the Electrical Characteristics.

"Power Good" Status Output

The PGOOD open-drain output will be pulled low if the regulator output exits a ±8% window around the regulation point. This condition is released once regulation within a ±5% window is achieved. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTC3626 PGOOD falling edge includes a filter time of approximately 40µs.

PV_{IN} Overvoltage Protection

To protect the internal power MOSFET devices against transient voltage spikes, the LTC3626 continuously monitors the PV_{IN} pin for an overvoltage condition. When PV_{IN} rises above 21.5V (typical), the regulator suspends operation by shutting off both power MOSFETs and resets soft-start. Once PV_{IN} drops below 20.5V (typical), the regulator restarts normal operation by executing a soft-start.

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A general LTC3626 application circuit is shown on the first page of this data sheet. External component selection is largely driven by the load requirement and begins with the selection of the inductor L. Once the inductor is chosen, the input capacitor, C_{IN}, the output capacitor, C_{OUT}, the internal regulator capacitor, C_{INTVCC}, and the boost capacitor, C_{BST}, can be selected. Next, the feedback resistors are selected to set the desired output voltage. Finally, the remaining optional external components can be selected for functions such as external loop compensation, PGOOD, average output current monitor and limit, average input current monitor and limit, and on-die temperature monitor and limit.

Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency, f, of the LTC3626 is determined by an external resistor that is connected between the RT pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_{RT} = \frac{3.2E11}{f}$$

where R_{RT} is in Ω and f is in Hz.

Connecting the RT pin to $INTV_{CC}$ will assert the internal default frequency f = 2MHz; however, this switching frequency will be more sensitive to process and temperature variations than using a resistor on RT (see Typical Performance Characteristics).

The LTC3626 is not optimized for constant on-time operation when configured to generate output voltages greater than 6V. Though output regulation will be maintained under this condition, it is possible the operating frequency may be higher than the programmed value. As a result, for output voltages greater than 6V, the value of the R_T resistor may need adjustment to obtain the desired operating frequency.

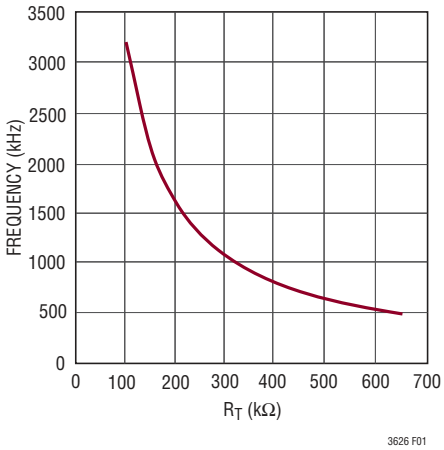

Figure 1. Switching Frequency vs R_T

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the inductor ripple current. More specifically, the inductor ripple current decreases with higher inductor value or higher operating frequency according to the following equation:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where ΔI_L = inductor ripple current, $V_{IN} = PV_{IN}$, f = operating frequency and L = inductor value. A trade-off between component size, efficiency and operating frequency can be seen from this equation. Accepting larger values of ΔI_L allows the use of lower value inductors but results in greater core loss in the inductor, greater ESR loss in the output capacitor, and larger output ripple. Generally, highest efficiency operation is obtained at low operating frequency with small ripple current.

A reasonable starting point for setting the ripple current is approximately $1A_{P-P}$. Note that the largest ripple current occurs at the highest V_{IN}. Further, the inductor ripple current must not be so large that the trough or valley reaches the negative valley current limit of –1A (typical) when operating in forced continuous mode. If the inductor current trough reaches the negative current limit while in forced continuous mode operation, V_{OUT} may exceed the

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target regulation voltage. To guarantee the ripple current does not exceed a specified maximum the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Once the value for L is known, the type of inductor must be selected. Actual core loss is independent of core size for a fixed inductor value but is very dependent on the inductance selected. As the inductance increases, core loss decreases. Unfortunately, increased inductance requires more turns of wire leading to increased copper loss.

Ferrite designs exhibit very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials saturate "hard," meaning the inductance collapses abruptly when the peak design current is exceeded. This collapse will result in an abrupt increase in inductor ripple current, so it is important to ensure the core will not saturate.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroidal or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy but generally cost more than powdered iron core inductors with similar characteristics. The choice of which style inductor to use mainly depends on the price versus size requirements and any radiated field/EMI requirements. New designs for surface mount inductors are available from Toko, Vishay, NEC/Tokin, Cooper, Coilcraft, TDK and Würth Elektronik. Table 1 gives a sampling of available surface mount inductors.

C_{IN} and C_{OUT} Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal wave current at the drain of the top power MOSFET. To prevent large voltage transients from occurring, a low ESR input capacitor sized for the maximum RMS current is recommended. The maximum RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}}$$

Table 1. Inductor Selection Table

INDUCTANCE	DCR	MAX CURRENT	DIMENSIONS	HEIGHT
Vishay IHLP-2525CZ-01 Series				
0.33µH	3.5mΩ	20A	6.5mm × 7mm	3mm
0.47µH	4.0mΩ	17.5A		
0.68µH	5.0mΩ	15.5A		
0.82µH	6.7mΩ	13A		
1.0µH	9.0mΩ	11A		
1.5µH	14mΩ	9A		
2.2µH	18mΩ	8A		
3.3µH	28mΩ	6A		
4.7µH	37mΩ	5.5A		
6.8µH	54mΩ	4.5A		
Toko FDV0620 Series				
0.47µH	8.3mΩ	9A	7mm × 7.7mm	2.0mm
1µH	18.3mΩ	5.7A		
NEC/Tokin MLC0730L Series				
0.47µH	4.5mΩ	16.6A	6.9mm × 7.7mm	3.0mm
0.75µH	7.5mΩ	12.2A		
1µH	9mΩ	10.6A		
Cooper HCP0703 Series				
0.47µH	4.2mΩ	17A	7mm × 7.3mm	3.0mm
0.68µH	5.5mΩ	15A		
0.82µH	8mΩ	13A		
1µH	10mΩ	11A		
1.5µH	14mΩ	9A		
TDK RLF7030 Series				
1µH	8.8mΩ	6.4A	6.9mm × 7.3mm	3.2mm
1.5µH	9.6mΩ	6.1A		
2.2µH	12mΩ	5.4A		
Würth Elektronik WE-HC 744312 Series				
0.47µH	3.4mΩ	16A	7mm × 7.7mm	3.8mm
0.72µH	7.5mΩ	12A		
1µH	9.5mΩ	11A		
1.5µH	10.5mΩ	9A		

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} \cong I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that ripple current ratings

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from capacitor manufacturers are often based on only 2000 hours of life which makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required.

Several capacitors may also be paralleled to meet size or height requirements in the design. For low input voltage applications, sufficient bulk input capacitance is needed to minimize transient effects during output load changes. Even though the LTC3626 design includes an overvoltage protection circuit, care must always be taken to ensure input voltage transients do not pose an overvoltage hazard to the part.

Additional input voltage filtering to the SV_{IN} pin (signal V_{IN}) is made possible by adding optional components R_{IN} and C_{IN2} as shown in the Functional Diagram. Generally, the inherent supply rejection of the LTC3626 makes the addition of these components unnecessary, however, users with large, asynchronous noise on the input supply may choose to populate these components. Typical values for R_{IN} and C_{IN2} are 5Ω and 0.33µF respectively.

The selection of C_{OUT} is determined by the effective series resistance (ESR) that is required to minimize voltage ripple and load step transients as well as the amount of bulk capacitance that is necessary to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response. The output ripple, ΔV_{OUT}, is approximated by:

$$\Delta V_{OUT} < \Delta I_L \left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}} \right)$$

When using low ESR ceramic capacitors, it is more useful to choose the output capacitor value to fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, V_{DROOP}, is usually about 3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx \frac{3 \bullet \Delta I_{OUT}}{f \bullet V_{DROOP}}$$

Though this equation provides a good approximation, more capacitance may be required depending on the duty cycle and load step requirements. The actual V_{DROOP} should be verified by applying a load step to the output.

Using Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now available in small case sizes. Their high voltage rating and low ESR make them ideal for switching regulator applications. However, due to the self-resonant and high-Q characteristics of some types of ceramic capacitors, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input, and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the V_{IN} input. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part. For a more detailed discussion, refer to Application Note 88.

When choosing the input and output ceramic capacitors choose the X5R or X7R dielectric formulations. These dielectrics provide the best temperature and voltage characteristics for a given value and size.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces a 3.3V supply voltage used to power much of the internal LTC3626 circuitry including the power MOSFET gate drivers. The $INTV_{CC}$ pin connects to the output of this regulator and should have a minimum 1µF of decoupling capacitance to ground. The decoupling capacitor should have low impedance electrical connections to the $INTV_{CC}$ and PGND pins to provide the transient currents required by the LTC3626. The user may connect a maximum load current of 5mA to this pin but must take into account the increased power dissipation and die temperature that

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results. Furthermore, this supply is intended only to supply additional DC load currents as desired and not intended to regulate large transient or AC behavior as this may impact LTC3626 operation.

Boost Capacitor

The boost capacitor, C_{BST}, on the Functional Diagram is used to create a voltage rail above the applied input voltage, V_{IN}. Specifically, the boost capacitor is charged to a voltage equal to approximately $INTV_{CC}$ each time the bottom power MOSFET is turned on. The charge on this capacitor is then used to supply the required transient current during the remainder of the switching cycle. When the top MOSFET is turned on, the BOOST pin voltage will be equal to approximately V_{IN} + 3.3V. For most applications a 0.1µF ceramic capacitor will provide adequate performance.

Output Voltage Programming

The LTC3626 will adjust the output voltage such that V_{FB} equals the reference voltage of 0.6V according to:

$$V_{OUT} = 0.6V\left(1+\frac{R1}{R2}\right)$$

The desired output voltage is set by the appropriate selection of resistors R1 and R2 as shown in Figure 2. Choosing large values for R1 and R2 will result in improved efficiency but may lead to undesired noise coupling or phase margin reduction due to stray capacitance at the FB node. Care should be taken to route the FB line away from any noise source, such as the SW or BOOST lines.

To improve the frequency response of the main control loop a feedforward capacitor, C_F, may be used as shown in Figure 2.

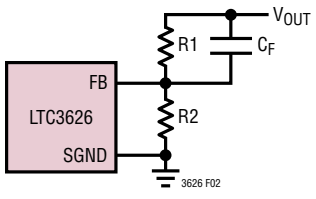

Figure 2. Optional Feedforward Capacitor

Minimum Off-Time/On-Time Considerations

The minimum off-time is the smallest amount of time that the LTC3626 requires to turn on the bottom power MOSFET, trip the current comparator and turn off the power MOSFET. This time is typically 40ns. For the controlled on-time current mode control architecture, the minimum off-time limit imposes a maximum duty cycle of:

$$DC_{MAX} = 1 - (f \bullet t_{OFF(MIN)})$$

where f is the switching frequency and $t_{OFF(MIN)}$ is the minimum off-time. If the maximum duty cycle is surpassed, due to a dropping input voltage for example, the output will drop out of regulation. The minimum input voltage to avoid this dropout condition is:

$$V_{IN(MIN)} = \frac{V_{OUT}}{1-\left(f \bullet t_{OFF(MIN)}\right)}$$

Users should consider reducing the LTC3626 operating frequency for applications that may violate the minimum off-time if constant regulation is required.

Conversely, the minimum on-time is the smallest duration of time in which the top power MOSFET can be in its "on" state. This time is typically 20ns. In continuous mode operation, the minimum on-time limit imposes a minimum duty cycle of:

$$DC_{MIN} = (f \bullet t_{ON(MIN)})$$

where $t_{ON(MIN)}$ is the minimum on-time. As the equation shows, reducing the operating frequency will alleviate the minimum duty cycle constraint.

In rare cases in which the LTC3626's minimum duty cycle is surpassed, the output voltage will still remain in regulation, however the switching frequency will be lower than its programmed value. This is an acceptable result in many applications, so high switching frequencies may be used in the design without fear of severe consequences. As the sections on Inductor and Capacitor Selection show, high switching frequencies allow the use of smaller board components, thus reducing the footprint of the application circuit.

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Internal/External Loop Compensation

The LTC3626 provides the option to use a fixed internal loop compensation network to reduce both the required external component count and design time. The internal loop compensation network can be selected by connecting the ITH pin to the $INTV_{CC}$ pin. To ensure stability, it is recommended that the internal compensation be used at operating frequencies of 1MHz or greater. When using internal compensation, a reasonable starting point for the minimum amount of output capacitance necessary for stability can be found as the greater of either 22µF or C_{OUT} defined by the equation:

$$C_{OUT} > \frac{70e\text{-}6}{V_{OUT}}$$

Alternatively, the user may choose specific external loop compensation components to optimize the main control loop transient response as desired. External loop compensation is chosen by simply connecting the desired network to the ITH pin.

Suggested compensation component values are shown in Figure 3. For a 2MHz application, an R-C (R_{COMP} and C_{COMP} in Figure 3) network of 220pF and 13kΩ provides a good starting point. The bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. A 10pF bypass capacitor (C_{BYP} in Figure 3) the ITH pin is recommended to filter out high frequency coupling from stray board capacitance. In addition, a feedforward capacitor, C_F, can be added to improve the high frequency response, as previously shown in Figure 2. Capacitor C_F provides phase lead by creating a high frequency zero with R1 which improves the phase margin.

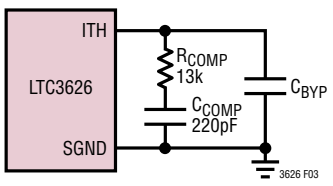

Figure 3. Compensation Components

Checking Transient Response

The regulator loop response can be checked by observing the response of the system to a load step. When configured for external compensation, the availability of the ITH pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time, and settling behavior at this test point reflect the system's closed-loop response. Assuming a predominantly second order system, the phase margin and/or damping factor can be estimated by observing the percentage of overshoot seen at this pin with a high impedance, low capacitance probe.

The ITH external components shown in Figure 3 will provide an adequate starting point for most applications. The series R-C filter sets the pole-zero loop compensation. The values can be modified slightly, from approximately 0.5 to 2 times their suggested values, to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The specific output capacitors must be selected because their various types and values determine the loop feedback factor, gain, and phase. An output current pulse of 20% to 100% of full load current, with a rise time of 1µs to 10µs, will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

When observing the response of V_{OUT} to a load step, the initial output voltage step may not be within the bandwidth of the feedback loop. As a result, the standard second order overshoot/DC ratio cannot be used to estimate phase margin. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76. As shown in Figure 2 a feed-forward capacitor, C_F, may be added across feedback resistor R1 to improve the high frequency response of the system. Capacitor C_F provides phase lead by creating a high frequency zero with R1.

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In some applications severe transients can be caused by switching in loads with large (>10µF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this output droop if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limit, short-circuit protection and soft-start functions.

Input/Output Current Monitor and Limit

The LTC3626 senses the average current through the synchronous switch during the on state and outputs a scaled replica of this current (which corresponds to the regulator's load current) to the $IMON_{OUT}$ pin. A mirrored version of this signal is modulated with the buck regulator's duty cycle to provide a scaled replica of the buck regulator's input current to the $IMON_{IN}$ pin. The average current at each of the monitor pins is 1/16000th the measured average current. The output current at either pin may be measured directly or converted to a voltage with an external resistor.

The average input and output current monitor circuits both use a chopping technique to achieve high accuracy. As a result, a small periodic ripple may be seen at either of these outputs, the average of which is the measured value of interest. The ripple frequency will be the operating frequency divided by 256. In addition, the average input current is measured by modulating the duty cycle of the average output current leading to an additional ripple at the operating frequency. If required, a capacitor may be placed on either output pin to reduce the magnitude of the ripple.

The voltages at the $IMON_{OUT}$ and $IMON_{IN}$ pins are continuously fed to independent current limit amplifiers that have a voltage reference of 1.2V (typical). A programmable average current limit for either average output current or average input current may be obtained by placing a resistor, R_{LIM}, from the monitor pin to SGND according to the following equation:

$$R_{LIM} = \frac{1.2V \bullet 16000}{I_{LIM}}$$

where I_{LIM} is the programmed current limit.

When active, the current limit amplifiers form a feedback loop that controls the maximum average current produced by the LTC3626. Thus, when using the current limit feature, a compensation capacitor should be placed between SGND and the monitor pin of interest. This capacitor, combined with the R_{LIM} resistor, is intended to create a dominant pole for compensation purposes. For most applications, a capacitor with a minimum value of 1µF will provide adequate loop stability. However, given the wide variation in loop parameters that depend on specific application requirements, loop stability should be confirmed by stepping the load current to a level that triggers the programmed current limit. The resultant transient response should provide a sense of the overall loop stability without breaking the feedback loop. The transient response that results from releasing the current limit should also be checked. If the transient response waveforms exhibit excessive ringing, indicating inadequate loop stability, increase the compensation capacitor value until adequate stability has been achieved.

The simple dominant pole compensation scheme discussed previously is intended to provide loop stability by limiting the bandwidth of the current limit feedback loop. As a result, the average current may momentarily exceed the programmed limit until the current limit feedback loop can respond. More advanced compensation networks may be used to potentially reduce the loop response time but generally require more caution and design expertise. For example, one technique is to add a low value resistor in

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series with the compensation capacitor. The resistor in series with the capacitor creates a zero in the current limit loop transfer function given by:

$$f_Z = \frac{1}{2 \bullet \pi \bullet R_Z \bullet C}$$

while minimally impacting the frequency of the compensation pole. Given the current limit loop frequency response contains several moderate frequency poles: one at approximately 10kHz (typical) and two at approximately 100kHz (typical), the placement of the zero in frequency can be used to provide additional phase margin, which in turn, may allow a higher loop bandwidth without sacrificing loop stability. For example, choosing C = 0.33µF and R_Z = 50 creates a zero at approximately 10kHz thereby reducing the impact of the internal pole located at that same frequency. With this compensation scheme, the LTC3626 current limit loop will have a dominant pole frequency, and overall loop bandwidth, roughly three times higher than that provided with a 1µF capacitor, while likely providing adequate loop stability.

As previously described, the LTC3626 senses the average output current through the synchronous FET during the off time. As a result, it is recommended the LTC3626 be operated with an off time of greater than 150ns for best current monitor accuracy. For many applications, this is of little concern unless operating at or near regulator dropout conditions (extremely high duty-cycle operation) and high switching frequencies. Overall, best current monitor accuracy is achieved with output currents above approximately 200mA in forced continuous mode with switching frequencies of 1MHz or lower.

On-Die Temperature Monitor and Limit

The LTC3626 produces a voltage at the TMON pin proportional to the measured junction temperature. The junction temperature-to-voltage scaling factor is 200°K/V. Thus, to obtain the junction temperature in degrees Kelvin, simply multiply the voltage provided at the TMON pin by the scaling factor. To obtain the junction temperature in degrees Celsius, subtract 273 from the value obtained in degrees Kelvin.

The temperature monitor function uses a chopping technique to achieve high precision. As a result, a small periodic ripple may be seen at the TMON pin, the average of which is the measured value of interest. The ripple frequency will be the operating frequency divided by 32. If required, a 1µF or greater capacitor to SGND may be placed on the output to reduce the magnitude of the ripple.

The temperature monitor output is driven from a flexible, internally compensated on-chip buffer capable of sourcing or sinking small amounts of continuous currents (<20µA typical). The buffer internal compensation is intended for capacitive loads up to approximately 150pF (typical). This configuration allows direct connection of TMON to convenient test equipment, such as a multimeter, for temperature measurement. The internal compensation may be overridden by connecting a capacitor of value 1µF or greater between TMON and SGND. This configuration allows for a wide range of applications requiring stability with higher load capacitance, such as some ADC inputs.

The voltage produced at TMON is continuously fed to a limit comparator that has the voltage at the TSET pin as its reference input. When triggered, this comparator generates an overtemperature fault that will initiate part shutdown and reset of soft-start. Thus, a programmable temperature limit may be obtained by providing a voltage at the TSET pin that corresponds to the temperature limit of interest. The voltage at the TSET pin may be derived from a resistor divider from $INTV_{CC}$, subject to the current constraints listed in the Electrical Characteristics section, or may be driven externally. The LTC3626 will clear the overtemperature fault and attempt to restart once the internal temperature falls 10°C (typical) from the threshold given at TSET. As an example, to set a temperature limit at approximately 125°C, the voltage at TSET should be:

$$V_{TSET} = \frac{125°C + 273}{200°K/V} \approx 2V$$

APPLICATIONS INFORMATION

MODE/SYNC Operation

The MODE/SYNC pin is a multipurpose pin allowing both mode selection and operating frequency synchronization. Connecting this pin to $INTV_{CC}$ enables Burst Mode operation for superior efficiency at low load currents at the expense of slightly higher output voltage ripple. When the MODE/SYNC pin is pulled to ground, forced continuous mode operation is selected creating the lowest output voltage ripple at the expense of light load efficiency.

The LTC3626 will detect the presence of an external clock signal on the MODE/SYNC pin and synchronize the internal oscillator to the phase and frequency of the incoming clock. The presence of an external clock will place the LTC3626 into forced continuous mode operation.

Output Voltage Tracking and Soft-Start

The LTC3626 allows the user to control the output voltage ramp rate by means of the TRACK/SS pin. From 0V to 0.6V the TRACK/SS pin will override the internal reference input to the error amplifier forcing regulation of the feedback voltage to that seen at the TRACK/SS pin. When the voltage at the TRACK/SS pin rises above 0.6V, tracking is disabled and the feedback voltage will be regulated to the internal reference voltage.

The voltage at the TRACK/SS pin may be driven from an external source, or alternatively, the user may leverage the internal 1.4µA (typical) pull-up current on TRACK/SS to implement a soft-start function by connecting a capacitor from the TRACK/SS pin to ground. The relationship between output rise time and TRACK/SS capacitance is given by:

$$t_{SS} = 430{,}000 \bullet C_{TRACK/SS}$$

A default internal soft-start timer forces a minimum soft-start time of 400µs (typical) by overriding the TRACK/SS pin input during this time period. Hence, capacitance values less than approximately 1000pF will not significantly affect soft-start behavior.

When using the TRACK/SS pin, the regulator defaults to Burst Mode operation until the output exceeds 80% of its final value (V_{FB} > 0.48V). Once the output reaches this voltage, the operating mode of the regulator switches to the mode selected by the MODE/SYNC pin as described above. During normal operation, if the output drops below 10% of its final value, as it may when tracking down for instance, the regulator will automatically switch to Burst Mode operation to prevent inductor saturation and improve TRACK/SS pin accuracy.

Output Power Good

The PGOOD output of the LTC3626 is driven by a 20Ω (typical) open-drain pull-down device. This pin will become high impedance once the output voltage is within 5% (typical) of the target regulation point allowing the voltage at PGOOD to rise via an external pull-up resistor. If the output voltage exits a 8% (typical) regulation window around the target regulation point, the open-drain output will pull down to ground, thereby dropping the PGOOD pin voltage. A filter time of 40µs (typical) acts to prevent unwanted PGOOD output changes during V_{OUT} transient events. As a result, the output voltage must be within the target regulation window of 5% for 40µs before the PGOOD pin is pulled high. Conversely, the output voltage must exit the 8% regulation window for 40µs before the PGOOD pin pulls to ground (see Figure 4).

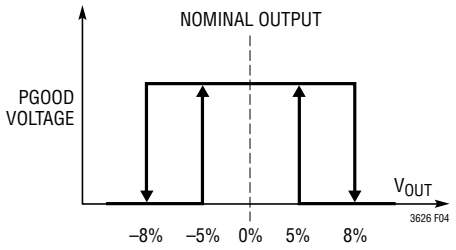


Figure 4. PGOOD Pin Behavior

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\% \text{ Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, etc. are the individual loss terms as a percentage of input power.

APPLICATIONS INFORMATION

Although all dissipative elements in the circuit produce losses, three main sources account for the majority of the losses in the LTC3626: 1) I^2R loss, 2) switching losses and quiescent current loss, 3) transition losses and other system losses.

1. I^2R loss is calculated from the DC resistance of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current will flow through inductor L but is "chopped" between the internal top and bottom power MOSFETs. Thus, the series resistance looking into the SW pin is a function of both the top and bottom MOSFET's $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus to obtain I^2R loss:

   $$\text{"}I^2R \text{ Loss"} = I_{OUT}^2 \bullet (R_{SW} + R_L)$$

2. The internal LDO supplies the power to the $INTV_{CC}$ rail. The total power loss here is the sum of the switching losses and quiescent current losses from the control circuitry.

   Each time a power MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from SV_{IN} to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the DC control bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom power MOSFETs and f is the switching frequency. For estimation purposes, $(Q_T + Q_B)$ on the LTC3626 is approximately 2.5nC. To calculate the total power loss from the LDO load, simply add the gate charge current and quiescent current and multiply by SV_{IN}:

   $$P_{LDO} = (I_{GATECHG} + I_Q) \bullet V_{IN}$$

3. Other "hidden" losses such as transition loss, copper trace resistances, and internal load currents can account for additional efficiency degradations in the overall power system. Transition loss arises from the brief amount of time the top power MOSFET spends in the saturated region during switch node transitions.

Other losses, including diode conduction losses during dead time and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

The LTC3626 requires the exposed package backplane metal (PGND) to be well soldered to the PC board to provide good thermal contact. This gives the QFN package exceptional thermal properties, compared to other packages of similar size, making it difficult in normal operation to exceed the maximum junction temperature of the part. In many applications, the LTC3626 does not generate much heat due to its high efficiency and low thermal resistance package backplane. However, in applications in which the LTC3626 is running at a high ambient temperature, high input voltage, high switching frequency, and maximum output current, the generated heat may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 175°C, both power switches will be turned off until temperature decreases approximately 10°C.

Thermal analysis should always be performed by the user to ensure the LTC3626 does not exceed the maximum junction temperature.

The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

Consider the example in which an LTC3626EUDC is operating with I_{OUT} = 2.5A, $PV_{IN} = SV_{IN}$ = 12V, f = 2MHz, V_{OUT} = 1.8V, and an ambient temperature of 70°C. From the Typical Performance Characteristics section the $R_{DS(ON)}$ of the top switch is found to be nominally 130mΩ while that of the bottom switch is nominally 85mΩ yielding an equivalent power MOSFET resistance R_{SW} of:

$$R_{DS(ON)TOP} \bullet \frac{1.8}{12} + R_{DS(ON)BOT} \bullet \frac{10.2}{12} = 92m\Omega$$

APPLICATIONS INFORMATION

From the previous section, $I_{GATECHG}$ is approximately 5mA when f = 2MHz, and the spec table lists the typical I_Q to be approximately 1mA. Therefore, the total power dissipation due to resistive losses and LDO losses is:

$$P_D = I_{OUT}^2 \bullet R_{SW} + V_{IN} \bullet (I_{GATECHG} + I_Q)$$

$$P_D = (2.5A)^2 \bullet (0.092\Omega) + 12V \bullet 5mA = 635mW$$

The QFN 3mm × 4mm package junction-to-ambient thermal resistance, θ_{JA}, is approximately 47°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

$$T_J = 0.63W \bullet 47°C/W + 70°C = 100°C$$

which is below the maximum junction temperature of 125°C.

Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3626.

1. Does the capacitor C_{IN} connect to PV_{IN} and PGND as close to the pins as possible? These capacitors provide the AC current to the internal power MOSFETs. The (–) plate of C_{IN} should be closely connected to PGND and the (–) plate of C_{OUT}.
2. The output capacitor, C_{OUT}, and inductor L1 should be closely connected to minimize loss. The (–) plate of C_{OUT} should be closely connected to PGND and the (–) plate of C_{IN}.
3. The resistive divider, R1 and R2, must be connected between the (+) plate of C_{OUT} and a ground line terminated near SGND. The feedback signal, V_{FB}, should be routed away from noisy components and traces such as the SW and BOOST lines, and its trace length should be minimized. In addition, RT, compensation components, and current and temperature monitor/limit components should be terminated to SGND.
4. Keep sensitive components away from the SW and BOOST pins. The R_{RT} resistor, the feedback resistors, the compensation components, the current monitor components, and the $INTV_{CC}$ bypass capacitor should all be routed away from the SW trace and the inductor.
5. A ground plane is preferred, but if not available the signal and power grounds should be segregated with both connecting to a common, low noise reference point. The point at which the ground terminals of the V_{IN} and V_{OUT} bypass capacitors are connected makes a good, low noise reference point. The connection to the PGND pin should be made with a minimal resistance trace from the reference point.
6. Flood all unused areas on all layers with copper in order to reduce the temperature rise of power components. These copper areas should be connected to the exposed backside connection of the IC.

Design Example

As a design example, consider using the LTC3626 in an application with the following specifications:

V_{IN} = 12V, V_{OUT} = 1.8V, $I_{OUT(MAX)}$ = 2.5A, $I_{OUT(MIN)}$ = 50mA

Further, the ability to continuously monitor the average output current (I_{OUT}) and the internal temperature is desired. Finally, an average I_{OUT} limit of 2.5A and an internal temperature limit of approximately 125°C are desired.

Because efficiency is important at both high and low load currents, Burst Mode operation and 1MHz operation is chosen.

First, the correct R_{RT} resistor value for 1MHz switching frequency must be chosen. Based on the equation in the Applications Information section, R_{RT} is calculated to be 320k. A standard 324k resistor is selected for R_{RT}.

APPLICATIONS INFORMATION

Next, determine the inductor value for approximately 40% ripple current using:

$$L = \left(\frac{1.8V}{1MHz \bullet 1A}\right)\left(1 - \frac{1.8V}{12V}\right) = 1.53\mu H$$

A standard 1.5µH inductor will work well for this application.

Next, C_{OUT} is selected based on the required output transient performance and the required ESR to satisfy the output voltage ripple. For this design, two 22µF ceramic capacitors will be used.

C_{IN} should be sized for a maximum current rating of:

$$I_{RMS} = 2.5A \bullet \frac{\sqrt{1.8V(12V - 1.8V)}}{12V} = 0.89A$$

Decoupling the PV_{IN} pin with a 47µF ceramic capacitor should be adequate for most applications. An additional 1µF capacitor on the PV_{IN} can be used to help reduce ringing as required. A 0.33µF capacitor on the SV_{IN} pin is optional and will be tied to PV_{IN} through a 5Ω resistor for additional filtering at the SV_{IN} pin. Finally, a 0.1µF boost capacitor should work for most applications.

To save board space, the ITH pin is connected to $INTV_{CC}$ to select the internal compensation network.

The PGOOD pin is connected to V_{IN} through a 100k resistor to $INTV_{CC}$.

To program the I_{OUT} limit at 2.5A, a resistor is connected between $IMON_{OUT}$ and SGND with a desired value equal to:

$$R_{IOUT} = \frac{16{,}000 \bullet 1.2V}{2.5A} = 7.68k\Omega$$

Thus, a standard 7.68kΩ will be selected for R_{IOUT}. A 1µF capacitor placed in parallel with R_{IOUT} for I_{OUT} limit loop compensation should be adequate for most applications.

The 125°C temperature limit is programmed by setting a voltage at the TSET pin equal to:

$$V_{TSET} = \frac{125°C + 273}{200°K/V} \approx 2V$$

In this example, the TSET voltage will be derived by dividing the available $INTV_{CC}$ voltage using R_{TSET1} = 432k and R_{TSET2} = 665k.

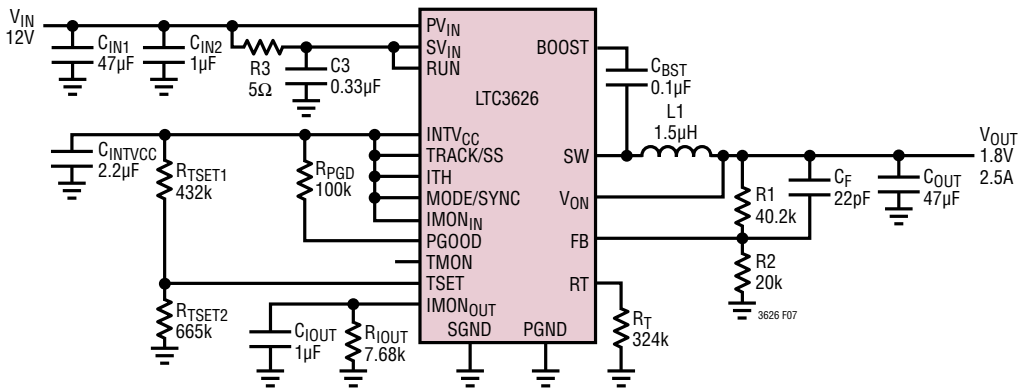
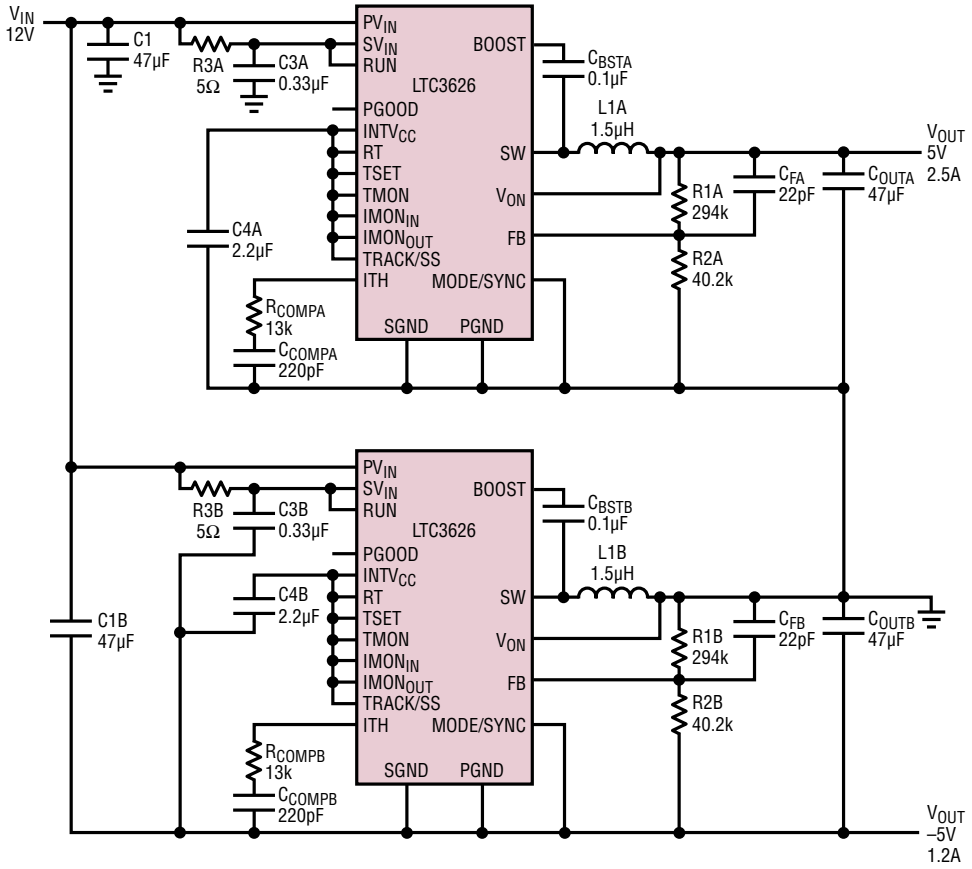


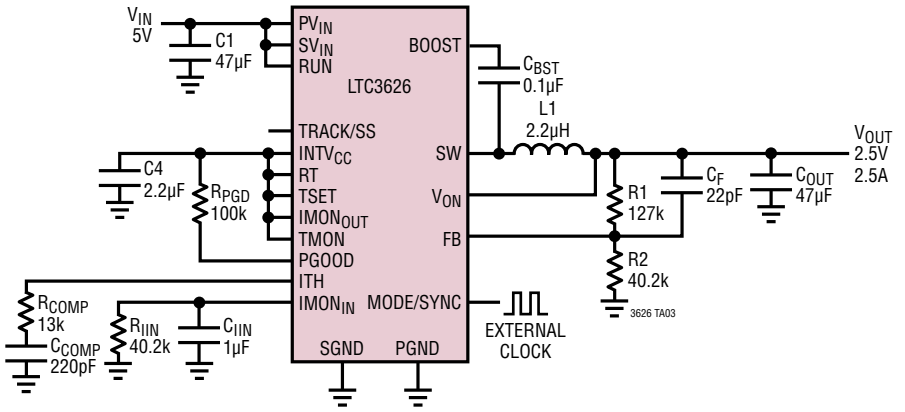
Figure 7. 12V Input to 1.8V Output, 2.5A Regulator at 1MHz in Burst Mode Operation with Output Current Monitor and 2.5A Limit, On-Die Temperature Monitor and 125°C Limit

TYPICAL APPLICATIONS

12V Input to ±5V Output at 2MHz

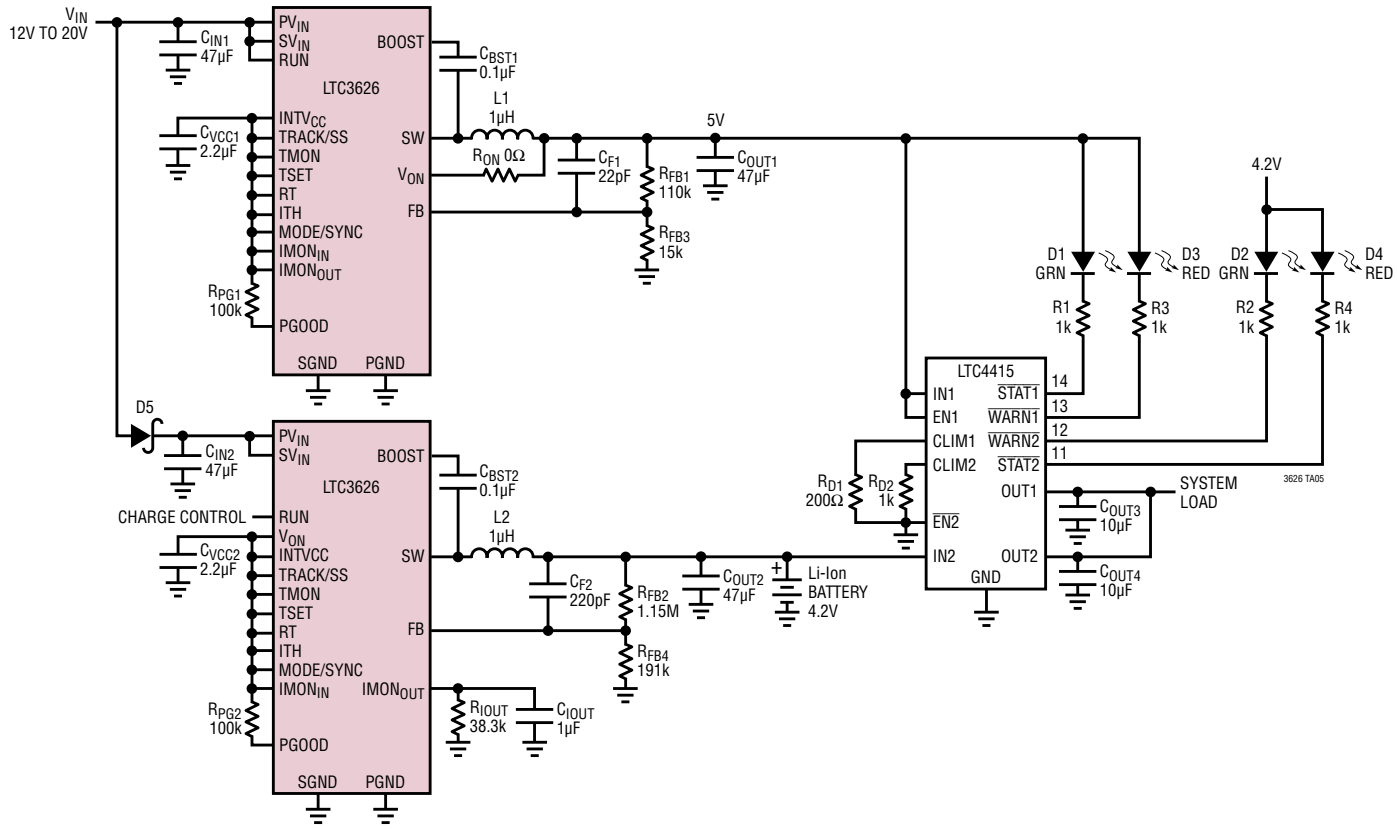


5V Input to 2.5V Output at 1MHz Synchronized Frequency with Input Current Monitor and 475mA Input Current Limit



TYPICAL APPLICATIONS

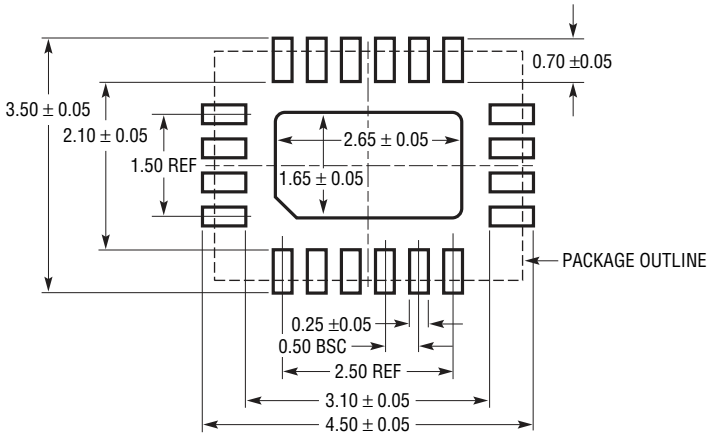
12V Input to 5V Output and 500mA Charger for Battery Backup System



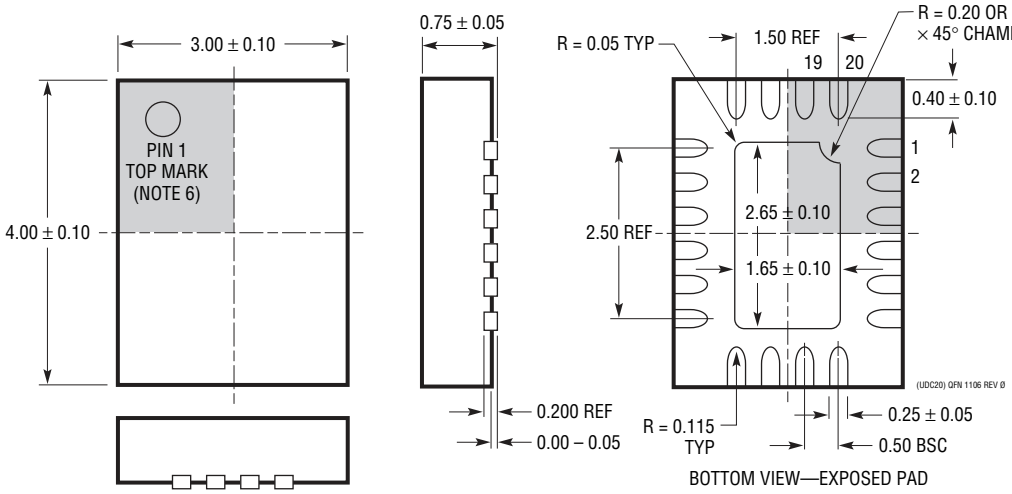
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

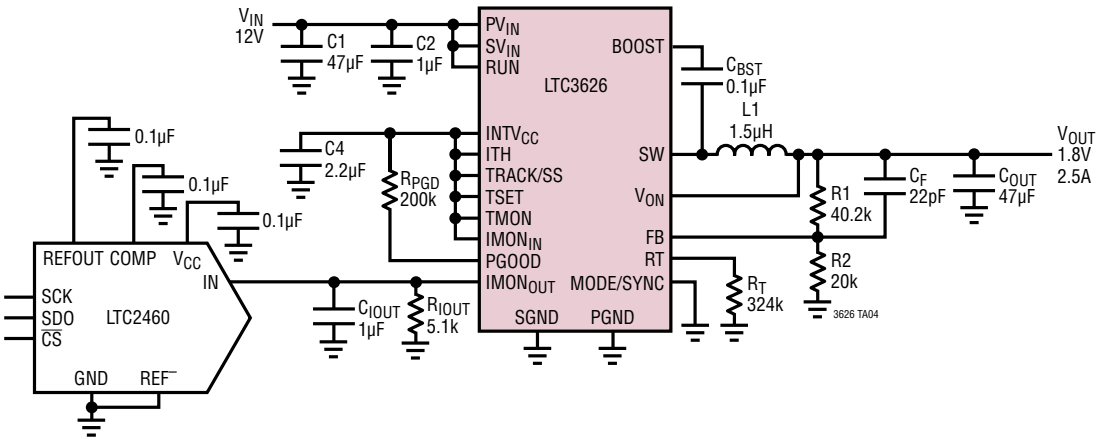
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/15	Clarified Electrical Table	3
		Clarified Inductor Selection Section	13
		Clarified Typical Application Schematics	24, 25

TYPICAL APPLICATION

12V Input to 1.8V Output, 2.5A Regulator with Digital Output Current Monitoring



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3601	15V, 1.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E
LTC3603	15V, 2.5A (I_{OUT}), 3MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4.5V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 75µA, I_{SD} < 1µA, 4mm × 4mm QFN-20, MSOP-16E
LTC3633	15V, Dual 3A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 500µA, I_{SD} < 15µA, 4mm × 5mm QFN-28, MSOP-28E
LTC3605A	20V, 5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 4V to 20V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 2mA, I_{SD} < 15µA, 4mm × 4mm QFN-24
LTC3604	15V, 2.5A (I_{OUT}), 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 3.6V to 15V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 300µA, I_{SD} < 15µA, 3mm × 3mm QFN-16, MSOP-16E

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