LV5122T

CMOS IC

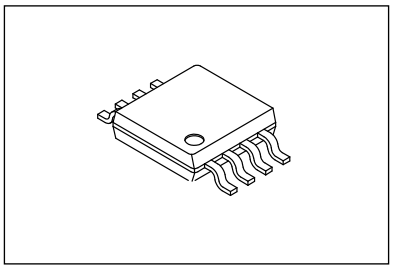
2-Cell Lithium-Ion Secondary Battery Protection IC

ON Semiconductor®

www.onsemi.com

Overview

The LV5122T is a protection IC for 2-cell lithium-ion secondary batteries.



MSOP8 (150mil)

Feature

- Monitoring function for each cell: Detects overcharge and over-discharge conditions and controls the charging and discharging operation of each cell.
- High detection voltage accuracy: Over-charge detection accuracy ±25mV
  Over-discharge detection accuracy ±100mV
- Hysteresis cancel function: The hysteresis of over-discharge detection voltage is canceled by sensing the connection of a load after overcharging has been detected.
- Discharge current monitoring function:
  Detects over-currents and load shorting, and an excessive discharge current is controlled.
- Low current consumption: Normal operation mode typ. 6.0μA
  Stand by mode max. 0.2μA
- 0V cell charging function: Charging is enabled even when the cell voltage is 0V by giving a potential difference between the V_{DD} pin and V^- pin.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter		Symbol	Conditions	Ratings	Unit
Power supply voltage		V_{DD}		-0.3 to +12	V
Input voltage Charger minus voltage		V^-		V_{DD}-28 to V_{DD}+0.3	V
Output voltage	Cout pin voltage	Vcout		V_{DD}-28 to V_{DD}+0.3	V
	Dout pin voltage	Vdout		V_{SS}-0.3 to V_{DD}+0.3	V
Allowable power dissipation		Pd max	Independent IC	170	mW
Operating ambient temperature		Topr		-30 to +80	°C
Storage temperature		Tstg		-40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

Electrical Characteristics 1 at Ta = 25°C, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operation input voltage	Vcell	Between V_{DD} and V_{SS}	1.5		10	V
0V cell charging minimum operation voltage	Vmin	Between V_{DD}-V_{SS} =0 and V_{DD}-V^-			1.5	V
Over-charge detection voltage	Vd1		4.325	4.350	4.375	V
Over-charge reset voltage	Vh1		4.100	4.150	4.200	V
Over-charge detection delay time	td1	V_{DD}-Vc=3.5V→4.5V, Vc-V_{SS}=3.5V	0.5	1.0	1.5	s
Over-charge reset delay time	tr1	V_{DD}-Vc=4.5V→3.5V, Vc-V_{SS}=3.5V	20.0	40.0	60.0	ms
Over-discharge detection voltage	Vd2		2.20	2.30	2.40	V
Over-discharge reset hysteresis voltage	Vh2		10.0	20.0	40.0	mV
Over-discharge detection delay time	td2	V_{DD}-Vc=3.5V→2.2V, Vc-V_{SS}=3.5V	50	100	150	ms
Over-discharge reset delay time	tr2	V_{DD}-Vc=2.2V→3.5V, Vc-V_{SS}=3.5V	0.5	1.0	1.5	ms
Over-current detection voltage	Vd3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.28	0.30	0.32	V
Over-current reset hysteresis voltage	Vh3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	5.0	10.0	20.0	mV
Over-current detection delay time	td3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	2.5	5.0	7.5	ms
Over-current reset delay time	tr3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.5	1.0	1.5	ms
Short circuit detection voltage	Vd4	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	1.0	1.3	1.6	V
Short circuit detection delay time	td4	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.2	0.5	0.8	ms
Standby reset voltage	Vstb	Between V_{DD}-Vc=2.0V, Vc-V_{SS}=2.0V (V^-)-V_{SS}	V_{DD}×0.4	V_{DD}×0.5	V_{DD}×0.6	V
Reset resistance (connected to V_{DD})	R_{DD}		100	200	400	kΩ
Reset resistance (connected to V_{SS})	R_{SS}		0.5	1.0	1.5	MΩ
Cout Nch ON voltage	$V_{OL}1$	I_{OL}=50μA, V_{DD}-Vc=4.4V, Vc-V_{SS}=4.4V			0.5	V
Cout Pch ON voltage	$V_{OH}1$	I_{OL}=50μA, V_{DD}-Vc=3.9V, Vc-V_{SS}=3.9V	V_{DD}-0.5			V
Dout Nch ON voltage	$V_{OL}2$	I_{OL}=50μA, V_{DD}-Vc=Vd2(min), Vc-V_{SS}=Vd2(min)			0.5	V
Dout Pch ON voltage	$V_{OH}2$	I_{OL}=50μA, V_{DD}-Vc=3.9V, Vc-V_{SS}=3.9V	V_{DD}-0.5			V
Vc input current	Ivc	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V		0.0	1.0	μA
Current drain	I_{DD}	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V		6.0	13.0	μA
Standby current	Istb	V_{DD}-Vc=2.2V, Vc-V_{SS}=3.5V			0.2	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Electrical Characteristics 2 at Ta = -20 to 70°C, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operation input voltage	Vcell	Between V_{DD} and V_{SS}	1.65		10	V
0V cell charging minimum operation voltage	Vmin	Between V_{DD}-V_{SS} =0 and V_{DD}-V^-			1.65	V
Over-charge detection voltage	Vd1		4.305	4.350	4.390	V
Over-charge reset voltage	Vh1		4.080	4.150	4.215	V
Over-charge detection delay time	td1	V_{DD}-Vc=3.5V→4.5V, Vc-V_{SS}=3.5V	0.350	1.000	1.950	s
Over-charge reset delay time	tr1	V_{DD}-Vc=4.5V→3.5V, Vc-V_{SS}=3.5V	14.0	40.0	78.0	ms
Over-discharge detection voltage	Vd2		2.18	2.30	2.42	V
Over-discharge reset hysteresis voltage	Vh2		8.0	20.0	42.0	mV
Over-discharge detection delay time	td2	V_{DD}-Vc=3.5V→2.2V, Vc-V_{SS}=3.5V	35	100	195	ms
Over-discharge reset delay time	tr2	V_{DD}-Vc=2.2V→3.5V, Vc-V_{SS}=3.5V	0.35	1.0	1.95	ms
Over-current detection voltage	Vd3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.271	0.300	0.329	V
Over-current reset hysteresis voltage	Vh3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	3.5	10.0	23.0	mV
Over-current detection delay time	td3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	1.75	5.00	9.75	ms
Over-current reset delay time	tr3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.35	1.00	1.95	ms
Short circuit detection voltage	Vd4	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.9	1.3	1.7	V
Short circuit detection delay time	td4	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.14	0.5	1.04	ms
Standby reset voltage	Vstb	Between V_{DD}-Vc=2.0V, Vc-V_{SS}=2.0V (V^-)-V_{SS}	V_{DD}×0.4	V_{DD}×0.5	V_{DD}×0.6	V
Reset resistance (connected to V_{DD})	R_{DD}		70	200	520	kΩ
Reset resistance (connected to V_{SS})	R_{SS}		0.35	1.0	1.95	MΩ
Cout Nch ON voltage	$V_{OL}1$	I_{OL}=50μA, V_{DD}-Vc=4.4V, Vc-V_{SS}=4.4V			0.5	V
Cout Pch ON voltage	$V_{OH}1$	I_{OL}=50μA, V_{DD}-Vc=3.9V, Vc-V_{SS}=3.9V	V_{DD}-0.5			V
Dout Nch ON voltage	$V_{OL}2$	I_{OL}=50μA, V_{DD}-Vc=Vd2(min), Vc-V_{SS}=Vd2(min)			0.5	V
Dout Pch ON voltage	$V_{OH}2$	I_{OL}=50μA, V_{DD}-Vc=3.9V, Vc-V_{SS}=3.9V	V_{DD}-0.5			V
Vc input current	Ivc	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V		0.0	1.0	μA
Current drain	I_{DD}	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V		6.0	16.9	μA
Standby current	Istb	V_{DD}-Vc=2.2V, Vc-V_{SS}=3.5V			0.2	μA

The Ratings of the table above is a design guarantees and are not measured.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Electrical Characteristics 3 at Ta = -30 to 85°C, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operation input voltage	Vcell	Between V_{DD} and V_{SS}	1.73		10	V
0V cell charging minimum operation voltage	Vmin	Between V_{DD}-V_{SS} =0 and V_{DD}-V^-			1.73	V
Over-charge detection voltage	Vd1		4.295	4.350	4.395	V
Over-charge reset voltage	Vh1		4.070	4.150	4.220	V
Over-charge detection delay time	td1	V_{DD}-Vc=3.5V→4.5V, Vc-V_{SS}=3.5V	0.3	1.0	2.1	s
Over-charge reset delay time	tr1	V_{DD}-Vc=4.5V→3.5V, Vc-V_{SS}=3.5V	12.0	40.0	84.0	ms
Over-discharge detection voltage	Vd2		2.17	2.30	2.43	V
Over-discharge reset hysteresis voltage	Vh2		6.0	20.0	42.0	mV
Over-discharge detection delay time	td2	V_{DD}-Vc=3.5V→2.2V, Vc-V_{SS}=3.5V	30	100	210	ms
Over-discharge reset delay time	tr2	V_{DD}-Vc=2.2V→3.5V, Vc-V_{SS}=3.5V	0.3	1.0	2.1	ms
Over-current detection voltage	Vd3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.267	0.300	0.333	V
Over-current reset hysteresis voltage	Vh3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	2.5	10.0	240	mV
Over-current detection delay time	td3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	1.5	5.0	10.5	ms
Over-current reset delay time	tr3	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.3	1.0	2.1	ms
Short circuit detection voltage	Vd4	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.8	1.3	1.8	V
Short circuit detection delay time	td4	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V	0.12	0.5	1.12	ms
Standby reset voltage	Vstb	Between V_{DD}-Vc=2.0V, Vc-V_{SS}=2.0V (V^-)-V_{SS}	V_{DD}×0.4	V_{DD}×0.5	V_{DD}×0.6	V
Reset resistance (connected to V_{DD})	R_{DD}		60	200	560	kΩ
Reset resistance (connected to V_{SS})	R_{SS}		0.3	1.0	2.1	MΩ
Cout Nch ON voltage	$V_{OL}1$	I_{OL}=50μA, V_{DD}-Vc=4.4V, Vc-V_{SS}=4.4V			0.5	V
Cout Pch ON voltage	$V_{OH}1$	I_{OL}=50μA, V_{DD}-Vc=3.9V, Vc-V_{SS}=3.9V	V_{DD}-0.5			V
Dout Nch ON voltage	$V_{OL}2$	I_{OL}=50μA, V_{DD}-Vc=Vd2(min), Vc-V_{SS}=Vd2(min)			0.5	V
Dout Pch ON voltage	$V_{OH}2$	I_{OL}=50μA, V_{DD}-Vc=3.9V, Vc-V_{SS}=3.9V	V_{DD}-0.5			V
Vc input current	Ivc	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V		0.0	1.0	μA
Current drain	I_{DD}	V_{DD}-Vc=3.5V, Vc-V_{SS}=3.5V		6.0	18.2	μA
Standby current	Istb	V_{DD}-Vc=2.2V, Vc-V_{SS}=3.5V			0.2	μA

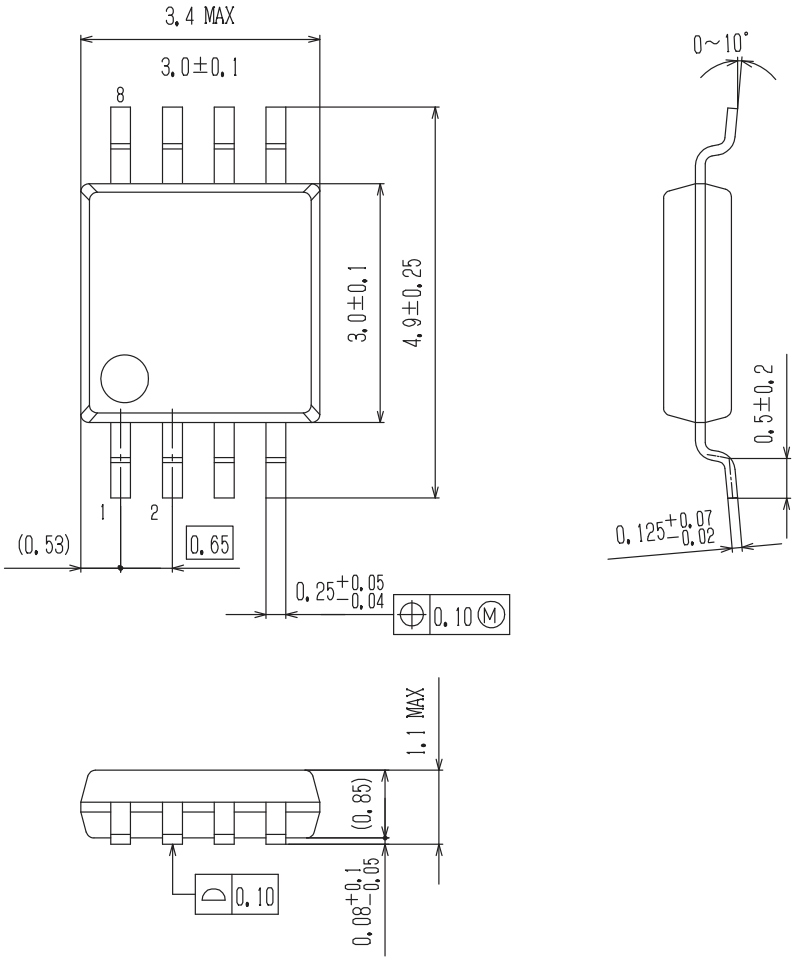
The Ratings of the table above is a design guarantees and are not measured.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

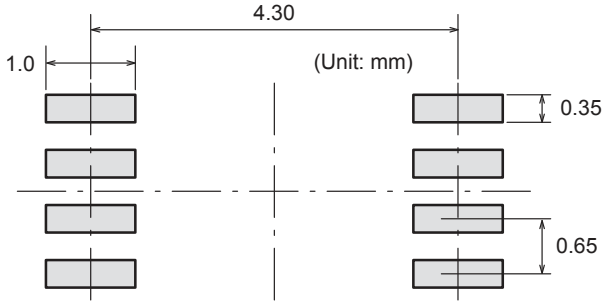
Package Dimensions

unit : mm

Micro8 / MSOP8 (150 mil)
CASE 846AH
ISSUE A



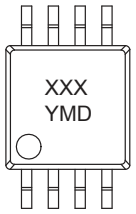
SOLDERING FOOTPRINT*



NOTE: The measurements are not to guarantee but for reference only.

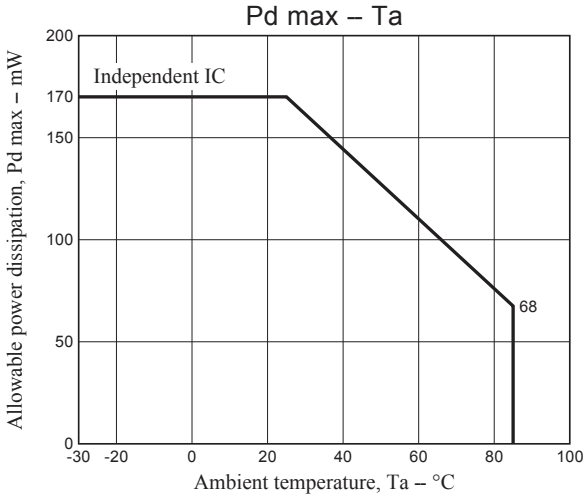
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

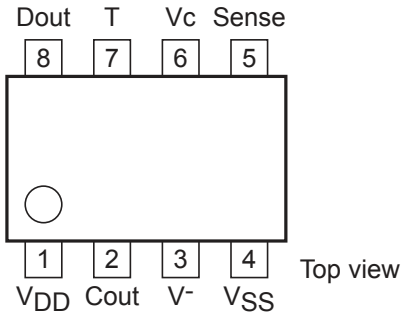


XXX = Specific Device Code
Y = Year
M = Month
D = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.



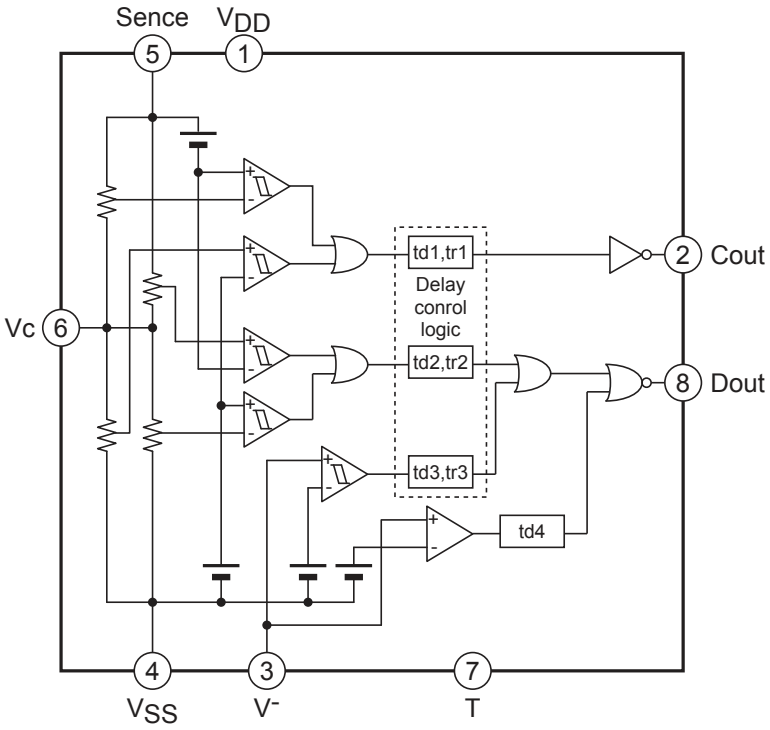
Pin Assignment



Pin Functions

Pin No.	Symbol	Description
1	V_{DD}	V_{DD} pin
2	Cout	Overcharge detection output pin
3	V^-	Charger minus voltage input pin
4	V_{SS}	V_{SS} pin
5	Sense	Sense pin
6	Vc	Intermediate voltage input pin
7	T	Pin to shorten detection time (open under normal condition)
8	Dout	Overdischarge detection output pin

Block Diagram



Functional Description

Over-charge detection

If either of the cell voltage is equal to or more than the over-charge detection voltage, stop further charging by turning "L" the Cout pin and turning off external Nch MOS FET after the over-charge detection delay time. This delay time is set by the internal counter.

The over-charge detection comparator has the hysteresis function. Note that this hysteresis can be cancelled by connecting the load after detection of over-charge detection.

Once over-charge detection is made, over-current detection is not made to prevent malfunction. Note that short-circuit can be detected.

Over-charge return

If charger is connected and both cell voltages become equal to or lower than the over-charge recovery voltage or over-charge detection voltage when load is connected, the Cout pin returns to "H" after the over-charge recovery delay time set by the internal counter.

When load is connected and either cell or both cell voltages are equal to or more than the over-charge detection voltage, the Cout pin does not return to "H." When the load current is passed through the external Cout pin parasite diode of Nch MOS FET after the over-charge recovery delay time and each cell voltage becomes equal to or below over-charge detection voltage, the Cout returns to "H."

Over-discharge detection

When either cell voltage is equal to or below over-discharge voltage, stop further discharge by turning "L" the Dout pin and turning off external Nch MOS FET after the over-charge detection delay time.

The IC becomes standby state after detecting over-discharge and its consumption current is kept at about 0A. After detection, the V^- pin will be connected to V_{DD} pin via 200kΩ.

Over-discharge return

Return from over-discharge is made by connecting charger. If the V^- pin voltage becomes equal to or lower than the standby return voltage by connecting charger after detecting over-discharge, it returns from the standby state to start cell voltage monitoring. If both voltages become equal to or more than the over-discharge detection voltage by charging, the Dout pin returns to "H" after the over-discharge return.

Over-current detection

When high current is passed through the battery, the V potential rises by the ON resister of external MOS FET and becomes equal to or more than the over-current detection voltage, that will be deemed over-current state. Turn "L" the Dout pin after the over-current detection delay time and turn off the external Nch MOS FET to prevent high current in the circuit. The delay time is set by the internal counter. After detection, the V^- pin will be connected to V_{SS} via 1MΩ. It will not go into standby state after detecting over-current.

Short circuit detection

If greater discharge current is passed and the V^- pin voltage becomes equal to or more than the short-circuit detection voltage, it will go into short-circuit detection state after the short circuit delay time shorter than the over-current detection delay time. When short-circuit is detected, just like the time of over-current detection, turn Dout pin "L" and turn off external Nch MOS FET to prevent high current in the circuit. The V^- pin will be connected to V_{SS} after detection via 30kΩ. It will not go into standby state after detecting short-circuit.

Over-current/short-detection return

After detecting over-current or short circuit, the return resistor (typ.1MΩ) between V^- pin and V_{SS} pin becomes effective and if the resistor is opened the V^- pin voltage will be pulled by the V_{SS} pin voltage. Thereafter, the IC will return from the over-current/short-circuit detection state when the V^- pin voltage becomes equal to or below the over-current detection voltage and the Dout pin returns to "H" after over-current return delay time set by the internal counter.

0V cell charge

If the cell voltage is 0V but a potential difference between V_{DD} and V becomes equal to or greater than the 0V cell charging lowest operation voltage, the Cout pin will output "H" and enable charging.

Test time reduction function

By turning T pin to the V_{DD} potential, the delay times set by the counter can be cut. Normal time settings if T pin is open. Delay time not set by the counter cannot be controlled by this pin.

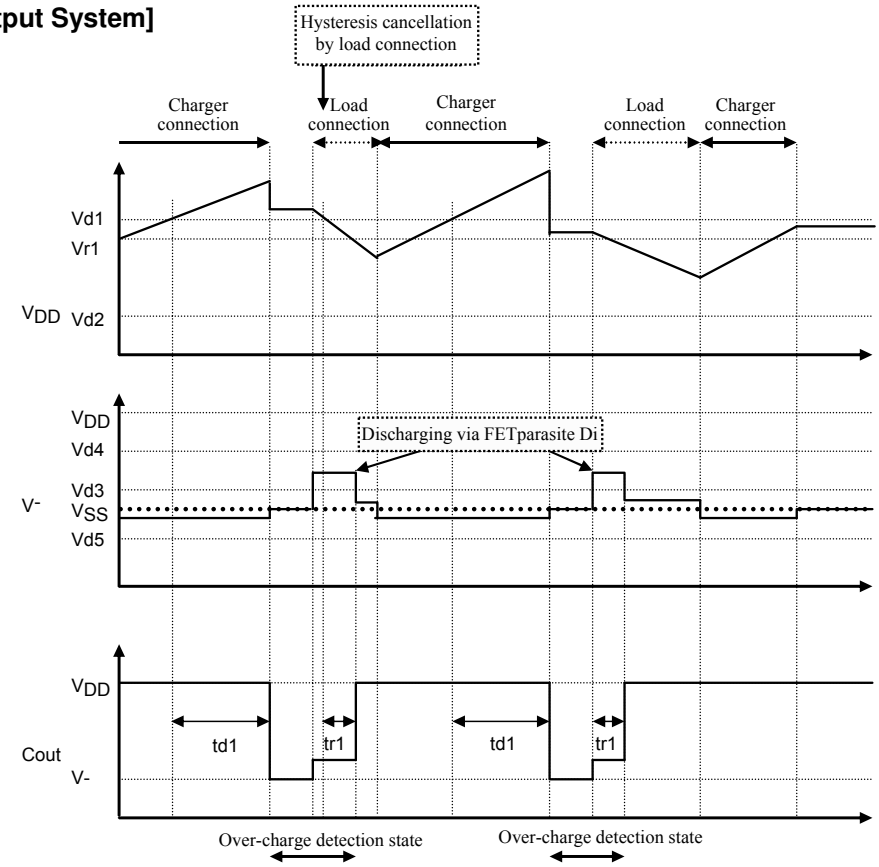
Operation in case of detection overlap

Overlap state		Operation in case of detection overlap	State after detection
When, during over-charge detection,	Over-discharge detection is made,	Over-charge detection is preferred. If over-discharge state continues even after over-charge detection, over-discharge detection is resumed.	When over-charge detection is made first, V^- is released. When over-discharge is detected after over-charge detection, the standby state is not effectuated. Note that V^- is connected to V_{DD} via 200kΩ.
	Over-current detection is made,	(*1) Both detections' can be made in parallel. Over-charge detection continues even when the over-current state occurs. If the over-charge state occurs first, over-current detection is interrupted.	(*2) When over-current is detected first, V^- is connected to V_{SS} via 1MΩ. When over-charge detection is made first, V^- is released.
When, during over-discharge detection,	Over-charge detection is made,	Over-discharge detection is interrupted and over-charge detection is preferred. When over-discharge state continues even after over-charge detection, over-discharge detection is resumed.	The standby state is not effectuated when over-discharge detection is made after over-charge detection. Note that V^- is connected to V_{DD} via 200kΩ.
	Over-current detection is made,	(*3) Both detections can be made in parallel. Over-discharge detection continues even when the over-current state is effectuated first. Over-current detection is interrupted when the over-discharge state is effectuated first,	(*4) If over-current is detected in advance, V will be connected to V_{SS} via 1MΩ. After detecting over-discharge, V will be connected to V_{DD} via 200kΩ to get into standby state. If over-discharge is detected in advance, V will be connected to V_{DD} via 200kΩ to get into standby state.
When, during over-current detection,	Over-charge detection is made,	(*1)	(*2)
	Over-discharge detection is made,	(*3)	(*4)

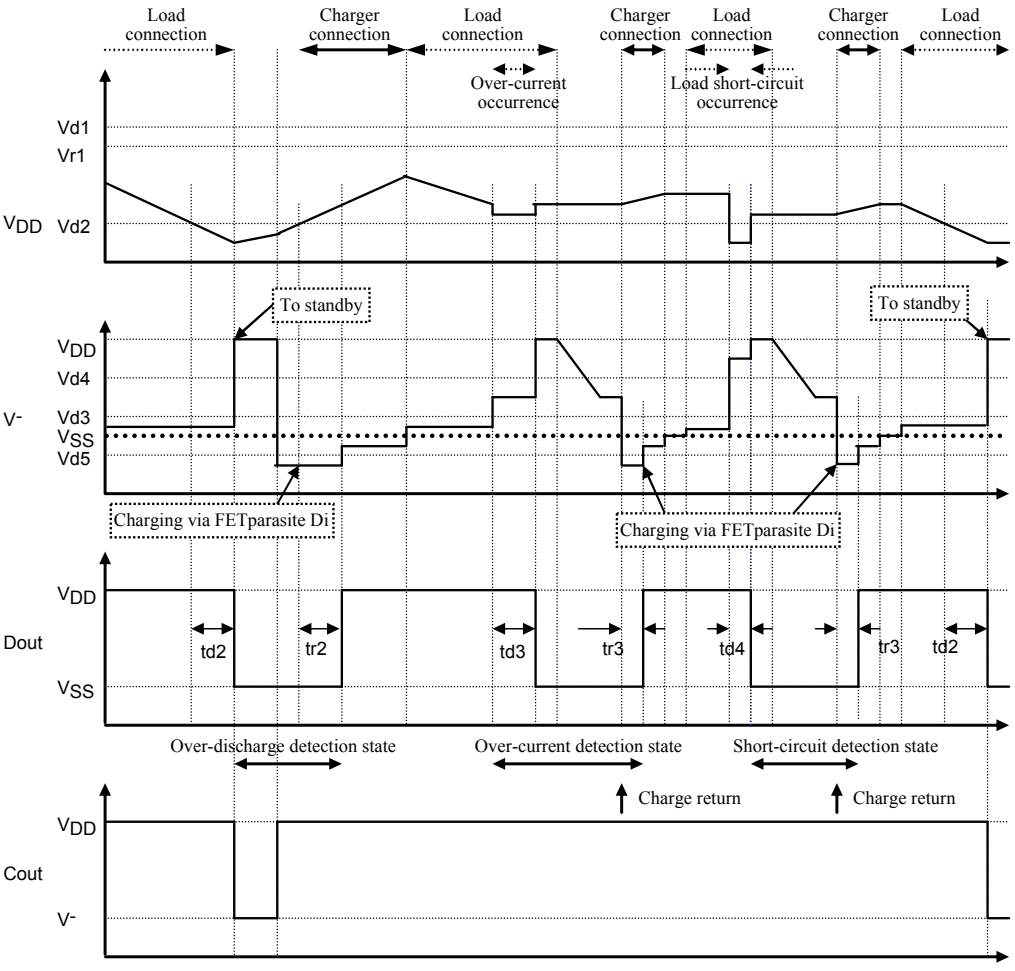
(Note) Short-circuit detection can be made independently.

Timing Chart

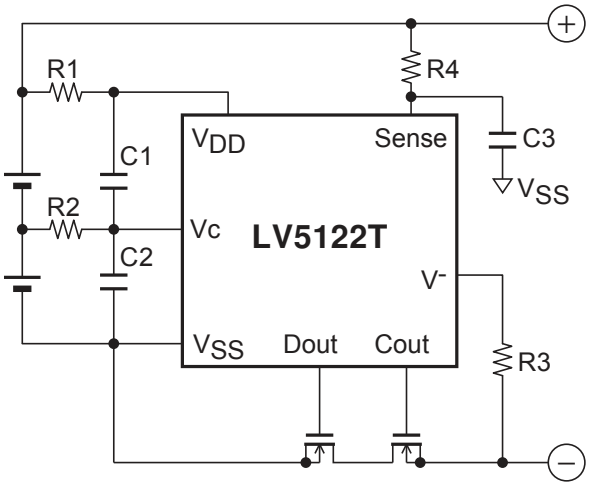
[Cout Output System]



[Dout Output System]



Application Circuit Example



Components	Recommended value	max	unit
R1, R2	100	1k	Ω
R3	2k	4k	Ω
R4	100	10k	Ω
C1, C2, C3	0.1μ	1μ	F

* These numbers don't mean to guarantee the characteristic of the IC.
* In addition to the components in the upper diagram, it is necessary to insert a capacitor with enough capacity between V_{DD} and V_{SS} of the IC as near as possible to stabilize the power supply voltage to the IC.

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV5122T-TLM-E	MSOP8 (150mil) (Pb-Free)	2000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF