STL80N3LLH6

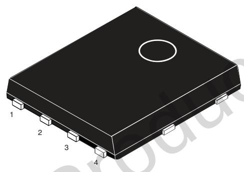
N-channel 30 V, 0.0046 Ω, 21 A PowerFLAT™ 5x6 STripFET™ VI DeepGATE™ Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STL80N3LLH6	30 V	0.0052 Ω	21 A [(1)]

1. The value is rated according $R_{thj\text{-}pcb}$

- $R_{DS(on)}$ * Q_g industry benchmark
- Extremely low on-resistance $R_{DS(on)}$
- High avalanche ruggedness
- Low gate drive power losses
- Very low switching gate charge



PowerFLAT™ 5x6

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 6[th] generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Figure 1. Internal schematic diagram

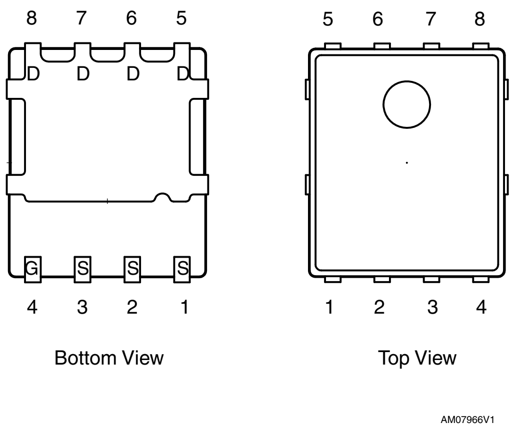


Table 1. Device summary

Order code	Marking	Package	Packaging
STL80N3LLH6	80N3LLH6	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	30	V
V_{GS}	Gate-source voltage	± 20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D (1)	Drain current (continuous) at T_C = 70 °C	60	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	51	A
I_D (2)	Drain current (continuous) at T_{pcb} = 25 °C	21	A
I_D (2)	Drain current (continuous) at T_{pcb}=70 °C	15.7	A
I_D (2)	Drain current (continuous) at T_{pcb}=100 °C	13.1	A
I_{DM} (3)	Drain current (pulsed)	84	A
P_{TOT} (1)	Total dissipation at T_C = 25 °C	60	W
P_{TOT} (2)	Total dissipation at T_{pcb} = 25 °C	4	W
	Derating factor	0.03	W/°C
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. The value is rated according to R_{thj-c}.
2. The value is rated according to $R_{thj-pcb}$.
3. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (drain, steady state)	2.08	°C/W
$R_{thj-pcb}$ (1)	Thermal resistance junction-ambient	31.3	°C/W

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 30 V, V_{DS} = 30 V at T_C =125 °C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250 µA	1	1.7	2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10 V, I_D= 10.5 A V_{GS}= 4.5 V, I_D= 10.5 A		0.0046 0.0067	0.0052 0.0076	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f=1 MHz, V_{GS}=0	1350 230 140	1690 290 176	2030 350 210	pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D = 21 A V_{GS} =4.5 V *(see Figure 14)*		17 8 6		nC nC nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	1.25	1.7	2	Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD}=15 V, I_D= 10.5 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 13)*	-	9.5 30 37 12	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		21	A
I_{SDM}(1)	Source-drain current (pulsed)		-		84	A
V_{SD}(2)	Forward on voltage	I_{SD} = 21 A, V_{GS}=0	-		1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 10.5 A, di/dt = 100 A/µs, V_{DD}=25 V	-	24 16.8 1.4		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

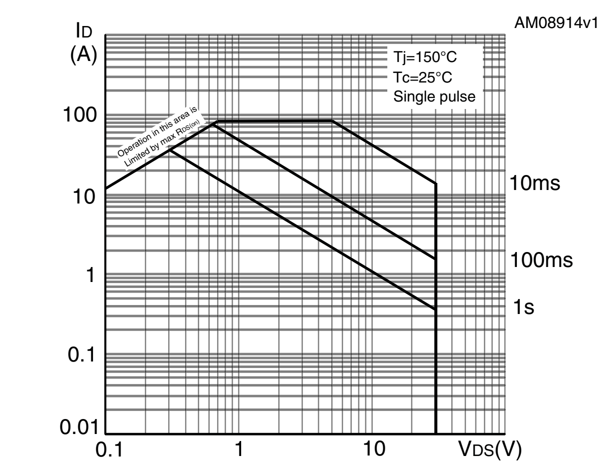


Figure 3. Thermal impedance

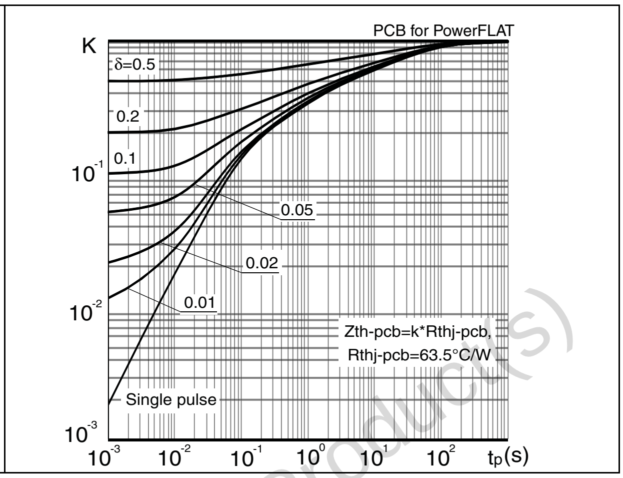


Figure 4. Output characteristics

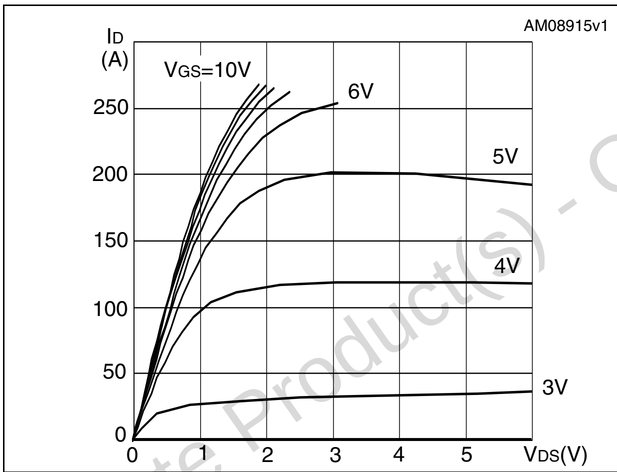


Figure 5. Transfer characteristics

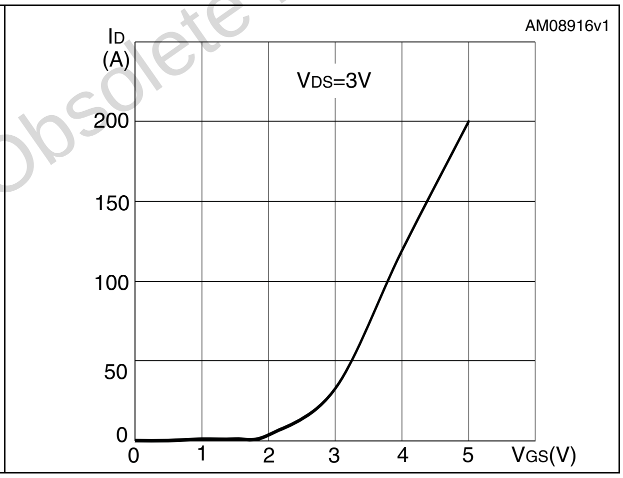


Figure 6. Normalized B_{VDSS} vs temperature

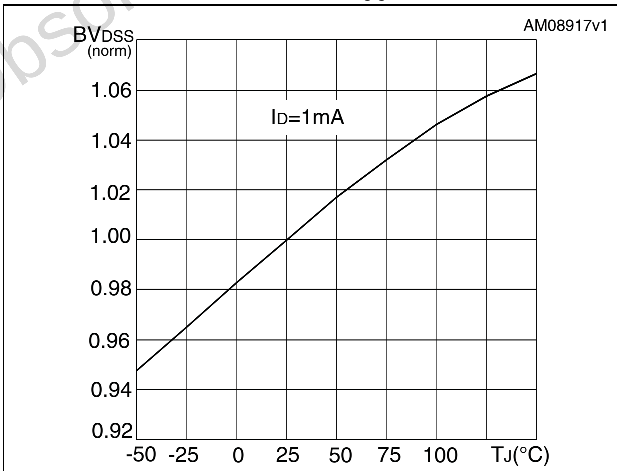


Figure 7. Static drain-source on resistance

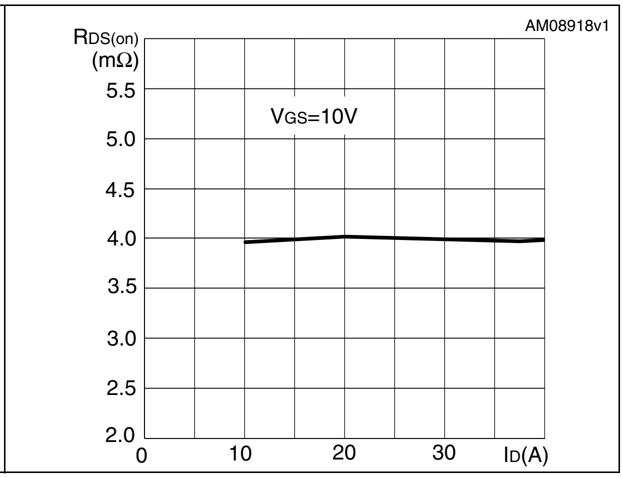


Figure 8. Gate charge vs gate-source voltage

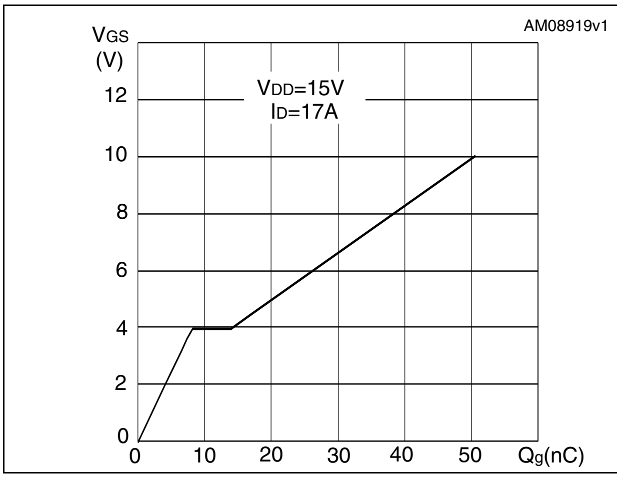


Figure 9. Capacitance variations

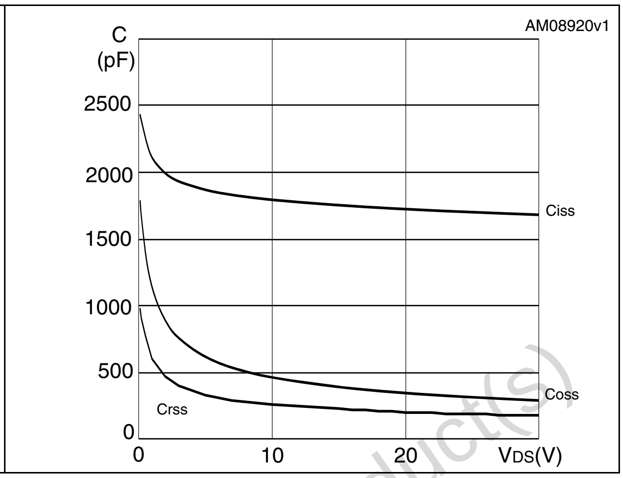


Figure 10. Normalized gate threshold voltage vs temperature

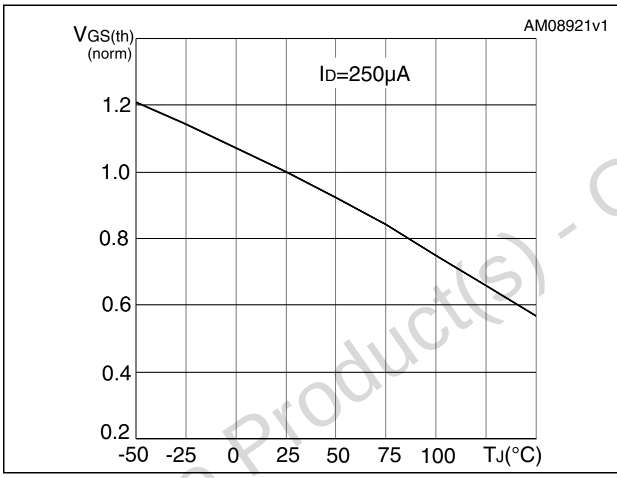


Figure 11. Normalized on resistance vs temperature

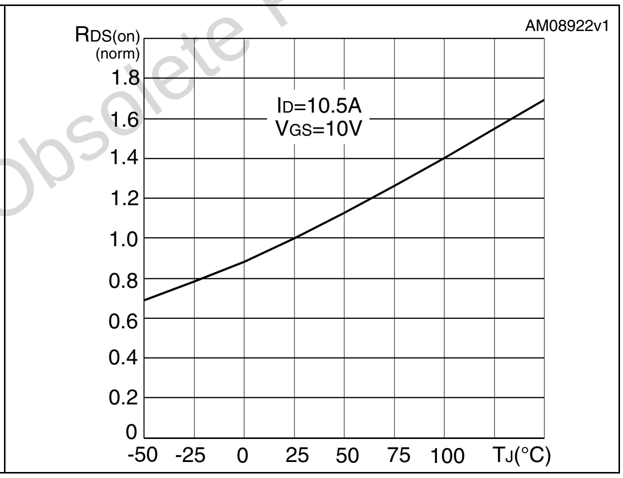
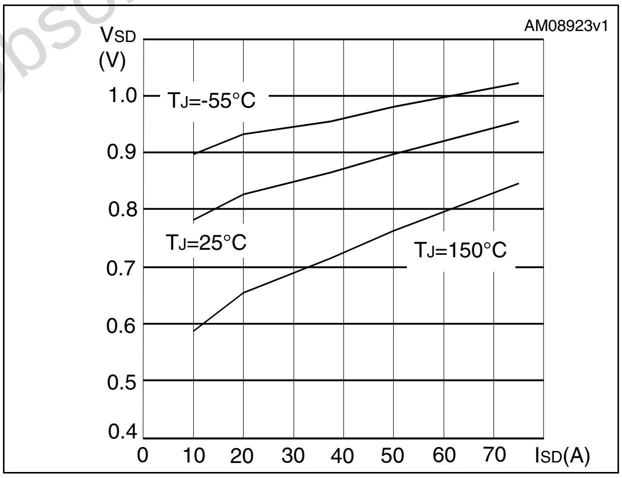


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

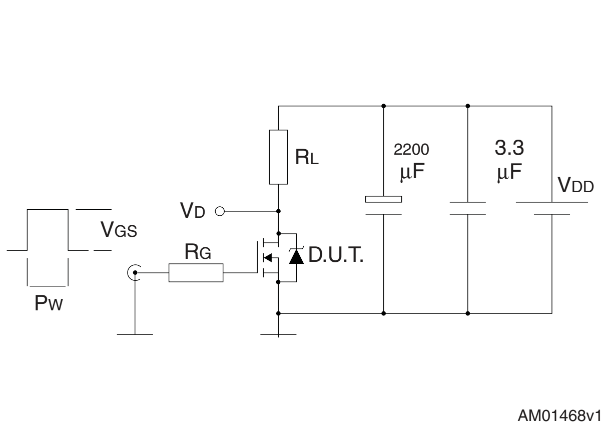


Figure 14. Gate charge test circuit

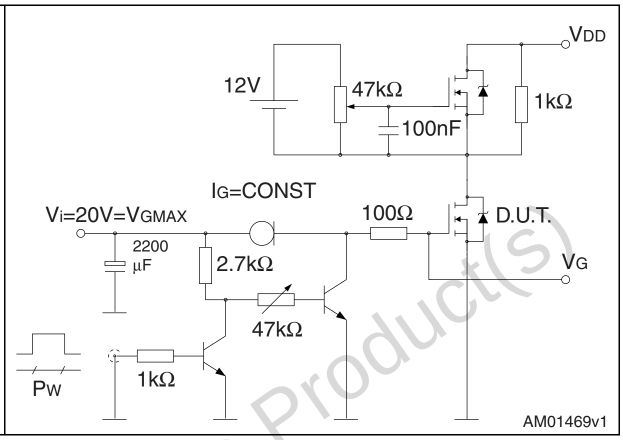


Figure 15. Test circuit for inductive load switching and diode recovery times

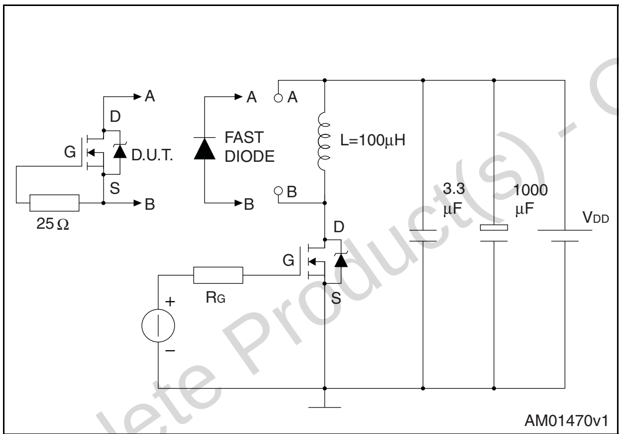


Figure 16. Unclamped inductive load test circuit

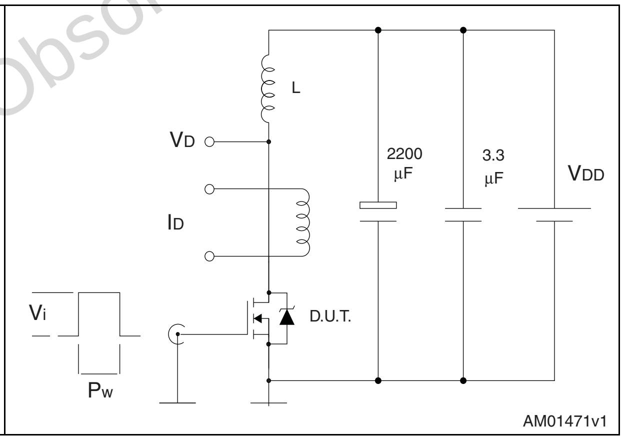


Figure 17. Unclamped inductive waveform

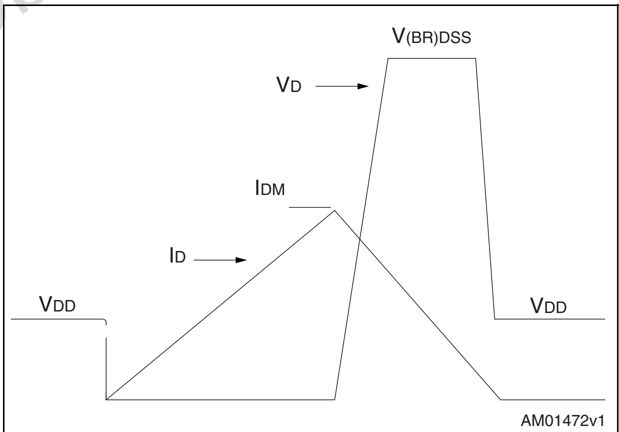
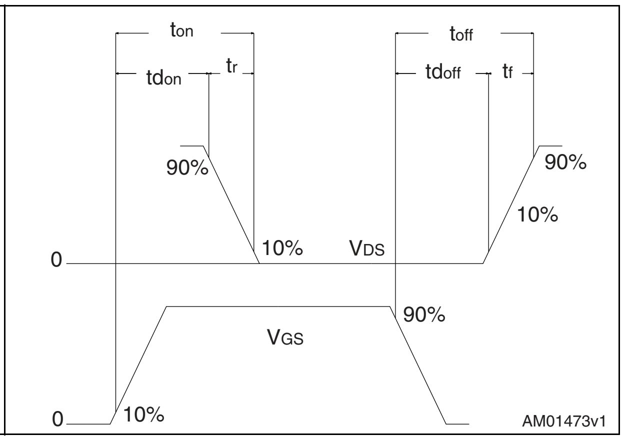


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerFLAT 5x6 type S-R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
L	0.50		0.80
K	1.275		1.575

Figure 19. PowerFLAT 5x6 type S-R drawing

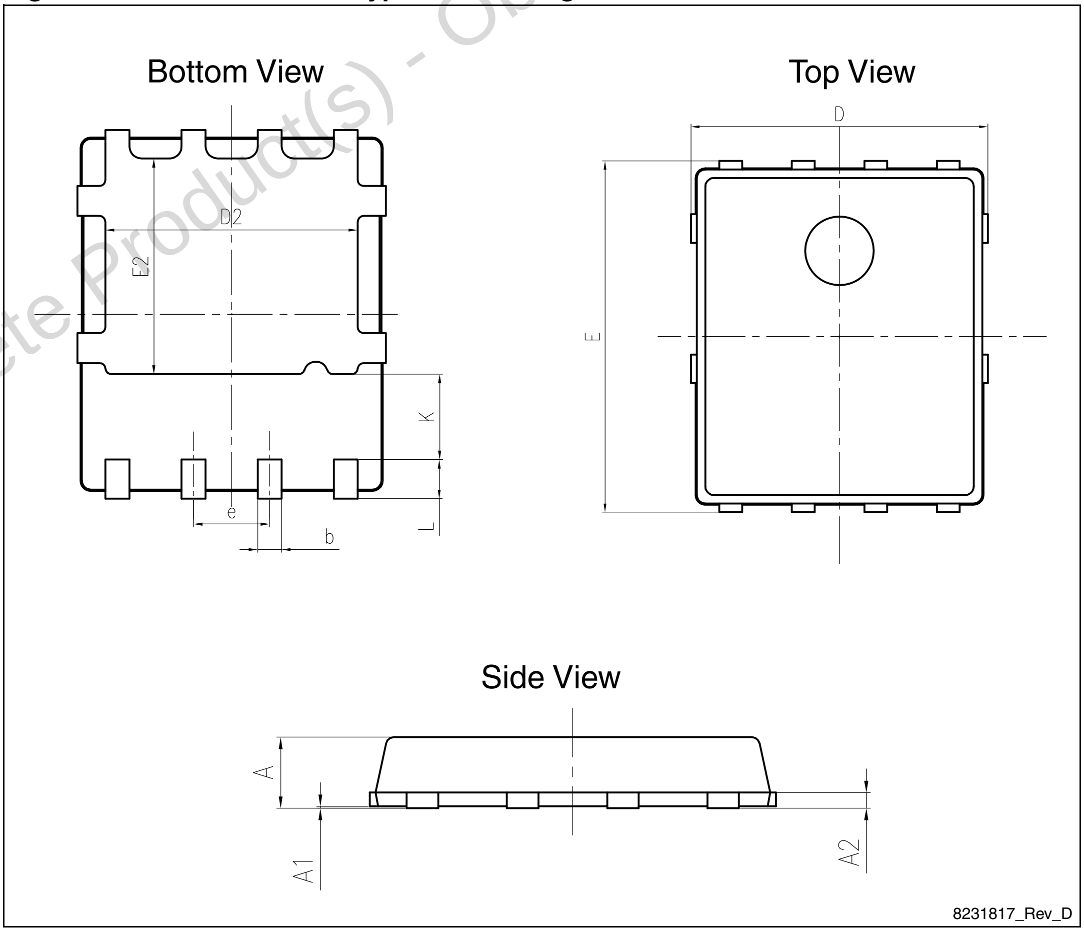
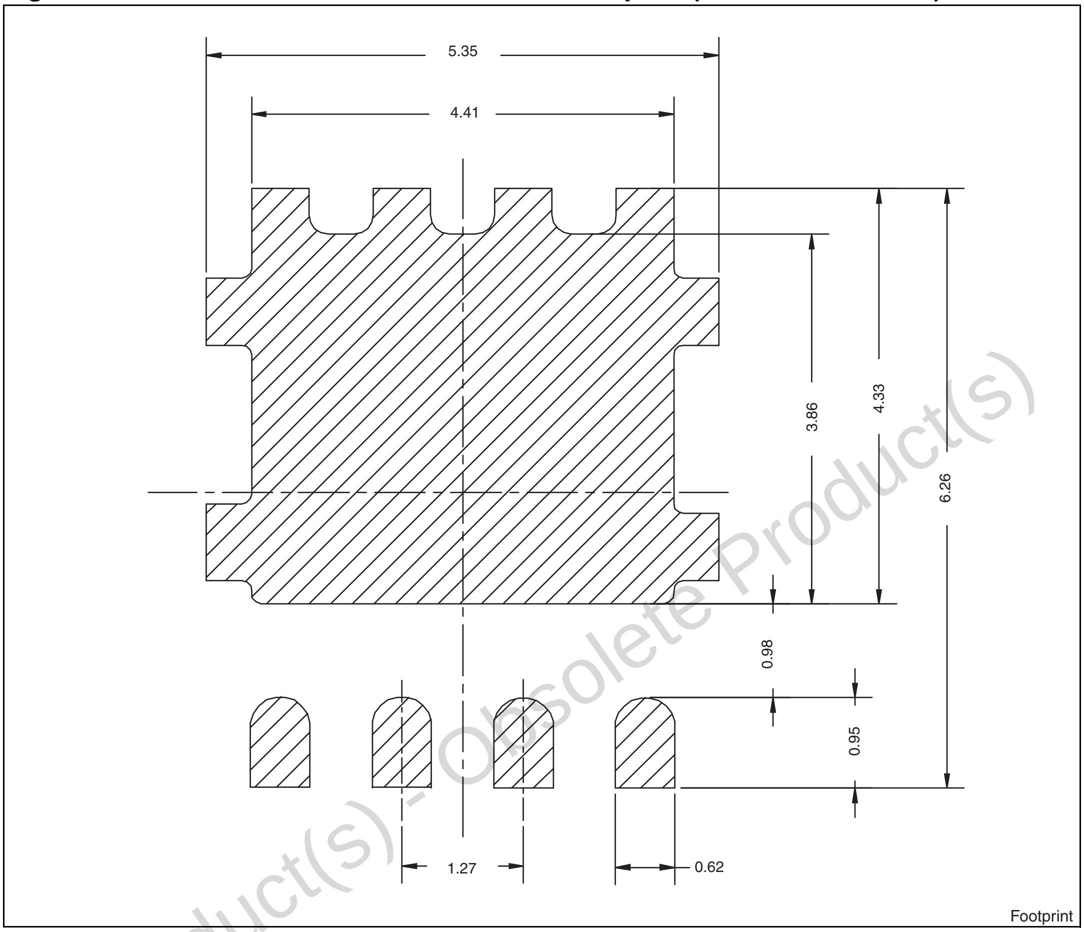


Figure 20. PowerFLAT™ 5x6 recommended footprint (dimensions in mm)



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
12-Nov-2009	1	First release.
30-Mar-2010	2	$R_{DS(on)}$ values changed in *Table 4: On/off states*
26-Sep-2011	3	– Document status promoted from preliminary data to datasheet; – Inserted I_D value @ 70 °C, in *Table 2: Absolute maximum ratings*.
02-Dec-2011	4	*Section 4: Package mechanical data* has been updated. Minor text changes.