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HCPL062N 3.3V Dual Channel High Speed-10 MBit/s Logic Gate Optocouplers

# The HCPL062N optocouplers consist of an AlGaAs LED, optically coupled to a very high speed integrated photo-

detector logic gate consisting of bipolar transistors on a CMOS process for reduced power consumption. The output features an open collector, thereby permitting wired OR outputs. The devices are housed in a compact small-outline package. The coupled parameters are guaranteed over the temperature range of -40°C to +85°C. An internal noise shield and provides superior common mode rejection.

# HCPL062N 3.3V Dual Channel High Speed-10 MBit/s Logic Gate **Optocouplers**

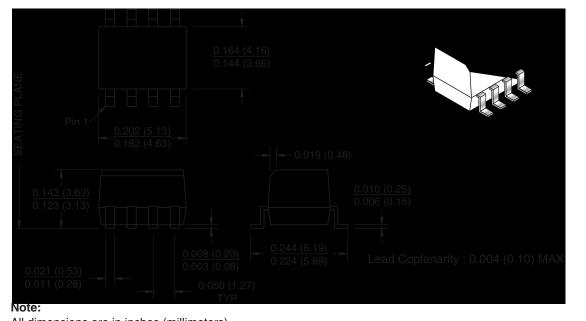
Description

## Features

- Compact SO8 package
- Very high speed 10MBit/s
- Superior CMR 25kV/µs minimum (1,000 volts common mode)
- Logic gate output
- Wired OR-open collector
- Fixed threshold detector design minimizes thermal impact on switching times
- U.L. recognized (File # E90700)

# **Applications**

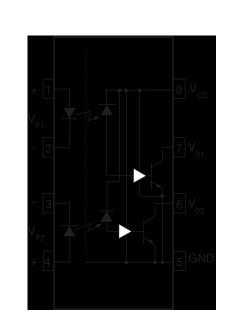
- Ground loop elimination
- Field buses
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer-peripheral interface
- Instrumentation input/output isolation



All dimensions are in inches (millimeters)







#### Note:

Circuit Drawing<sup>(1)</sup>

The V<sub>CC</sub> supply to each optoisolator must be bypassed by a 0.1µF capacitor or larger. This can be either a ceramic
or solid tantalum capacitor with good high frequency characteristic and should be connected no further than 3mm
from the V<sub>CC</sub> and GND pins of each device.

#### Truth Table (Positive Logic)

Input	Output
Н	L
L	Н

A  $0.1 \mu F$  bypass capacitor must be connected between pins 8 and 5.

HCPL062N
3.3V
Dual
.062N 3.3V Dual Channel
High
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0 MBit/s
Logic
Gate
Optocoupler
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Absolute Maximum	Ratings	(No derating required up to 85°C)
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Symbol	Parameter	Value	Units
T <sub>STG</sub>	Storage Temperature	-40 to +125	°C
T <sub>OPR</sub>	Operating Temperature	-40 to +85	°C
EMITTER		łł	
١ <sub>F</sub>	DC/Average Forward Input Current (each channel)	50	mA
V <sub>R</sub>	Reverse Input Voltage (each channel)	5.0	V
PI	Power Dissipation	45	mW
DETECTOR		łł	
V <sub>CC</sub> (1 minute max)	Supply Voltage	7.0	V
Ι <sub>Ο</sub>	Output Current (each channel)	15	mA
V <sub>O</sub>	Output Voltage (each channel)	7.0	V
Po	Collector Output Power Dissipation	85	mW

## **Recommended Operating Conditions**

Symbol	Parameter	Min.	Max.	Units
I <sub>FL</sub>	Input Current, Low Level	0	250	μA
I <sub>FH</sub>	Input Current, High Level	6.3 <sup>(2)</sup>	15	mA
V <sub>CC</sub>	Supply Voltage, Output	2.7	3.3	V
T <sub>A</sub>	Operating Temperature	-40	+85	°C
N	Fan Out (TTL load)	_	5	TTL Loads
RL	Output Pull-up	330	4K	Ω

Note:

2. 6.3mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0mA or less

# **Electrical Characteristics** ( $T_A = -40^{\circ}C$ to $+85^{\circ}C$ Unless otherwise specified.)

#### **Individual Component Characteristics**

Symbol	Parameter	Test Conditions	Min.	Typ. <sup>(3)</sup>	Max.	Unit
EMITTER			•	•		
V <sub>F</sub>	Input Forward Voltage	I <sub>F</sub> = 10mA	-	-	1.8	V
		T <sub>A</sub> =25°C	-	-	1.75	
B <sub>VR</sub>	Input Reverse Breakdown Voltage	Ι <sub>R</sub> = 10μΑ	5.0	-	_	V
$\Delta V_F / \Delta T_A$	Input Diode Temperature Coefficient	I <sub>F</sub> = 10mA	-	-1.5	_	mV/°C
DETECTO	R	-				
I <sub>CCH</sub>	High Level Supply Current	$I_{F} = 0mA, V_{CC} = 3.3V$	-	7.1	10	mA
I <sub>CCL</sub>	Low Level Supply Current	I <sub>F</sub> = 10mA, V <sub>CC</sub> = 3.3V	_	6.7	15	mA

#### Switching Characteristics (T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 3.3V, I<sub>F</sub> = 7.5 mA Unless otherwise specified.)

Symbol	AC Characteristics	Test Conditions	Min.	Typ. <sup>(3)</sup>	Max.	Unit
T <sub>PLH</sub>	Propagation Delay Time to Output High Level	$R_L = 350\Omega, C_L = 15pF$ Note 4, Fig. 10	-	-	90	ns
T <sub>PHL</sub>	Propagation Delay Time to Output Low Level	$R_L = 350\Omega$ , $C_L = 15pF$ Note 5, Fig. 10	-	_	75	ns
IT <sub>PHL</sub> –T <sub>PLH</sub> I	Pulse Width Distortion	$R_L = 350\Omega$ , $C_L = 15pF$ Fig. 10	-	-	25	ns
t <sub>r</sub>	Output Rise Time (10–90%)	$R_L = 350\Omega, C_L = 15pF)$ Note 6, Fig. 10	-	16	_	ns
t <sub>f</sub>	Output Fall Time (90–10%)	$R_L = 350\Omega$ , $C_L = 15pF$ Note 7, Fig. 10	-	4	-	ns
ICM <sub>H</sub> I	Common Mode Transient Immunity (at Output High Level)		25,000	_	_	V/µs
ICMLI	Common Mode Transient Immunity (at Output Low Level)	$\label{eq:RL} \begin{array}{l} R_{L} = 350\Omega, \ T_{A} = 25^\circ C, \ I_{F} = 7.5 mA, \\ V_{CC} = 3.3V, \ V_{O(Max.)} = 0.8V \\ IV_{CM}I = 1,000V \\ Notes \ 9, \ 11, \ Fig. \ 11 \end{array}$	25,000	_	_	V/µs

Transfer Characteristics	$T_A = -40^{\circ}C$ to $+85^{\circ}C$ Unless	otherwise specified.)
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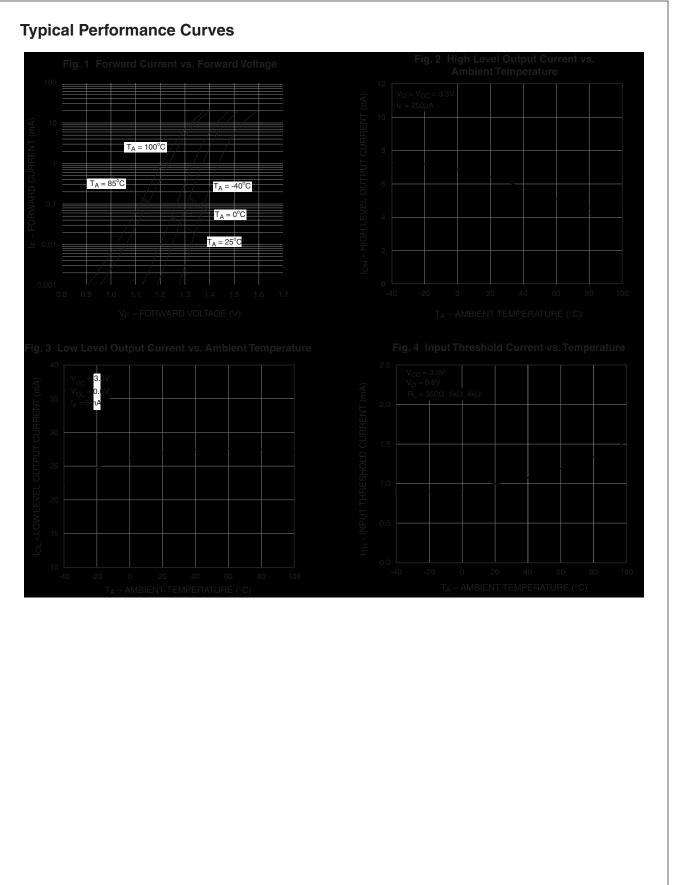
Symbol	DC Characteristics	Test Conditions	Min.	Typ. <sup>(3)</sup>	Max.	Unit
V <sub>OL</sub>	Low Level Output Voltage	$V_{CC} = 3.3V$ , $I_F = 5mA$ , $I_{OL} = 13mA$	_	_	0.6	V
I <sub>FT</sub>	Input Threshold Current	$V_{CC} = 3.3V, V_O = 0.6V, I_{OL} = 13mA$	_	_	5	mA

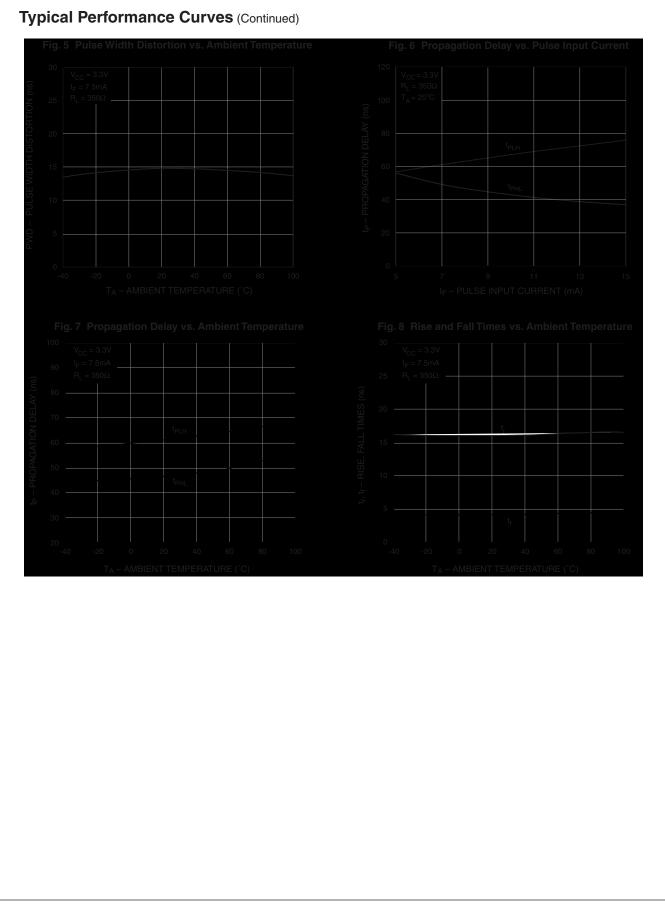
Isolation Characteristics (T<sub>A</sub> = -40°C to +85°C Unless otherwise specified.)

Symbol	Characteristics	Test Conditions	Min.	Typ. <sup>(3)</sup>	Max.	Unit
I <sub>I-O</sub>	Input-Output Insulation Leakage Current	$\label{eq:relative} \begin{split} & \text{Relative humidity} = 45\% \\ & \text{T}_{\text{A}} = 25^{\circ}\text{C}, \ \text{t} = 5 \ \text{sec.} \\ & \text{V}_{\text{I-O}} = 3000 \ \text{VDC}, \ \text{Note 10} \end{split}$	_	_	1.0	μΑ
V <sub>ISO</sub>	Withstand Insulation Test Voltage	$\label{eq:R_H} \begin{array}{l} R_{H} < 50\%,  T_{A} = 25^{\circ}C \\ I_{I \text{-}O} \leq 2\mu\text{A},  t = 1   \text{min.}, \\ \text{Note 10} \end{array}$	2500	_	_	V <sub>RMS</sub>
R <sub>I-O</sub>	Resistance (Input to Output)	V <sub>I-O</sub> = 500V, Note 10	-	10 <sup>12</sup>	-	Ω
C <sub>I-O</sub>	Capacitance (Input to Output)	f = 1MHz, Note 10	_	0.6	_	pF

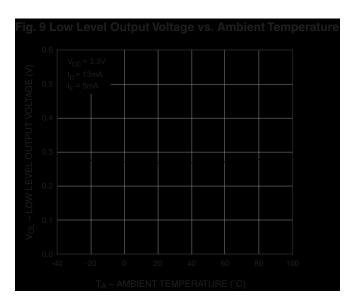
#### Notes:

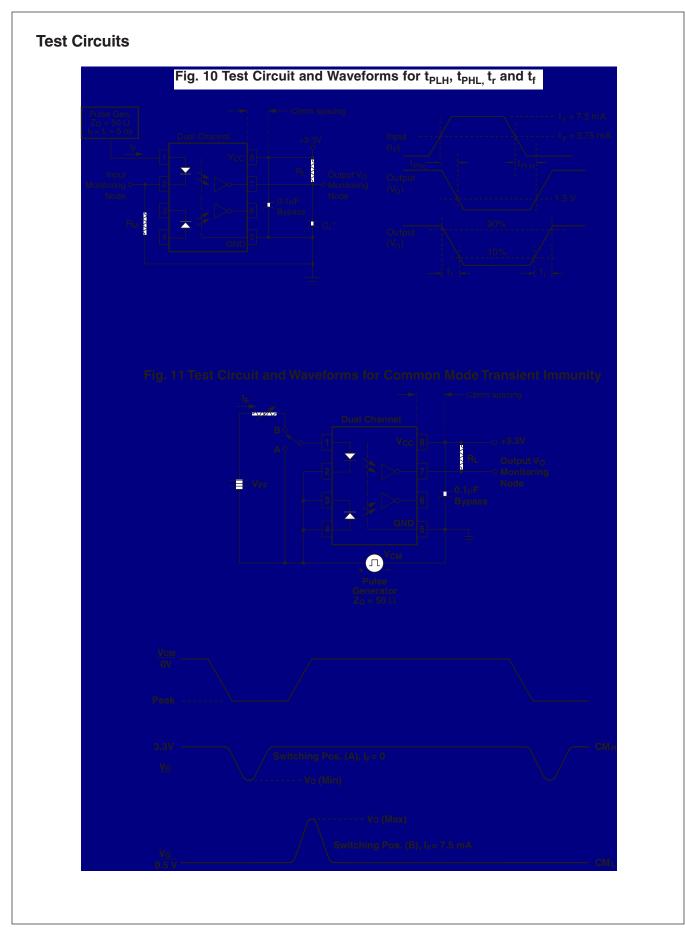
- 3. All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C unless otherwise specified.
- t<sub>PLH</sub> Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
- t<sub>PHL</sub> Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
- 6.  $t_r$  Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
- 7.  $t_f$  Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
- CM<sub>H</sub> The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state (i.e., V<sub>OUT</sub> > 2.0 V). Measured in volts per microsecond (V/μs).
- CM<sub>L</sub> The maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state (i.e., V<sub>OUT</sub> < 0.8 V). Measured in volts per microsecond (V/μs).</li>
- 10. Device considered a two-terminal device: Pins 1,2,3 and 4 shorted together, and Pins 5,6,7 and 8 shorted together.
- 11. The power supply bypass capacitors must be no further than 3mm from the leads of the optocoupler. A low inductance ground plane width of with ≤ 5nHy of series lead inductance is required.



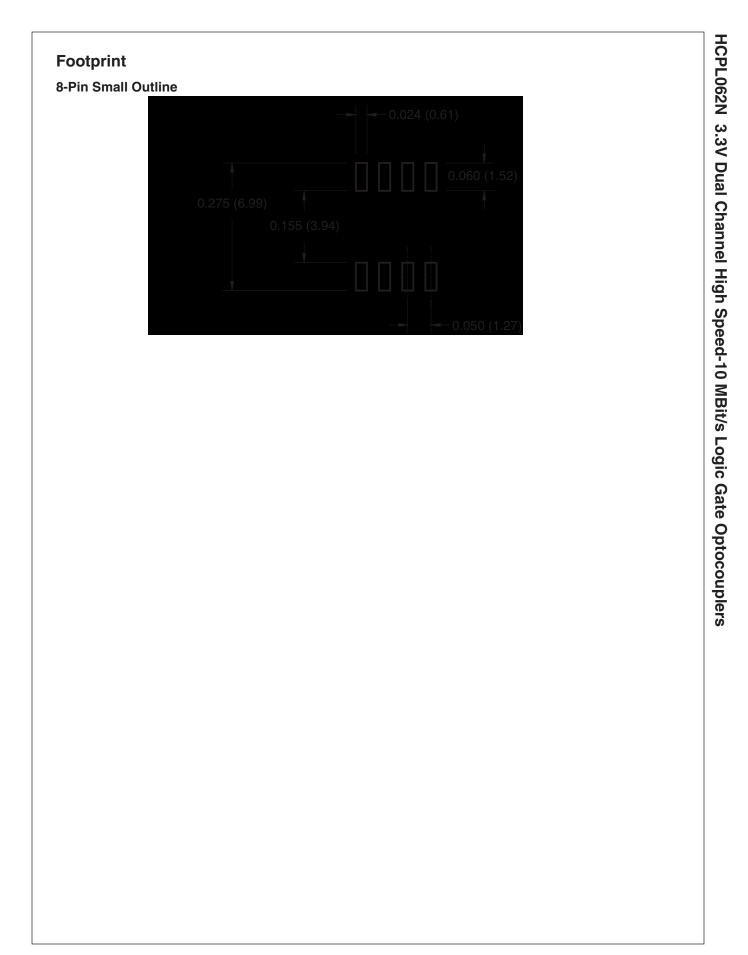








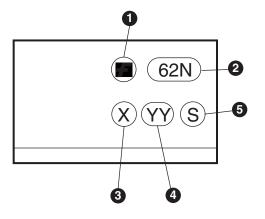
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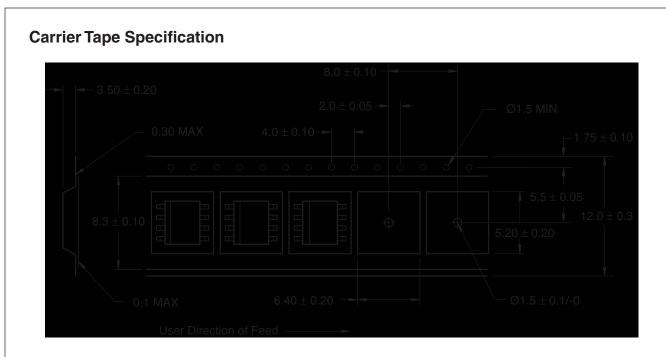
## **Ordering Information**

Option	Order Entry Identifier	Description	
No Suffix	HCPL062N	Shipped in tubes (50 units per tube)	
R1	HCPL062NR1	Tape and Reel (500 units per reel)	
R2	HCPL062NR2	Tape and Reel (2500 units per reel)	

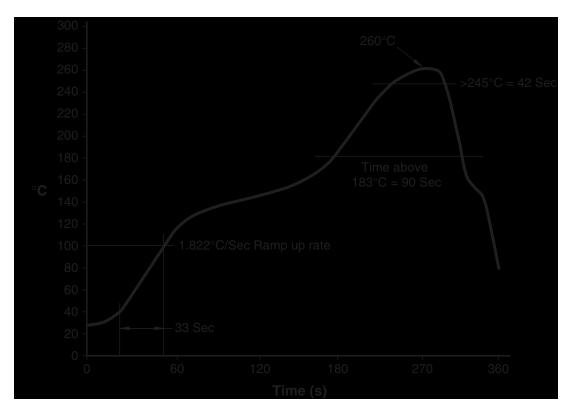
## **Marking Information**



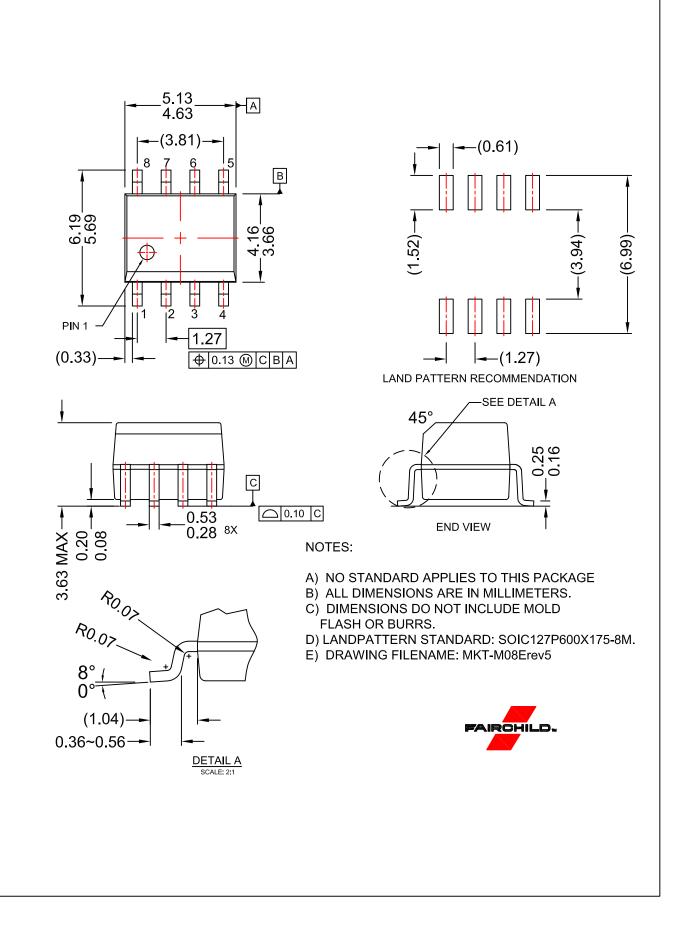
Definiti	Definitions		
1	Fairchild logo		
2	Device number		
3	One digit year code, e.g., '3'		
4	Two digit work week ranging from '01' to '53'		
5	Assembly package code		



#### **Reflow Profile**



HCPL062N 3.3V Dual Channel High Speed-10 MBit/s Logic Gate Optocouplers



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