

March 1992

### Features

- **Fast Access Time**
  - $V_{DD} = 5V$  ..... 450ns
  - $V_{DD} = 10V$  ..... 250ns
- **Common Data Inputs and Outputs**
- **Multiple Chip Select Inputs to Simplify Memory System Expansion**

### Description

The CDP1823 and CDP1823C are 128-word by 8-bit CMOS SOS static random-access memories. These memories are compatible with general-purpose microprocessors. The two memories are functionally identical. They differ in that the CDP1823 has a recommended operating voltage range of 4 volts to 10.5 volts, and the CDP1823C has a recommended operating voltage range of 4 volts to 6.5 volts.

The CDP1823 memory has 8 common data input and data output terminals for direct connection to a bidirectional data bus and is operated from a single voltage supply. Five chip-select inputs are provided to simplify memory-system expansion. In order to enable the CDP1823, the chip-select inputs  $\overline{CS2}$ ,  $\overline{CS3}$  and  $\overline{CS5}$  require a low input signal, and the chip-select inputs  $\overline{CS1}$  and  $\overline{CS4}$  require a high input signal.

The  $\overline{MRD}$  signal enables all 8 output drivers when in the low state and should be in a high state during a write cycle.

After valid data appear at the output, the address inputs may be changed immediately. Output data will be valid until either the  $\overline{MRD}$  signal goes high, the device is deselected, or  $t_{AA}$  (access time) after address changes.

The CDP1823 and CDP1823C types are supplied in 24-lead dual-in-line ceramic packages (D suffix), and in 24-lead dual-in-line plastic packages (E suffix).

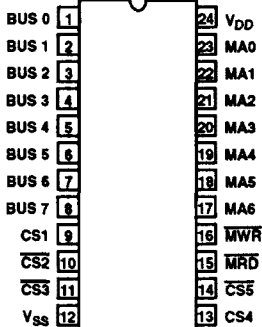
### Ordering Information

PACKAGE	TEMP. RANGE	5V	10V
Plastic DIP Burn-In	-40°C to +85°C	CDP1823CE	CDP1823E
		CDP1823CEX	CDP1823EX
Ceramic DIP Burn-In *883B	-40°C to +85°C	CDP1823CD	CDP1823D
		CDP1823CDX	-
	-55°C to +125°C	CDP1823CD3	-

\*Respective specifications are included at the end of this datasheet.

### Pinout

24 LEAD DIP  
TOP VIEW



OPERATIONAL MODES

FUNCTION	$\overline{MRD}$	$\overline{MWR}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{CS4}$	$\overline{CS5}$	BUS TERMINAL STATE
Read	0	X	1	0	0	1	0	Storage State of Addressed Word
Write	1	0	1	0	0	1	0	Input High-Impedance
Stand-By (Active)	1	1	1	0	0	1	0	High Impedance
Not Selected	X	X	0	X	X	X	X	High Impedance
	X	X	X	1	X	X	X	High Impedance
	X	X	X	X	1	X	X	High Impedance
	X	X	X	X	X	0	X	High Impedance
	X	X	X	X	X	X	1	High Impedance

Logic 1 = High, Logic 0 = Low, X = Don't Care

## Specifications CDP1823, CDP1823C

### Absolute Maximum Ratings

DC Supply Voltage Range, ( $V_{DD}$ ):

(All Voltages Referenced to  $V_{SS}$  Terminal)

CDP1823 ..... -0.5V to +11V

CDP1823C ..... -0.5V to +7V

Input Voltage Range, All Inputs ..... -0.5V to  $V_{DD}$  +0.5V

DC Input Current, Any One Input .....  $\pm 10\mu\text{A}$

Operating Temperature Range ( $T_A$ ):

Package Type D ..... -55°C to +125°C

Package Type E ..... -40°C to +85°C

Storage Temperature Range ( $T_{stg}$ ) ..... -65°C to +150°C

Lead Temperature (During Soldering):

At distance 1/16  $\pm$  1/32 In. (1.59  $\pm$  0.79mm)

from case for 10s max ..... +265°C

### Recommended Operating Conditions

At  $T_A$  = Full Package Temperature Range. For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	CDP1823D		CDP1823CD		
	MIN	MAX	MIN	MAX	
Supply Voltage Range	4	10.5	4	6.5	V
Recommended Input Voltage Range	$V_{SS}$	$V_{DD}$	$V_{SS}$	$V_{DD}$	V

### Static Electrical Characteristics

At  $T_A$  = -40°C to +85°C, Except as Noted:

CHARACTERISTIC	SYMBOL	CONDITIONS			LIMITS						UNITS
		$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	CDP1823			CDP1823C			
					MIN	(Note 1) TYP	MAX	MIN	(Note 1) TYP	MAX	
Quiescent Device Current	$I_{DD}$	-	0, 5	5	-	-	500	-	-	500	$\mu\text{A}$
		-	0, 10	10	-	-	1000	-	-	-	$\mu\text{A}$
Output Low (Sink) Current	$I_{OL}$	0.4	0, 5	5	2	4	-	2	4	-	$\text{mA}$
		0.5	0, 10	10	4.5	9	-	-	-	-	$\text{mA}$
Output High (Source) Current	$I_{OH}$	4.6	0, 5	5	-1	-2	-	-1	-2	-	$\text{mA}$
		9.5	0, 10	10	-2.2	-4.4	-	-	-	-	$\text{mA}$
Output Voltage Low-Level	$V_{OL}$	-	0, 5	5	-	0	0.1	-	0	0.1	V
		-	0, 10	10	-	0	0.1	-	-	-	V
Output Voltage High-Level	$V_{OH}$	-	0, 5	5	4.9	5	-	4.9	5	-	V
		-	0, 10	10	9.9	10	-	-	-	-	V
Input Low Voltage	$V_{iL}$	0.5, 4.5	-	5	-	-	1.5	-	-	1.5	V
		0.5, 9.5	-	10	-	-	3	-	-	-	V
Input High Voltage	$V_{iH}$	0.5, 9.5	-	5	3.5	-	-	3.5	-	-	V
		0.5, 9.5	-	10	7	-	-	-	-	-	V
Input Leakage Current	$I_{IN}$	Any Input	0, 5	5	-	-	$\pm 5$	-	-	$\pm 5$	$\mu\text{A}$
			0, 10	10	-	-	$\pm 10$	-	-	-	$\mu\text{A}$
Operating Current (Note 2)	$I_{DD1}$	-	0, 5	5	-	4	8	-	4	8	$\text{mA}$
		-	0, 10	10	-	8	16	-	-	-	$\text{mA}$
3-State Output Leakage Current	$I_{OUT}$	0, 5	0, 5	5	-	-	$\pm 5$	-	-	$\pm 5$	$\mu\text{A}$
		0, 10	0, 10	10	-	-	$\pm 10$	-	-	-	$\mu\text{A}$
Input Capacitance	$C_{IN}$	-	-	-	-	5	7.5	-	5	7.5	$\text{pF}$
Output Capacitance	$C_{OUT}$	-	-	-	-	10	15	-	10	15	$\text{pF}$

#### NOTES:

- Typical values are for  $T_A$  = +25°C and nominal  $V_{DD}$ .
- Outputs open circuited; Cycle time = 1 $\mu\text{s}$ .

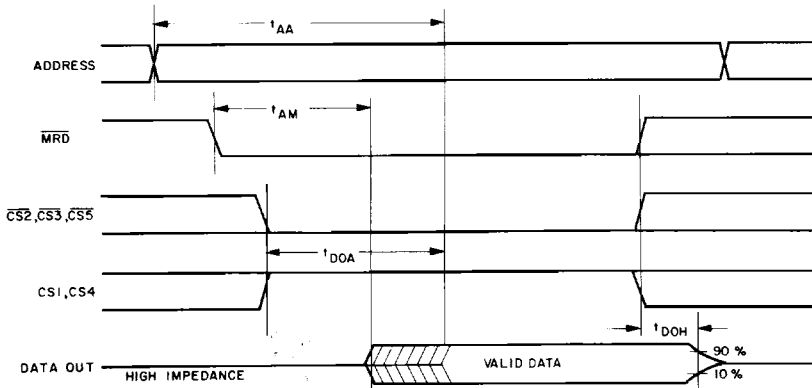
## CDP1823, CDP1823C

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} \pm 5\%$ ,  
 $t_r, t_f = 20$  ns,  $C_L = 100$  pF.

CHARACTERISTIC	VDD (V)	LIMITS						UNITS
		CDP1823			CDP1823C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
<b>Read Cycle (See Fig. 1)</b>								
Access Time From Address Change, $t_{AA}$	5	—	275	450	—	275	450	ns
Access Time From Chip Select, $t_{DOA}$	10	—	150	250	—	—	—	
MRD to Output Active, $t_{AM}$	5	—	150	250	—	150	250	
Data Hold Time After Read, $t_{DOH}$	10	—	100	150	—	—	—	
	5	25	50	75	25	50	75	
	10	15	25	40	—	—	—	

\* Typical values are at  $T_A = 25^\circ\text{C}$  and nominal voltage.

† Time required by a limit device to allow for the indicated function.



NOTE:  $\overline{MRD}$  IS HIGH DURING READ OPERATION.  
 TIMING MEASUREMENT REFERENCE IS  $0.5 V_{DD}$ .

Fig. 1 - Read cycle timing diagram.

## CDP1823, CDP1823C

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = -40$  to  $+85^\circ\text{C}$ ,  $V_{DD} \pm 5\%$ ,  $t_r, t_f = 20$  ns,  $C_L = 100$  pF.

CHARACTERISTIC	VDD (V)	LIMITS						UNITS
		CDP1823			CDP1823C			
		Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
<b>Write Cycle (See Fig. 2)</b>								
Write Recovery, $t_{WR}$	5	75	—	—	75	—	—	ns
	10	50	—	—	—	—	—	
Write Cycle, $t_{WC}$	5	400	—	—	400	—	—	
	10	225	—	—	—	—	—	
Write Pulse Width, $t_{WRW}$	5	200	—	—	200	—	—	
	10	100	—	—	—	—	—	
Address Setup Time, $t_{AS}$	5	125	—	—	125	—	—	
	10	75	—	—	—	—	—	
Data Setup Time, $t_{DS}$	5	100	—	—	100	—	—	
	10	75	—	—	—	—	—	
Data Hold Time From $\overline{MWR}$ , $t_{DH}$	5	75	—	—	75	—	—	
	10	50	—	—	—	—	—	

\*Typical values are at  $T_A = 25^\circ\text{C}$  and nominal voltage.

†Time required by a limit device to allow for the indicated function.

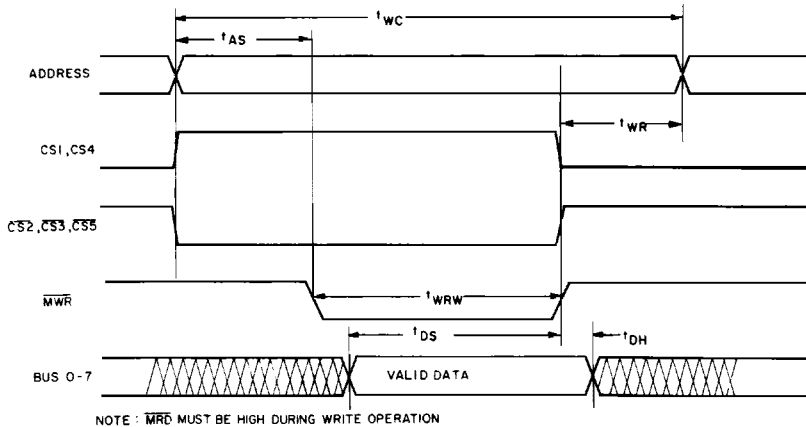


Fig. 2 - Write cycle timing diagram.

# CDP1823, CDP1823C

**DATA RETENTION CHARACTERISTICS** at  $T_A = -40$  to  $+85^\circ\text{C}$ ; see Fig. 3

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	$V_{DR}$ (V)	$V_{DD}$ (V)	CDP1823			CDP1823C			
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Min. Data Retention Voltage, $V_{DR}$	—	—	—	1.5	2	—	1.5	2	V
Data Retention Quiescent Current, $I_{DD}$	2	—	—	30	100	—	30	100	$\mu\text{A}$
Chip Deselect to Data Retention Time, $t_{CDR}$	—	5	600	—	—	600	—	—	ns
	—	10	300	—	—	—	—	—	
Recovery to Normal Operation Time, $t_{RC}$	—	5	600	—	—	600	—	—	
	—	10	300	—	—	—	—	—	
$V_{DD}$ to $V_{DR}$ Rise and Fall Time $t_r, t_f$	2	5	1	—	—	1	—	—	$\mu\text{s}$

\*Typical values are for  $T_A = 25^\circ\text{C}$  and nominal  $V_{DD}$ .

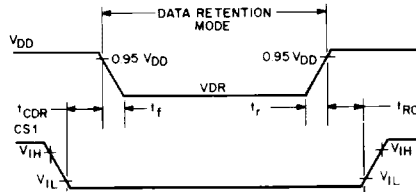
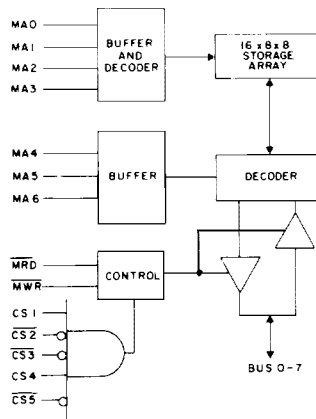


Fig. 3 - Low  $V_{DD}$  data retention timing waveforms.



Functional Diagram

Fig. 4 - Functional diagram.

# CDP1823, CDP1823C

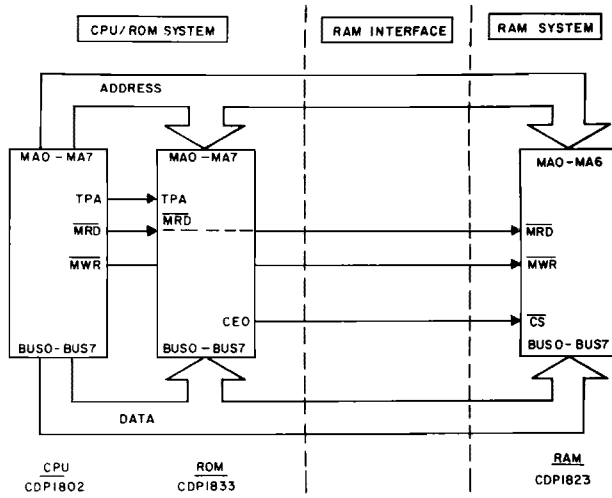


Fig. 5 - CDP1823 (128 x 8) minimum system (128 x 8)