V_{DS}	1200 V
I_{DS}	300 A

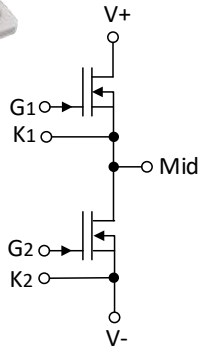
WAB300M12BM3

1200 V, 300 A All-Silicon Carbide
THB-80 Qualified, Switching Optimized, Half-Bridge Module

Technical Features

- Industry Standard 62 mm Footprint
- High Humidity Operation THB-80 (HV-H3TRB)
- High Junction Temperature (175 °C) Operation
- Implements Switching Optimized Third Generation SiC MOSFET Technology
- Low Inductance (10.2 nH) Design
- Silicon Nitride Insulator and Copper Baseplate

Package 105mm x 61.5 mm x 31.4 mm



Applications

- Railway & Traction
- Solar
- EV Chargers
- Industrial Automation & Testing

System Benefits

- Fast Time-to-Market with Minimal Development Required for Transition from 62mm Si IGBT Packages
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- High Reliability Material Selection

Key Parameters (T_C = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{DS\,max}$	Drain-Source Voltage			1200	V		
$V_{GS\,max}$	Gate-Source Voltage, Maximum Value	-8		+19		Transient, <100 ns	Fig. 32
$V_{GS\,op}$	Gate-Source Voltage, Recommended Op. Value	-4		+15		Static	
I_{DS}	DC Continuous Drain Current		382		A	V_{GS} = 15 V, T_C = 25 ˚C, T_{VJ} ≤ 175 ˚C	Fig. 20
			270			V_{GS} = 15 V, T_C = 90 ˚C, T_{VJ} ≤ 175 ˚C	Note 1
I_{SD}	DC Source-Drain Current		382			V_{GS} = 15 V, T_C = 25 ˚C, T_{VJ} ≤ 175 ˚C	
$I_{SD\,BD}$	DC Source-Drain Current (Body Diode)		190			V_{GS} = - 4 V, T_C = 25 ˚C, T_{VJ} ≤ 175 ˚C	
$I_{DS\,(pulsed)}$	Maximum Pulsed Drain-Source Current			600		t_{Pmax} limited by T_{jmax} V_{GS} = 15 V, T_C = 25 ˚C	
$I_{SD\,(pulsed)}$	Maximum Pulsed Source-Drain Current			600			
$T_{VJ\,op}$	Maximum Virtual Junction Temperature under Switching Conditions	-40		175	°C		

Note 1 Assumes $R_{TH\,JC}$ = 0.16 °W and $R_{DS(on)}$ = 6.4 mΩ. Calculate $P_D = (T_{VJ} - T_C) / R_{TH\,JC}$. Calculate $I_{D\_MAX} = \sqrt{(P_D / R_{DS(on)})}$

MOSFET Characteristics (Per Position) (T_{VJ} = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_D = 92 mA	
			2.0			V_{DS} = V_{GS}, I_D = 92 mA, T_{VJ}= 175 °C	
I_{DSS}	Zero Gate Voltage Drain Current		10	150	µA	V_{GS} = 0 V, V_{DS} = 1200 V	
I_{GSS}	Gate-Source Leakage Current		0.05	1		V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance (Devices Only)		4.0	5.2	mΩ	V_{GS} = 15 V, I_D = 300 A	Fig. 2 Fig. 3
			6.4			V_{GS} = 15 V, I_D = 300 A, T_{VJ} = 175 °C	
g_{fs}	Transconductance		212		S	V_{DS}= 20 V, I_{DS}= 300 A	Fig. 4
			200			V_{DS}= 20 V, I_{DS}= 300 A, T_{VJ} = 175 °C	
E_{On}	Turn-On Switching Energy, T_J = 25 °C T_J = 125 °C T_J = 175 °C		4.75 5.33 5.88		mJ	V_{DS} = 600 V, I_D = 300A, V_{GS} = -4 V/15 V, $R_{G(ext)}$ = 2.0 Ω, L= 20.7 µH	Fig. 11 Fig. 13
E_{Off}	Turn-Off Switching Energy, T_J = 25 °C T_J = 125 °C T_J = 175 °C		4.99 5.23 5.30				
$R_{G(int)}$	Internal Gate Resistance		1.4		Ω	T_{VJ} = 25 °C	
C_{iss}	Input Capacitance		24.5		nF	V_{GS} = 0 V, V_{DS} = 1000 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
C_{oss}	Output Capacitance		0.97				
C_{rss}	Reverse Transfer Capacitance		50		pF		
Q_{GS}	Gate to Source Charge		256		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 400 A Per IEC60747-8-4 pg 21	
Q_{GD}	Gate to Drain Charge		308				
Q_G	Total Gate Charge		908				
$R_{th\ JC}$	FET Thermal Resistance, Junction to Case		0.16	0.18	°C/W		Fig. 17

Body Diode Characteristics (Per Position) (T_{VJ} = 25 ˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Body Diode Forward Voltage		6.0		V	V_{GS} = -4 V, I_{SD} = 300 A	Fig. 7
			5.5			V_{GS} = -4 V, I_{SD} = 300 A, T_J = 175 °C	
t_{RR}	Reverse Recovery Time		36.5		ns	V_{GS} = -4 V, I_{SD} = 300 A, V_R = 600 V di_F/dt = 14.5 A/ns, T_J = 175 °C	
Q_{RR}	Reverse Recovery Charge		7.3		µC		
I_{RRM}	Peak Reverse Recovery Current		323		A		
E_{RR}	Reverse Recovery Energy T_J = 25 °C T_J = 125 °C T_J = 175 °C		0.65 1.98 3.01		mJ	V_{DS} = 600 V, I_D = 300A, V_{GS} = -4 V/15 V, $R_{G(ext)}$ = 2.0 Ω, L= 20.7 µH	Fig. 14

Module Physical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
R_{3-1}	Package Resistance, M1		0.60		mΩ	T_C = 125 °C, Note 2
R_{1-2}	Package Resistance, M2		0.51			T_C = 125 °C, Note 2
L_{Stray}	Stray Inductance		10.2		nH	Between Terminals 2 and 3
T_C	Case Temperature	-40		125	°C	
W	Weight		300		g	
M_S	Mounting Torque	4.5	5	5.5	N-m	Baseplate, M6 bolts
		4.5	5	5.5		Power Terminals, M6 bolts
V_{isol}	Case Isolation Voltage			5.5	kV	AC, 50 Hz, 1 min
CTI	Comparative Tracking Index		600			

Note 2 Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance.

Typical Performance

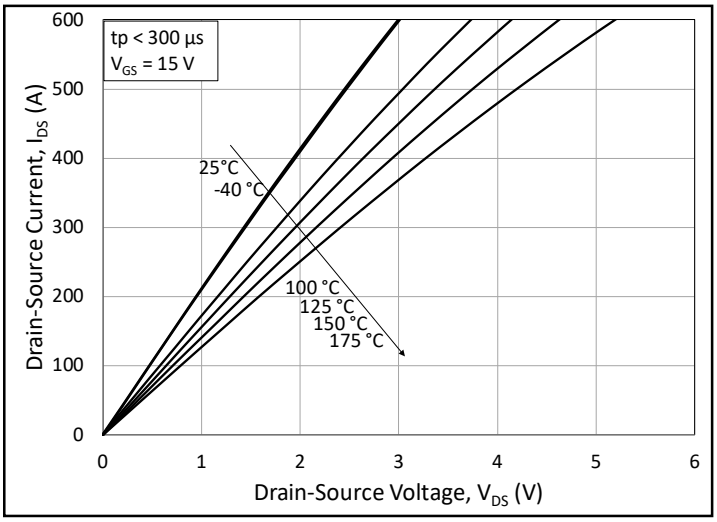


Figure 1. Output Characteristics for Various Junction Temperatures

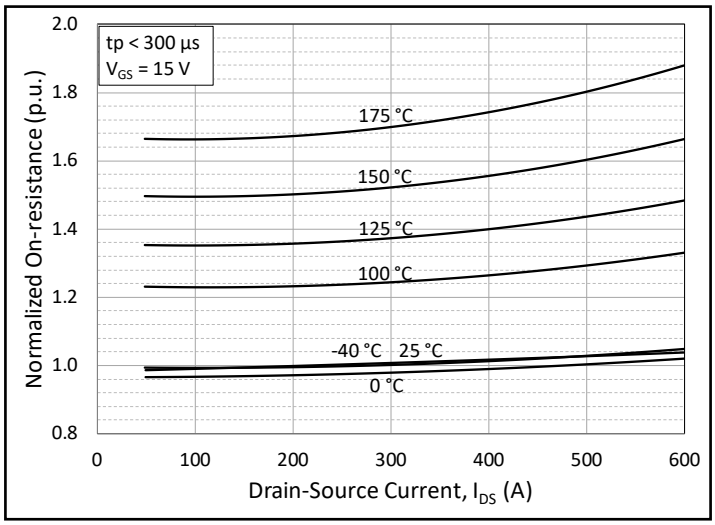


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Juction Temperatures

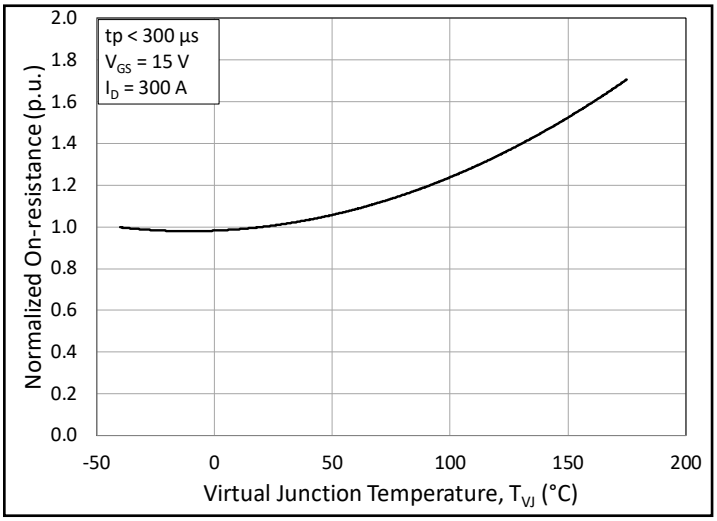


Figure 3. Normalized On-State Resistance vs. Juction Temperature

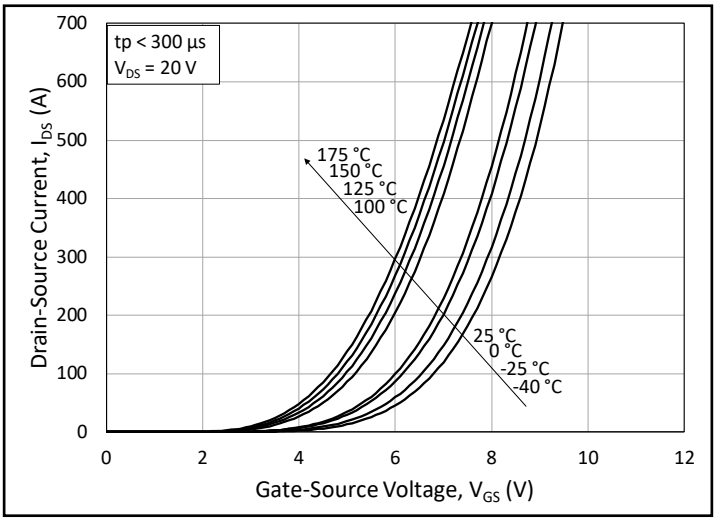


Figure 4. Transfer Characteristic for Various Junction Temperatures

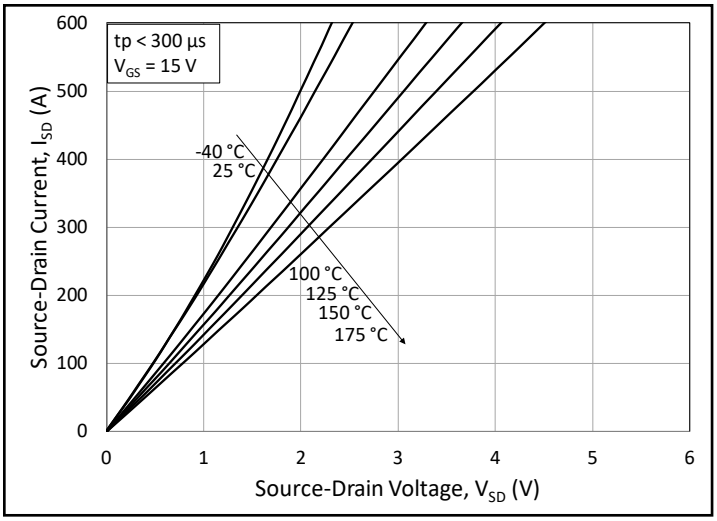


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

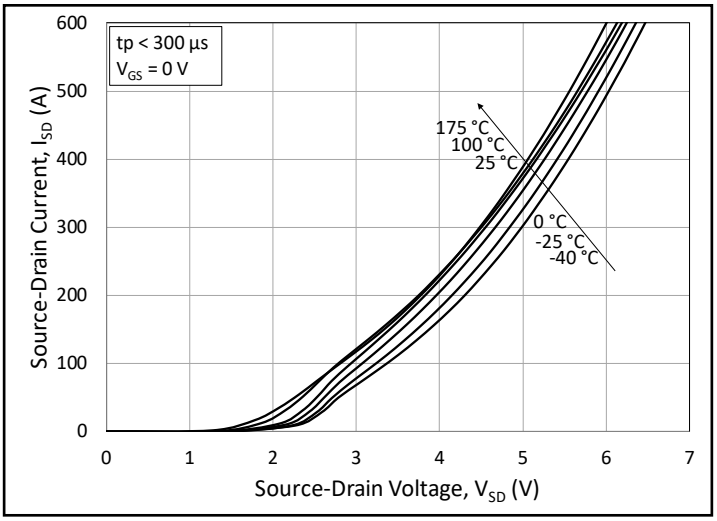


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V (Body Diode)

Typical Performance

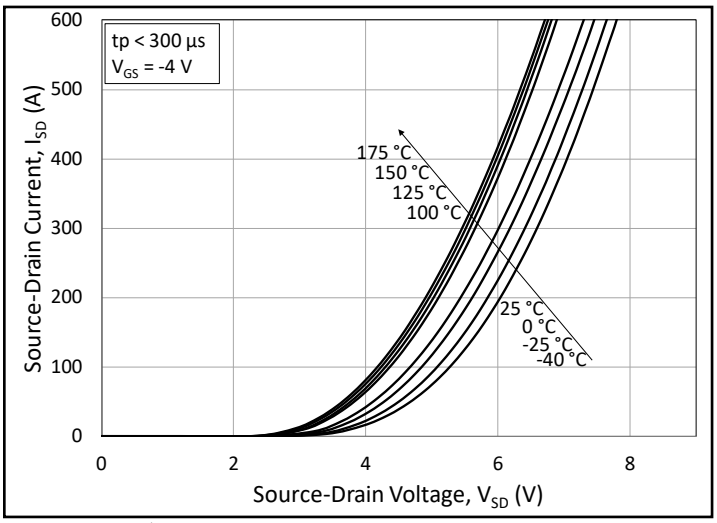


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Body Diode)

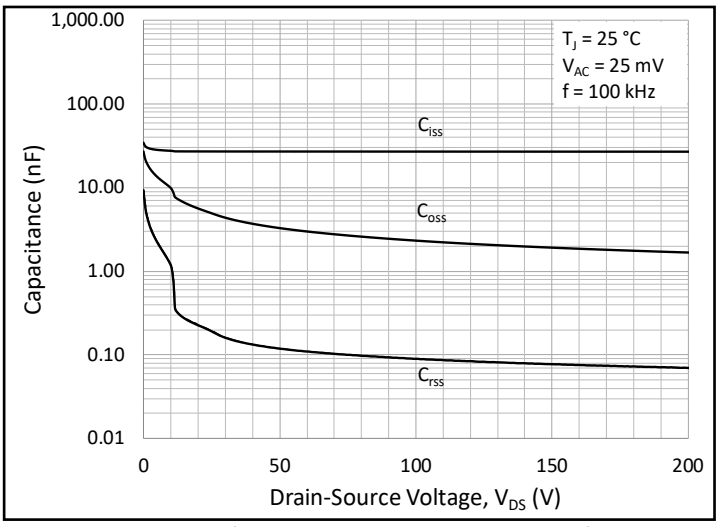


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

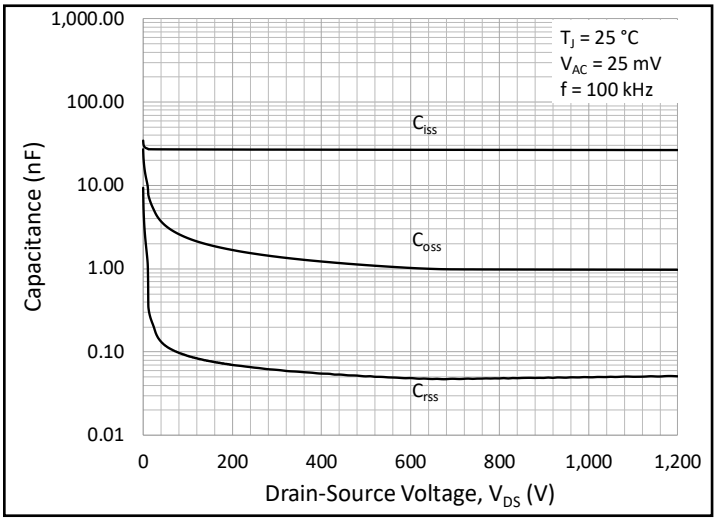


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

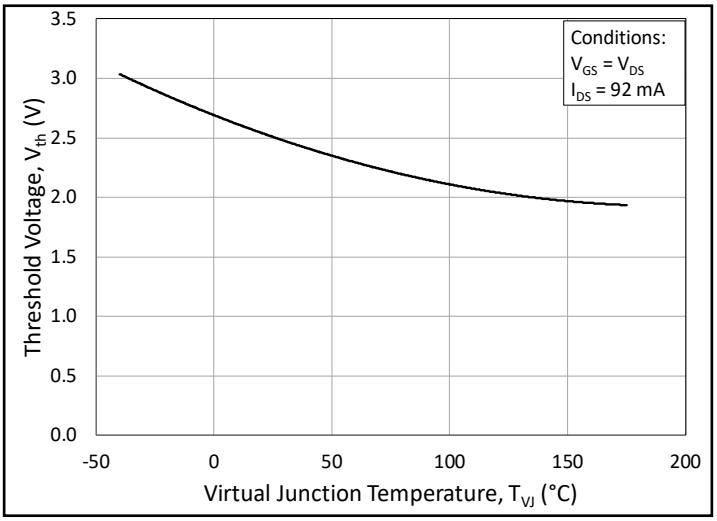


Figure 10. Threshold Voltage vs. Junction Temperature

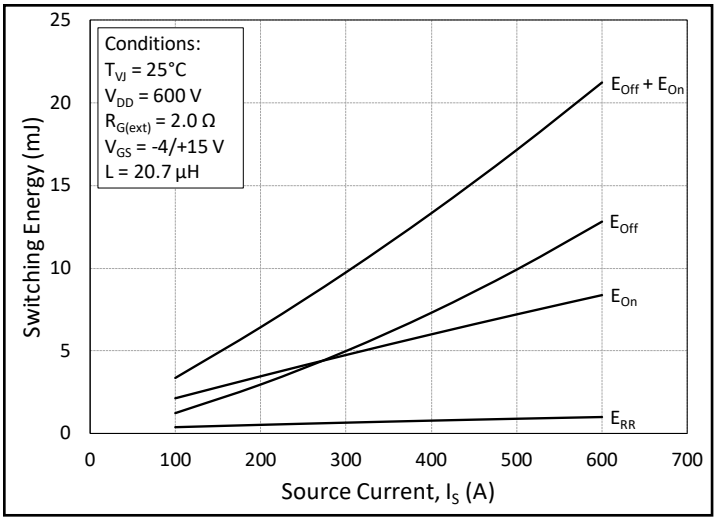


Figure 11. Switching Energy vs. Drain Current (V_{DS} = 600 V)

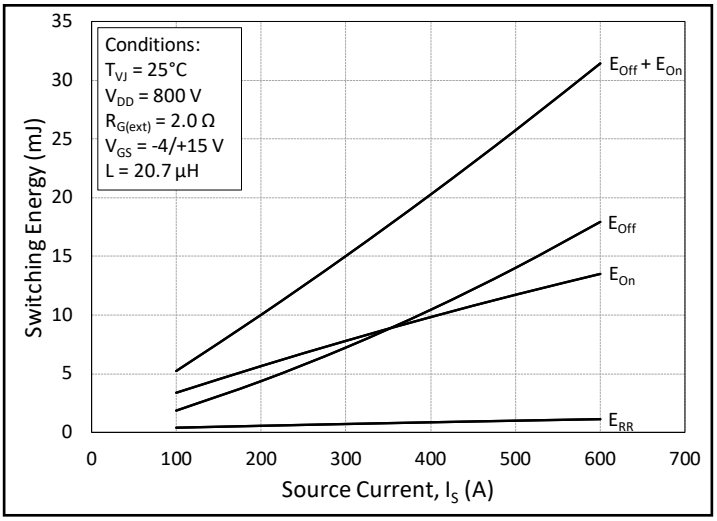


Figure 12. Switching Energy vs. Drain Current (V_{DS} = 800 V)

Typical Performance

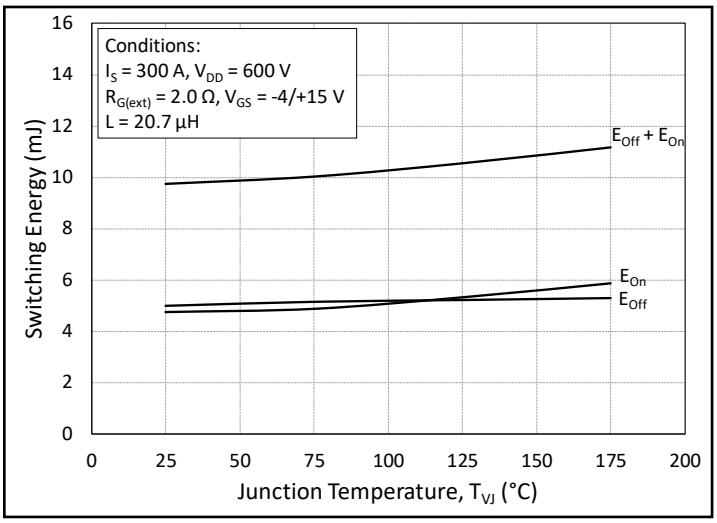


Figure 13. MOSFET Switching Energy vs. Junction Temperature

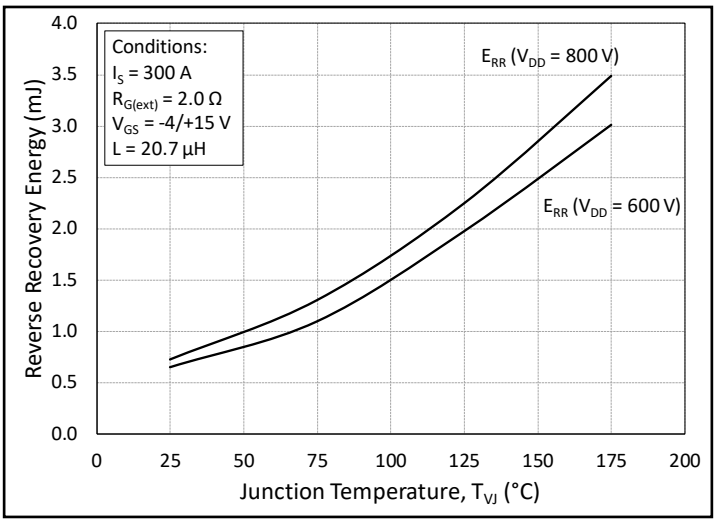


Figure 14. Reverse Recovery Energy vs. Junction Temperature

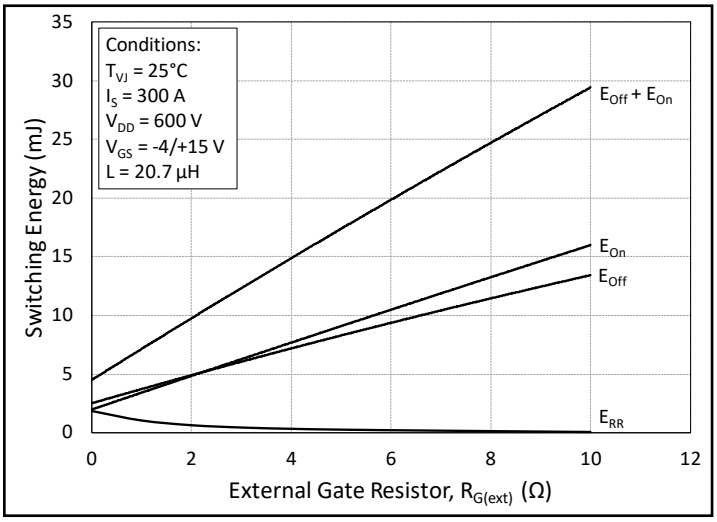


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

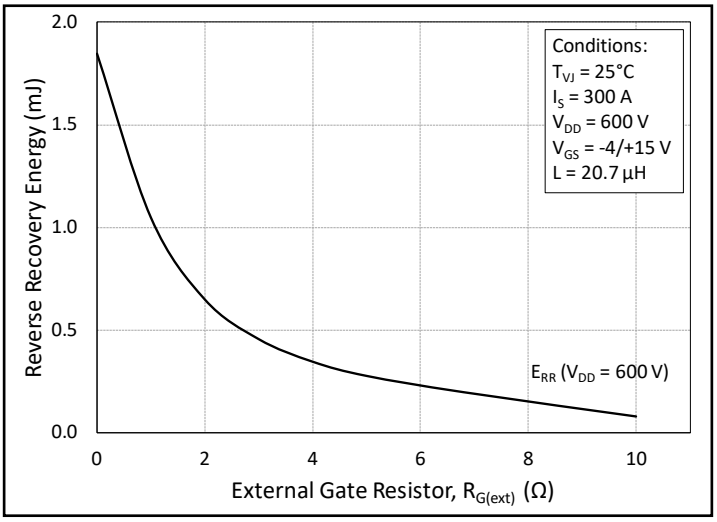


Figure 16. Reserve Recovery Energy vs. External Gate Resistance

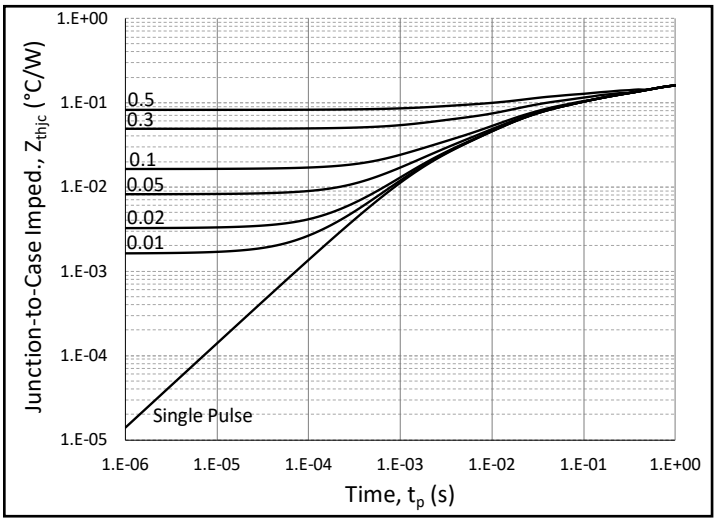


Figure 17. MOSFET Juction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

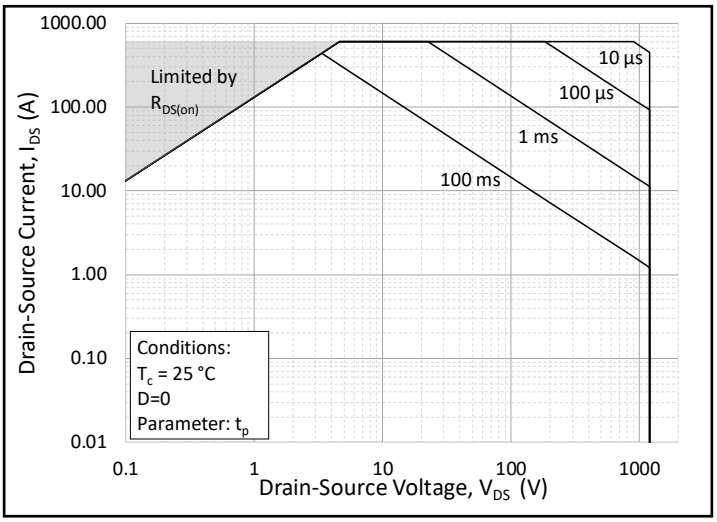


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

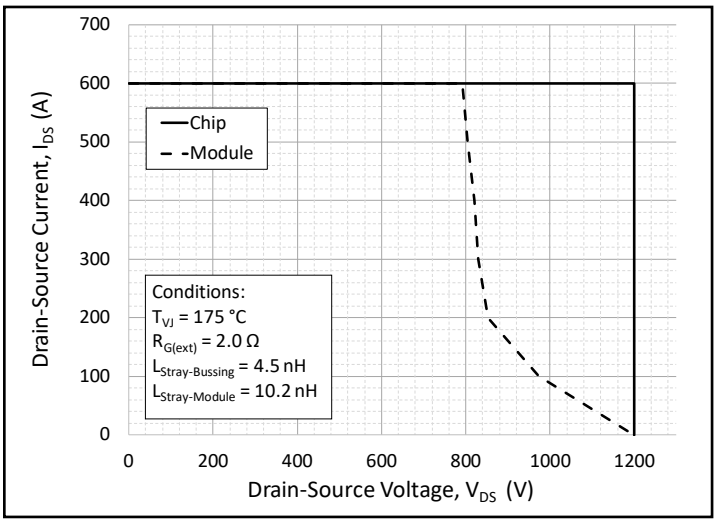


Figure 19. Reverse Bias Safe Operating Area (RBSOA)

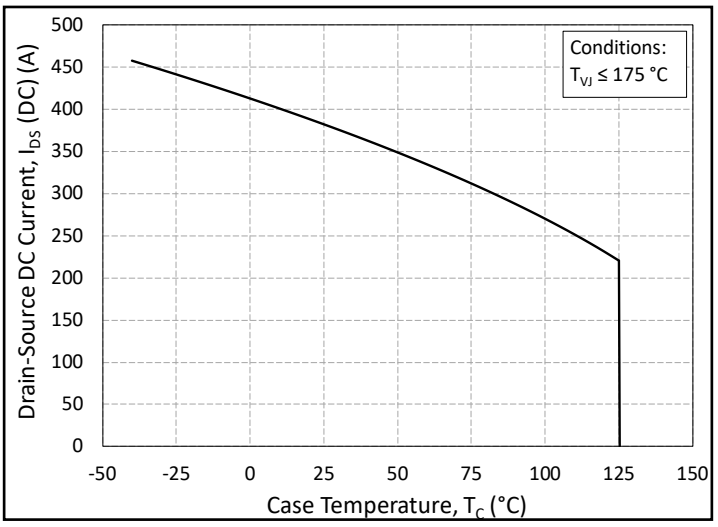


Figure 20. Continuous Drain Current Derating vs. Case Temperature

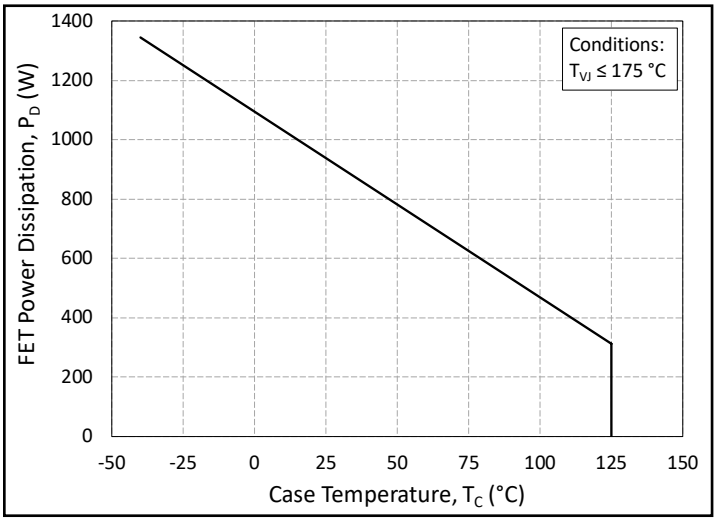


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

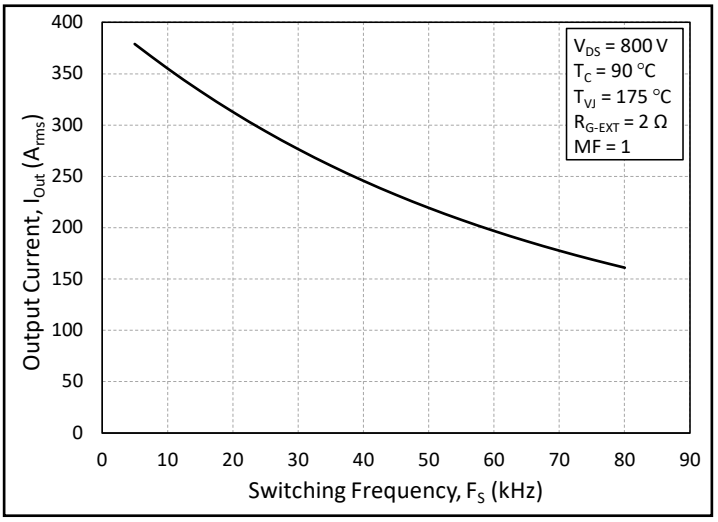


Figure 22. Typical Ouput Current Capablity vs. Switching Frequency (Inverter Application)

Timing Characteristics

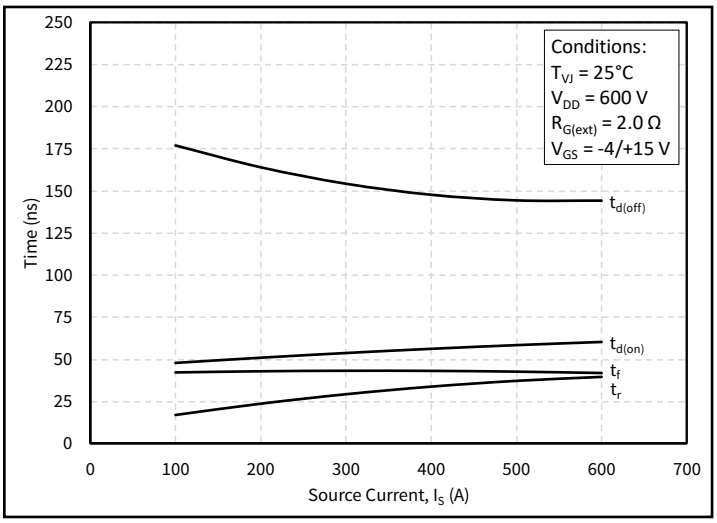


Figure 23. Timing vs. Source Current

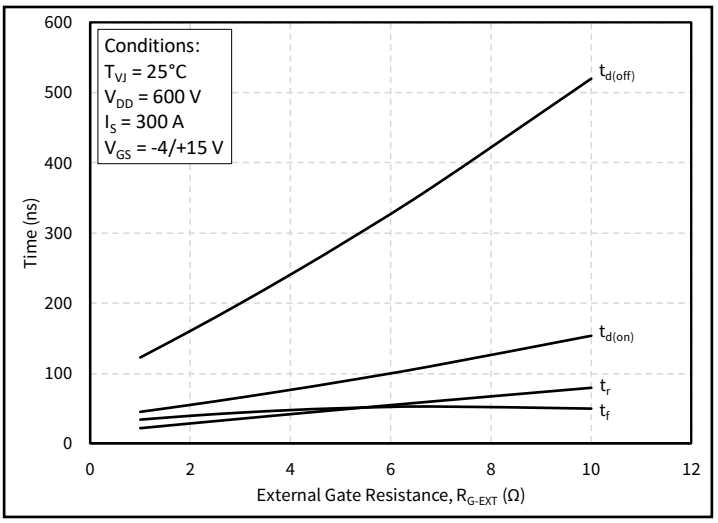


Figure 24. Timing vs. External Gate Resistance

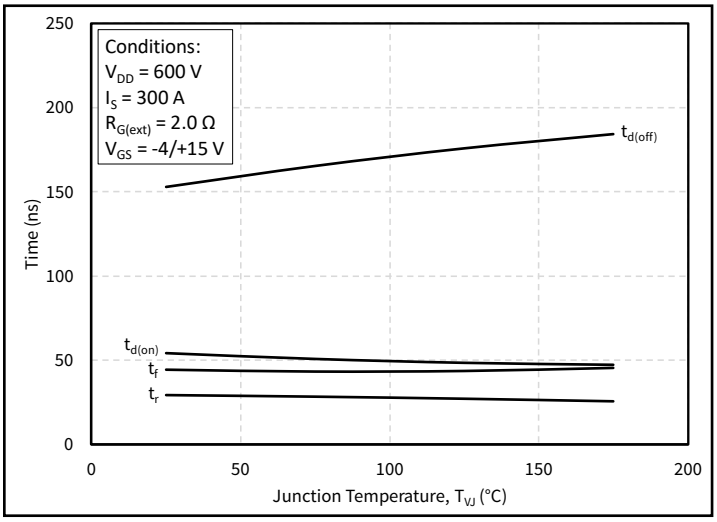


Figure 25. Timing vs. Junction Temperature

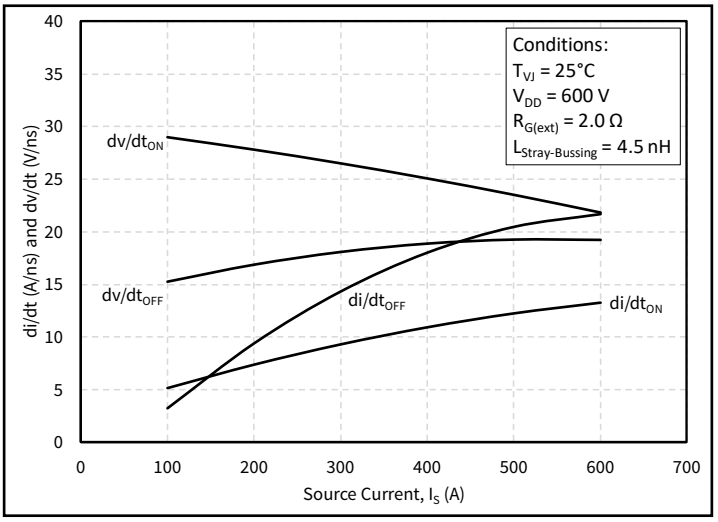


Figure 26. dv/dt and di/dt vs. Source Current

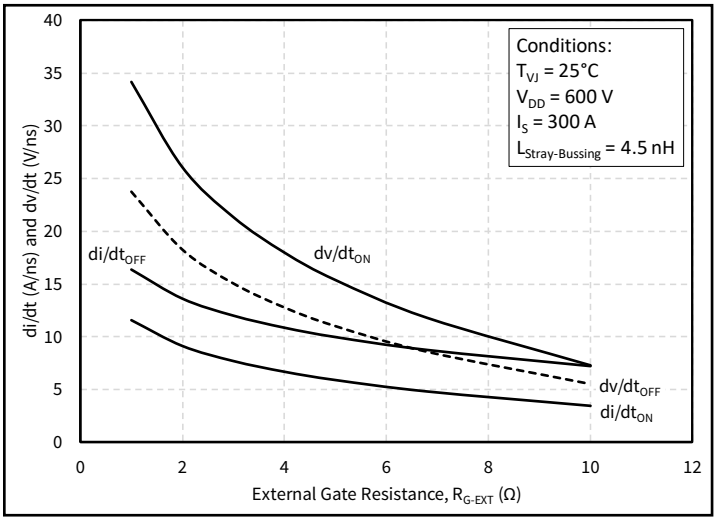


Figure 27. dv/dt and di/dt vs. External Gate Resistance

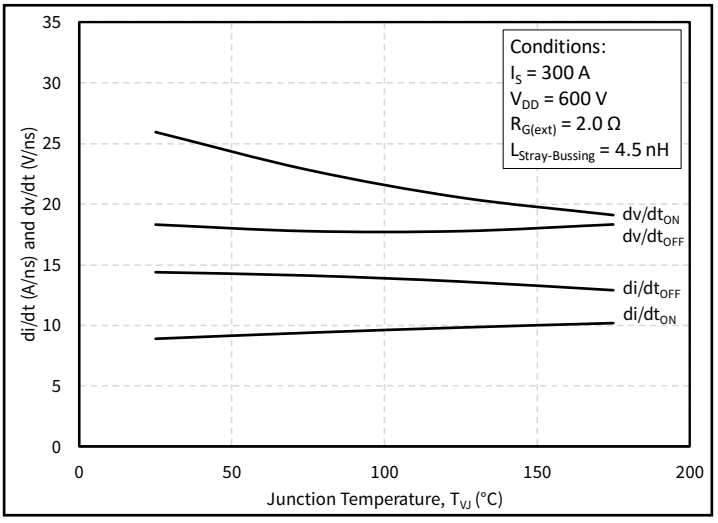


Figure 28. dv/dt and di/dt vs. Junction Temperature

Definitions

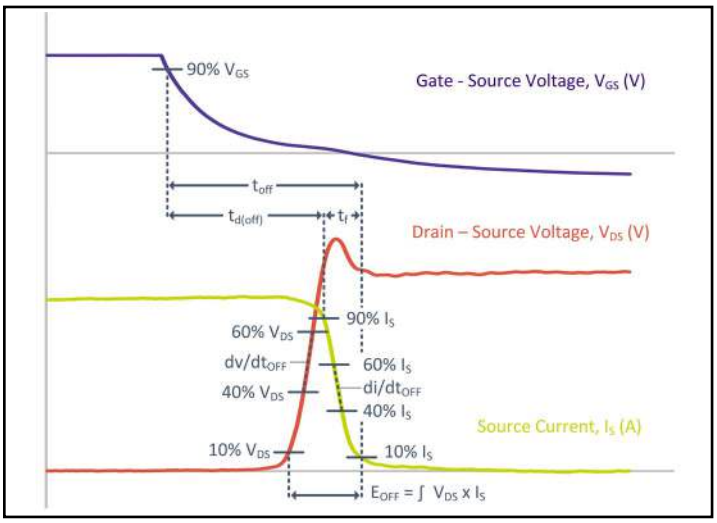


Figure 29. Turn-off Transient Definitions

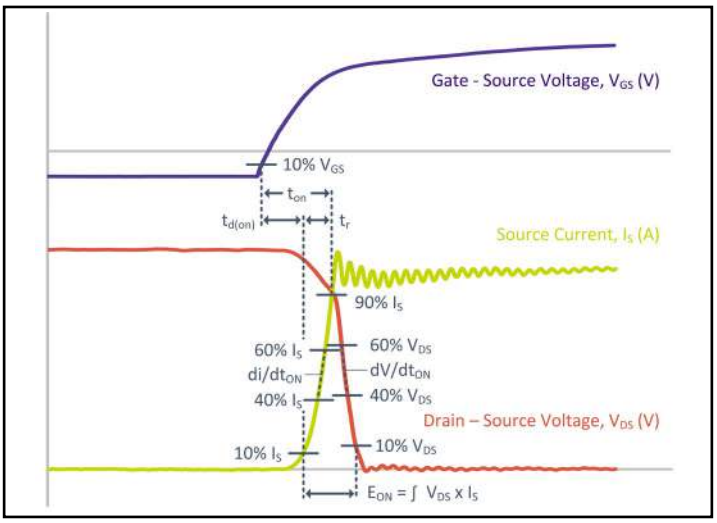


Figure 30. Turn-on Transient Definitions

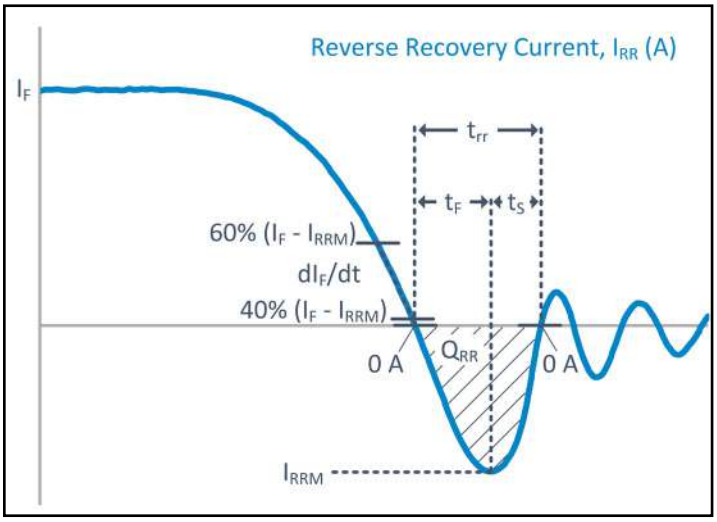


Figure 31. Reverse Recovery Definitions

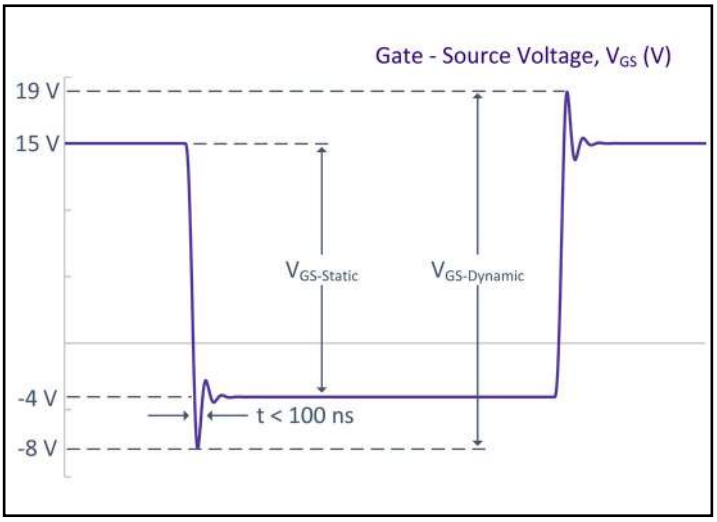
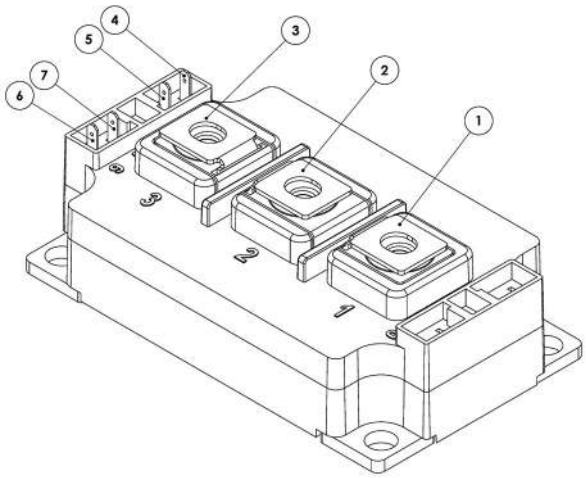
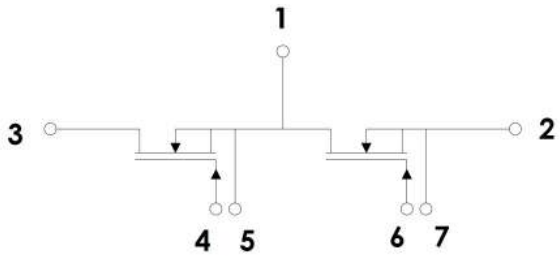


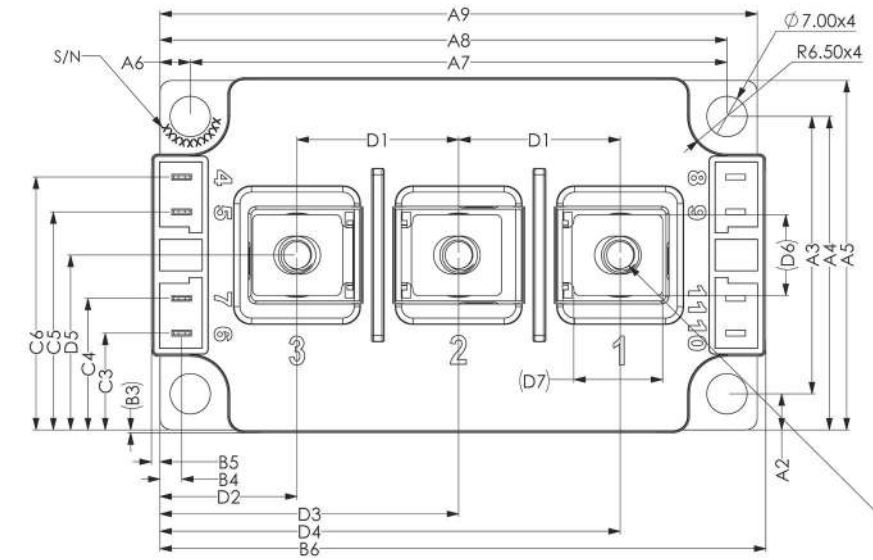
Figure 32. V_{GS} Transient Definitions

Schematic and Pin Out

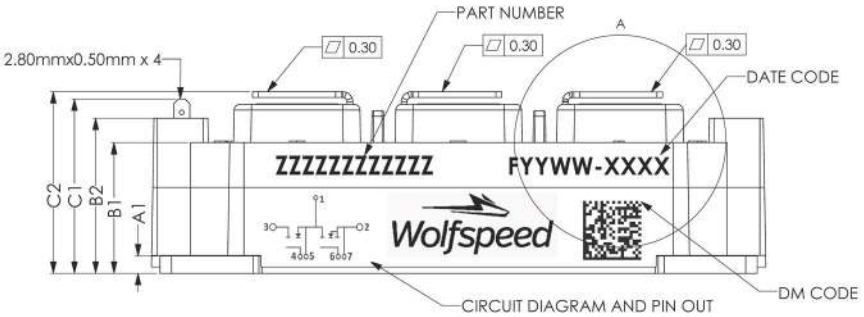


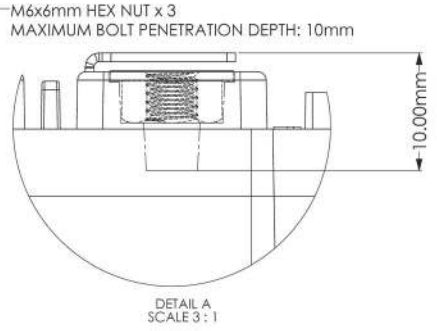


Package Dimensions (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION (mm)	TOLERANCE (mm)
A1	3.00	±0.30
A2	6.22	±0.30
A3	48.00	±0.30
A4	54.22	±0.30
A5	60.44	±0.30
A6	5.25	±0.30
A7	93	±0.30
A8	98.25	±0.30
A9	103.50	±0.30
B1	22.75	±0.30
B2	27.30	±0.30
B3	0.51 x 2	REF
B4	3.76	±0.40
B5	1.25	±0.40
B6	105.00	±0.30
C1	30.60	±0.50
C2	31.40	±0.40
C3	16.72	±0.40
C4	22.75	±0.40
C5	37.7	±0.40
C6	43.73	±0.40
D1	28.00	±0.50
D2	24.20	±0.40
D3	52.00	±0.40
D4	79.80	±0.40
D5	30.22	±0.40
D6	14.00 x 3	REF
D7	15.40 x 3	REF





3D Model (Requires Adobe Acrobat or Compatible Viewer With 3D Capability)

Supporting Links & Tools

- CGD1200HB2P-BM3 Evaluation Gate Driver
- CGD12HB00D: Differential Transceiver Board
- KIT-CRD-CIL12N-BM: Dynamic Performance Evaluation Board for the BM2 & BM3 Module (CPWR-AN-36)
- CPWR-AN-34: Module Mounting Application Note
- CPWR-AN-35: Thermal Interface Material Application Note

Notes

- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, or air traffic control systems.

- The SiC MOSFET module switches at speeds beyond what is customarily associated with IGBT-based modules. Therefore, special precautions are required to realize optimal performance. The interconnection between the gate driver and module housing needs to be as short as possible. This will afford optimal switching time and avoid the potential for device oscillation. Also, great care is required to insure minimum inductance between the module and DC link capacitors to avoid excessive VDS overshoot.